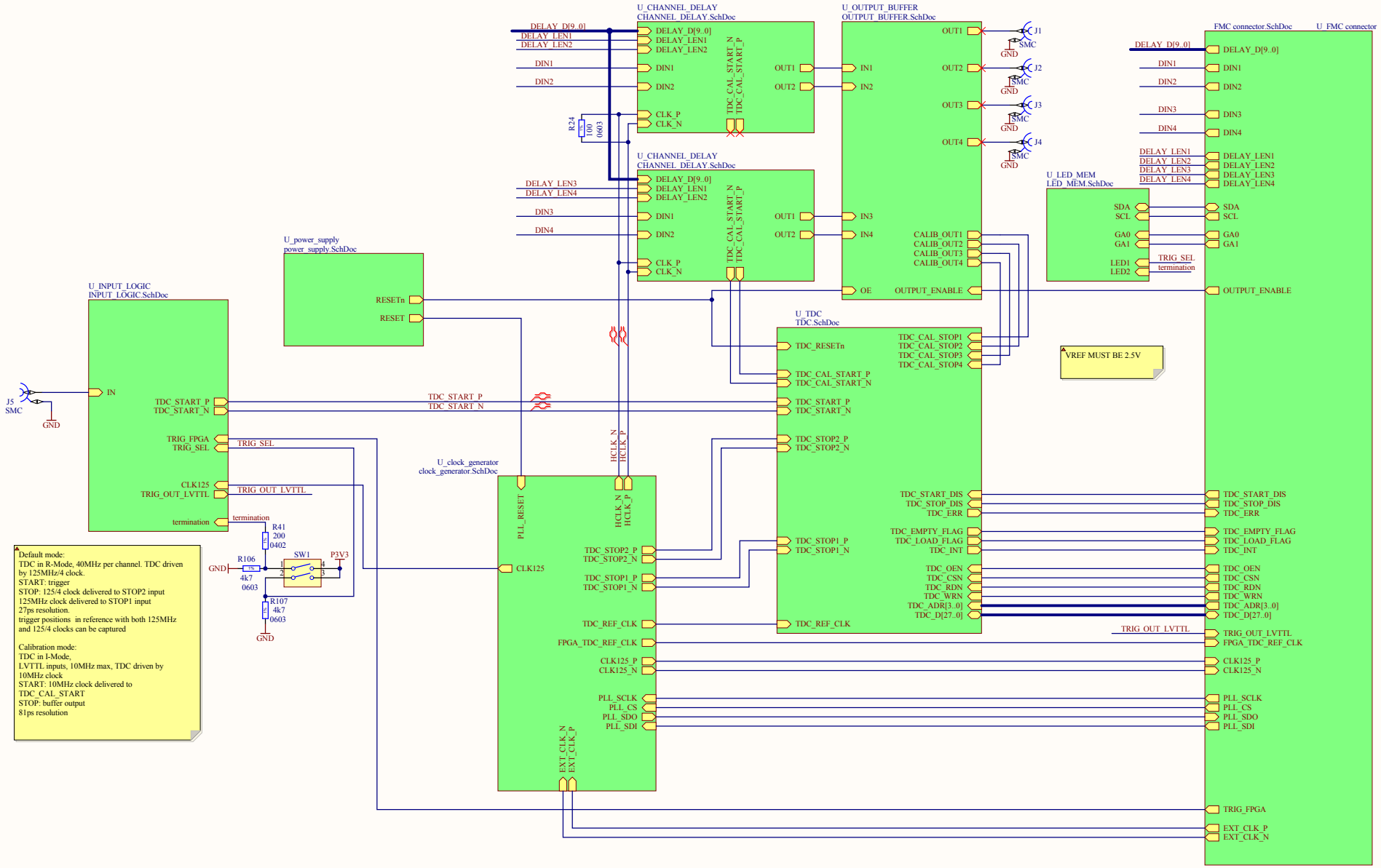
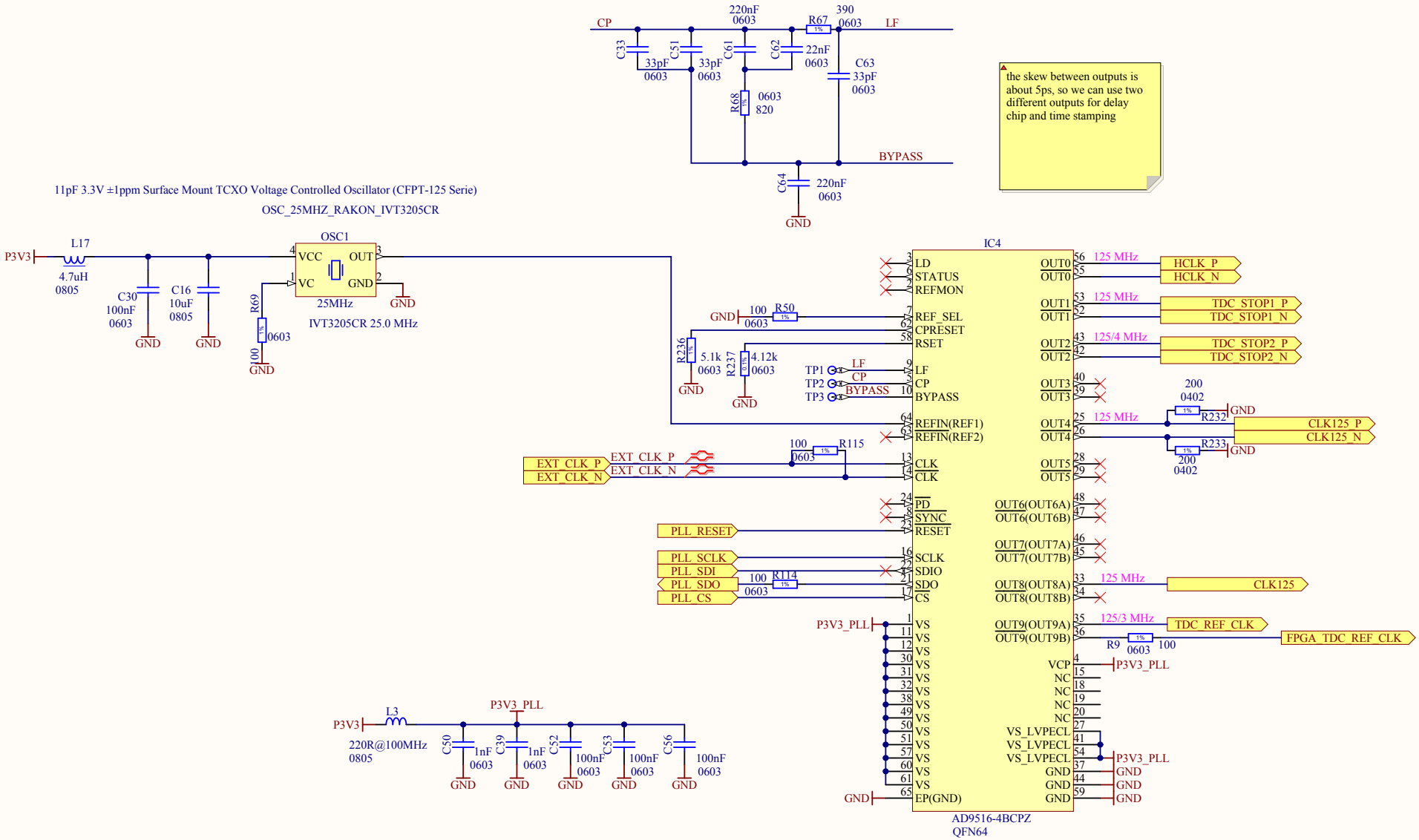

U_CHANNEL_DELAY
CHANNEL_DELAY.SchDoc
U_OUTPUT_BUFFER
OUTPUT_BUFFER.SchDoc
FMC connector.SchDoc
U_FMC connector
U_LED_MEM
LED_MEM.SchDoc
U_power_supply
power_supply.SchDoc
U_INPUT_LOGIC
INPUT_LOGIC.SchDoc
U_TDC
TDC.SchDoc
U_clock_generator
clock_generator.SchDoc
VREF MUST BE 2.5V
Default mode:
TDC in R-Mode, 40MHz per channel. TDC driven by 125MHz/4 clock.
START: trigger
STOP: 125/4 clock delivered to STOP2 input
125MHz clock delivered to STOP1 input
27ps resolution.
trigger positions in reference with both 125MHz and 125/4 clocks can be captured
Calibration mode:
TDC in I-Mode,
LVTTL inputs, 10MHz max, TDC driven by 10MHz clock
START: 10MHz clock delivered to TDC_CAL_START
STOP: buffer output
81ps resolution
Project/Equipment
FMC Delay 1ns 4cha
Document
FMC delay top
BE-CO
Designer GK
Drawn by GK
Check.by -
Last Mod. - 2010-11-12
File FMC_Delay_1ns_4Cha.SchDoc
Print Date 2010-11-12 11:36:58
Sheet 1 of 9
European Organization for Nuclear Research
CH-1211 Geneve 23 - Switzerland
EDA-XXXXX-VX-X
Size A3
Rev -



Project/Equipment	FMC Delay 1ns 4cha		
Document	**ADC clock generator**	Designer GK	
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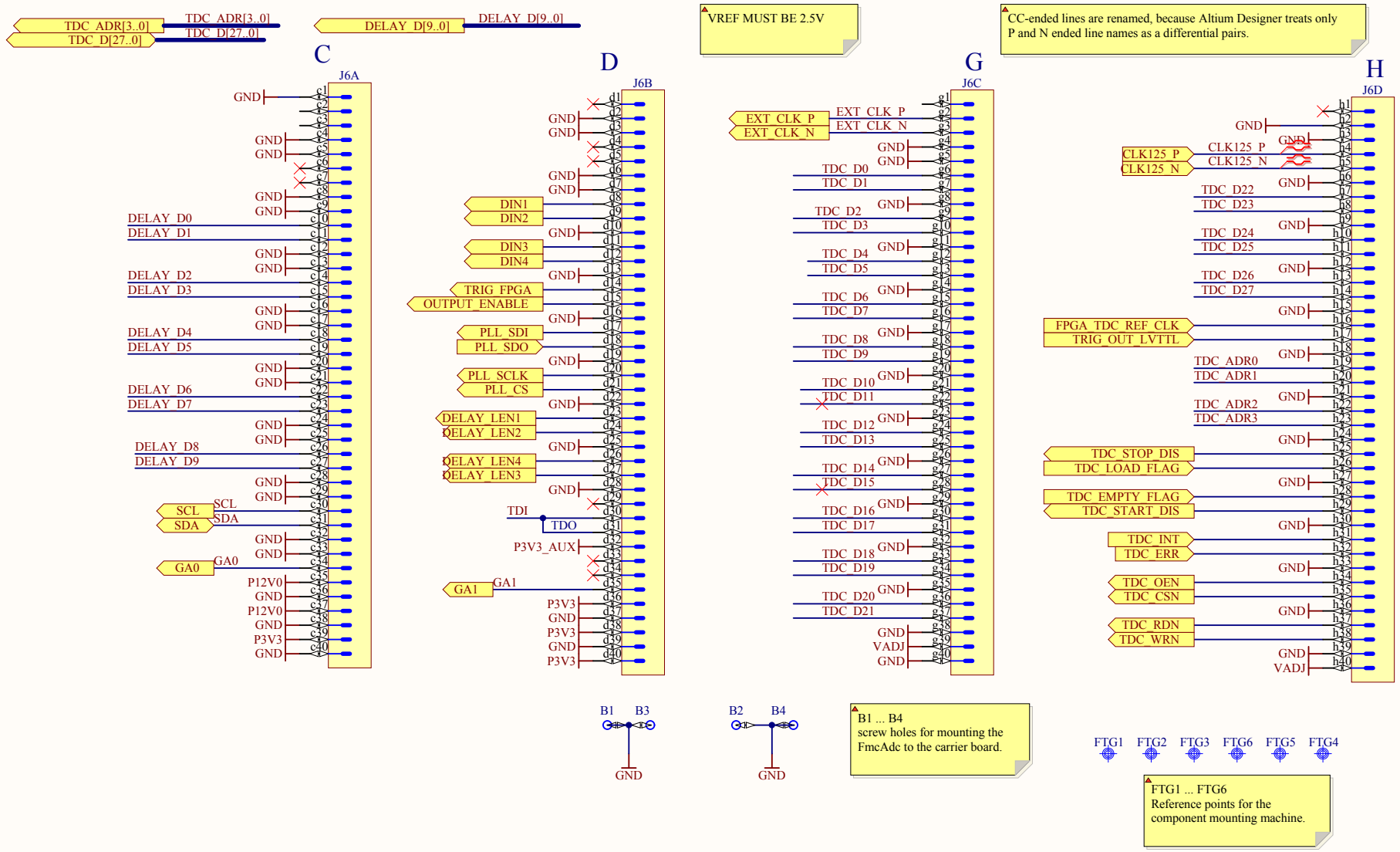
		Print Date 2010-11-12 11:36:58	Sheet 2 of 9
BE-CO	*European Organization for Nuclear Research* *CH-1211 Geneve 23 - Switzerland*	EDA-XXXXX-VX-X	Size A4 / Rev -



Project/Equipment	FMC Delay 1ns 4cha		
Document	**SAMTEC VITA 57 Low Pin Count Connector**	Designer GK	
BE-CO		Drawn by GK	
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		Last Mod. -	2010-11-11
		File FMC connector.SchDoc	
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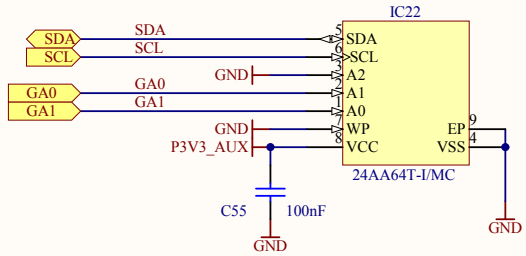
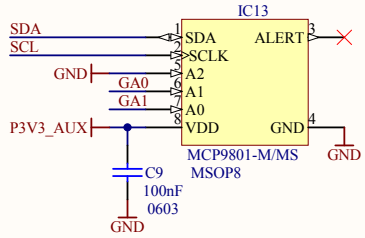
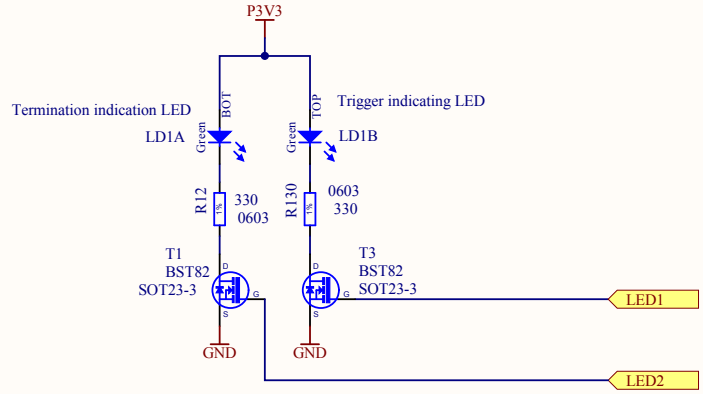
European Organization for Nuclear Research CH-1211 Geneve 23 - Switzerland	EDA-XXXXX-XX-X	Size A4	Rev -







24AA64T = 1 0 1 0 0 GA0 GA1
MCP9801 = 1 0 0 1 0 GA0 GA1

Project/Equipment	FMC Delay 1ns 4cha		
Document	**LED and MEMORY**	Designer GK	
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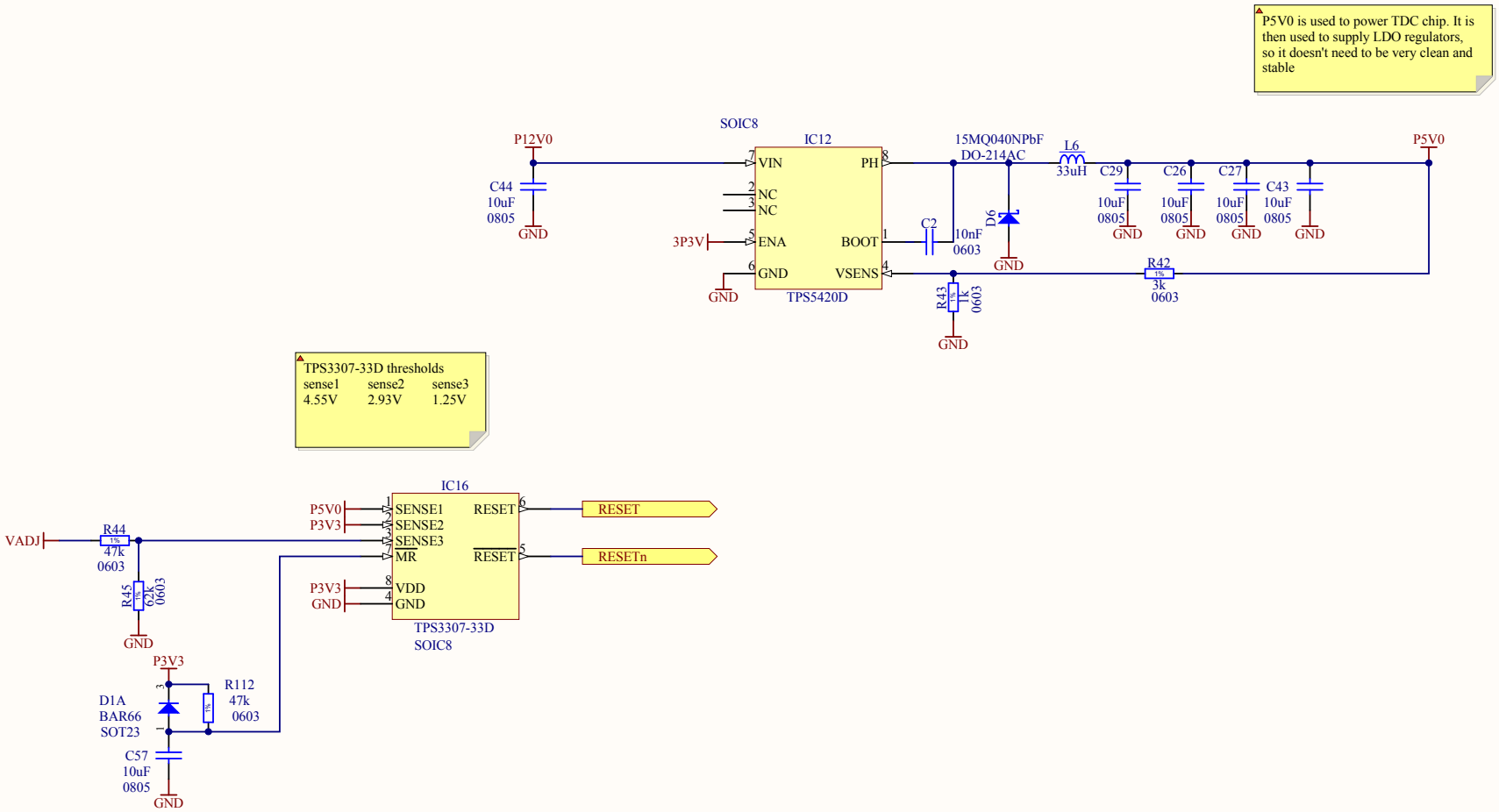
		Print Date 2010-11-12 11:36:59	Sheet 4 of 9
BE-CO	*European Organization for Nuclear Research* *CH-1211 Geneve 23 - Switzerland*	EDA-XXXXX-VX-X	Size A4 / Rev -



Project/Equipment	FMC Delay 1ns 4cha		
Document	**Power supplies** -	Designer GK	
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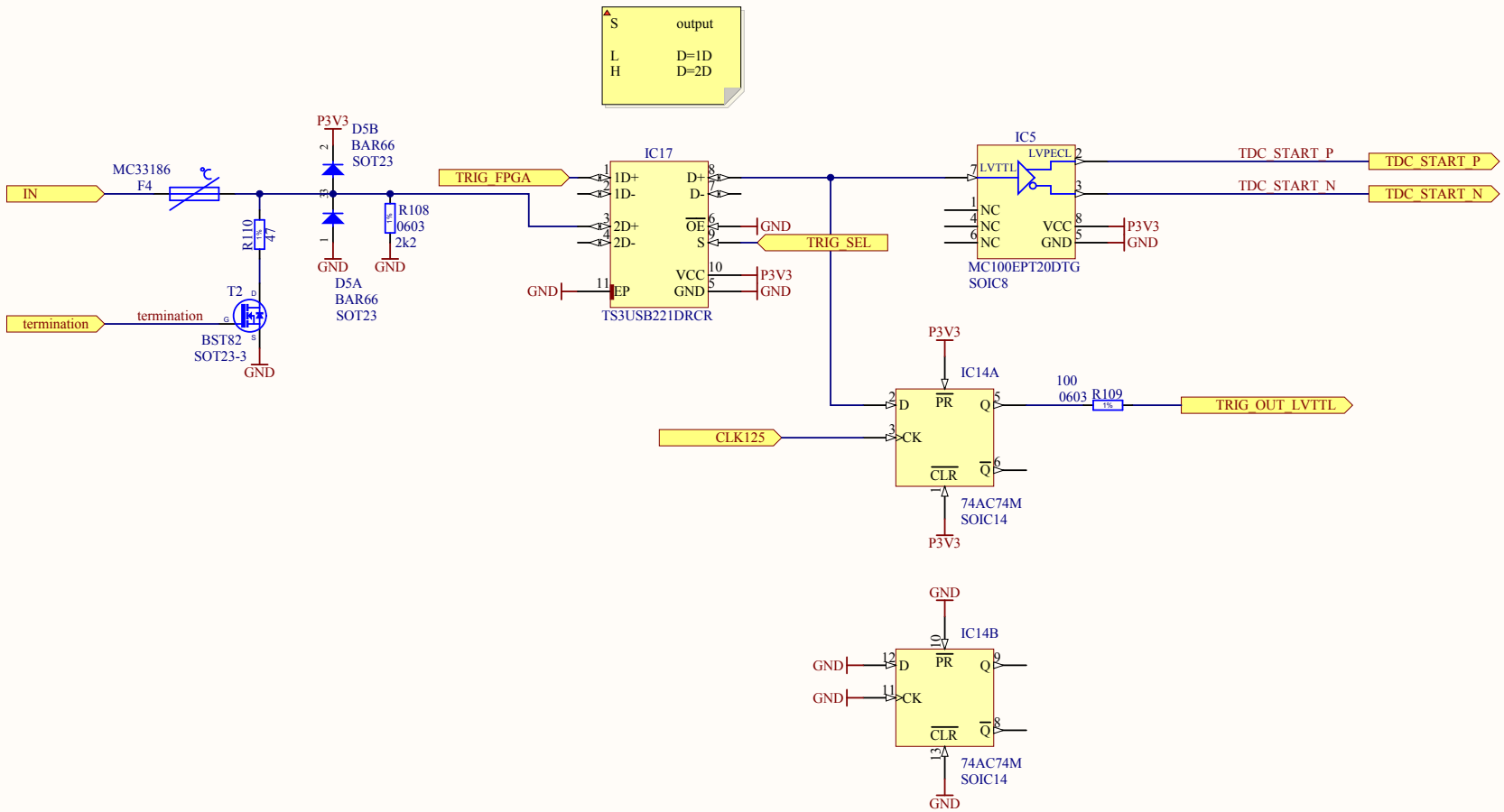
BE-CO CERN	*European Organization for Nuclear Research CH-1211 Geneve 23 - Switzerland*	EDA-XXXXX-VX-X	Size A4 / Rev -



Project/Equipment	FMC Delay 1ns 4cha		
Document	***Input logic***	Designer GK	
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		Last Mod. -	2010-11-12
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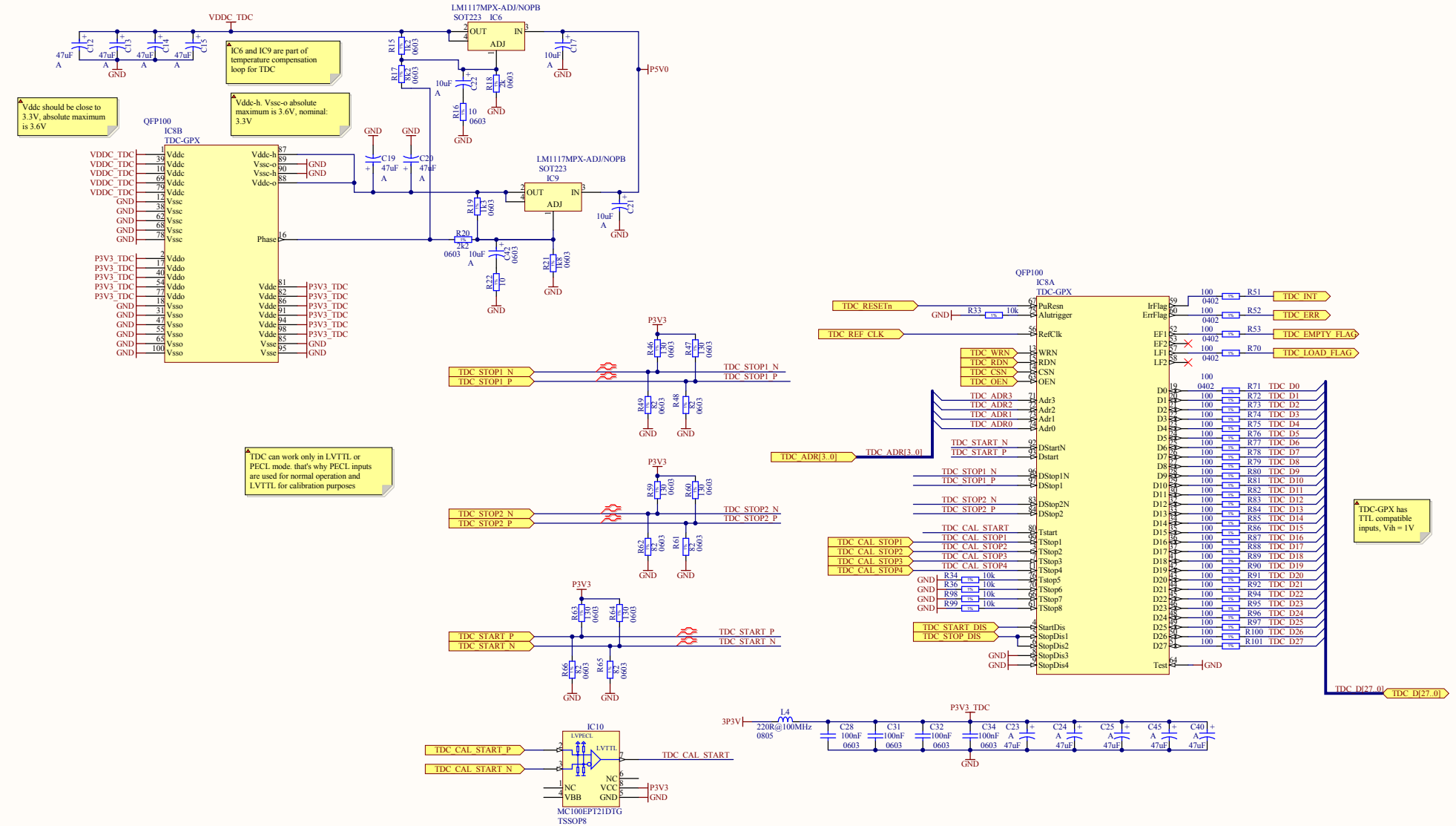
		Print Date 2010-11-12 11:36:59	Sheet 6 of 9
BE-CO	*European Organization for Nuclear Research* *CH-1211 Geneve 23 - Switzerland*	EDA-XXXXX-VX-X	Size A4 / Rev -



Project/Equipment	FMC Delay 1ns 4cha
Document	TDC
BE-CO	
Designer	GK
Drawn by	GK
Check.by	-
Last Mod.	-
File	TDC.SchDoc
Print Date	2010-11-12 11:36:59
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Sheet	7 of 9
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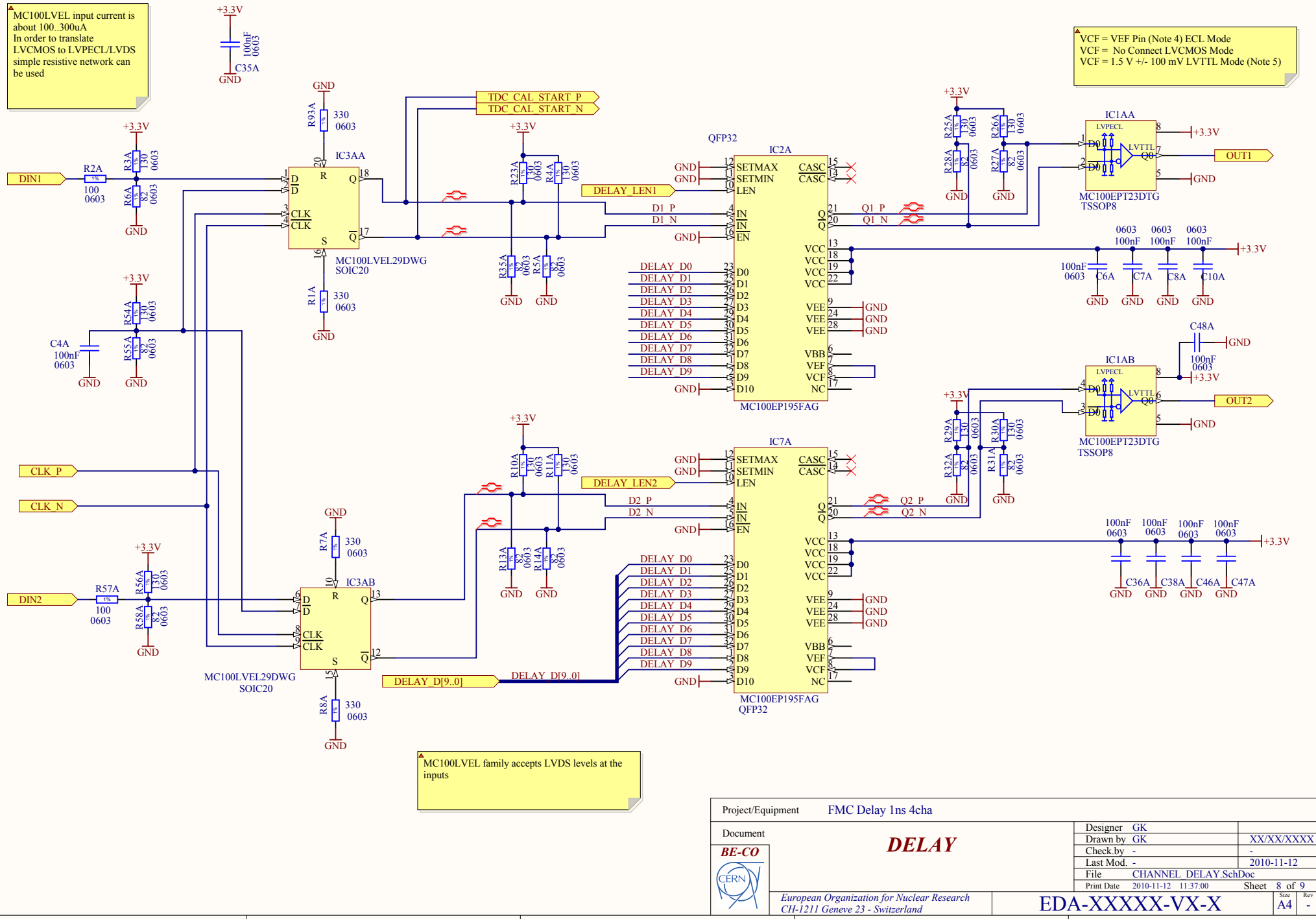
Size	A3
Rev	-


MC100LVEL input current is about 100..300uA
In order to translate LVCMOS to LVPECL/LVDS simple resistive network can be used
VCF = VEF Pin (Note 4) ECL Mode
VCF = No Connect LVCMOS Mode
VCF = 1.5 V +/- 100 mV LVTTL Mode (Note 5)
MC100LVEL family accepts LVDS levels at the inputs
TDC_CAL_START_P
TDC_CAL_START_N
DELAY_LEN1
DELAY_LEN2
DELAY_D[9..0]
DIN1
DIN2
CLK_P
CLK_N
OUT1
OUT2
IC3AA
IC3AB
IC2A
IC7A
IC1AA
IC1AB
MC100LVEL29DWG
SOIC20
MC100EP195FAG
QFP32
MC100EPT23DTG
TSSOP8
Project/Equipment FMC Delay 1ns 4cha
Document
DELAY
BE-CO
European Organization for Nuclear Research
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Designer GK
Drawn by GK
Check.by -
Last Mod. -
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Print Date 2010-11-12 11:37:00
Sheet 8 of 9
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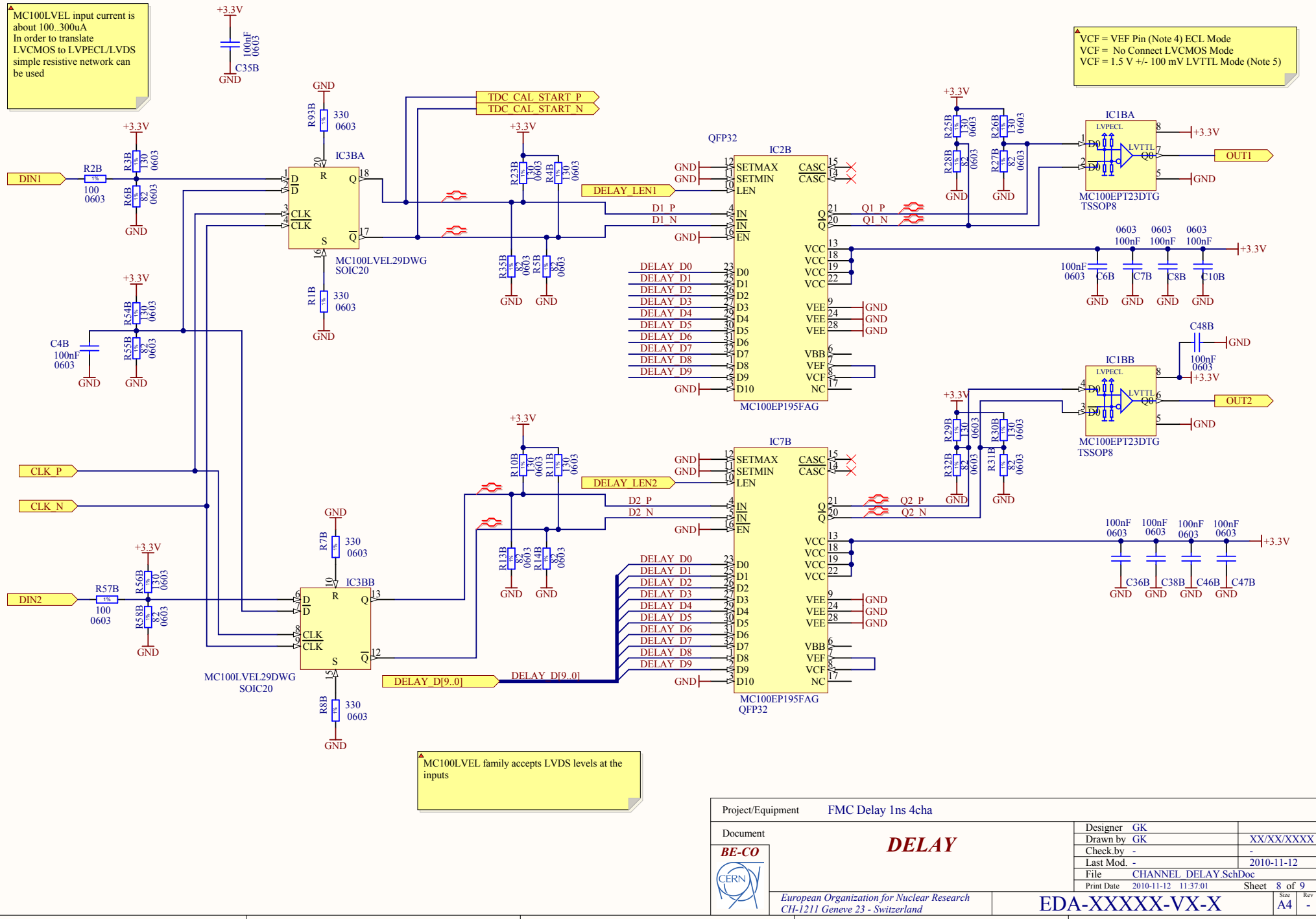
Size A4
Rev -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VCF = VEF Pin (Note 4) ECL Mode
VCF = No Connect LVCMOS Mode
VCF = 1.5 V +/- 100 mV LVTTL Mode (Note 5)
MC100LVEL family accepts LVDS levels at the inputs
TDC_CAL_START_P
TDC_CAL_START_N
DIN1
DIN2
CLK_P
CLK_N
DELAY_LEN1
DELAY_LEN2
DELAY_D[9..0]
D1_P
D1_N
D2_P
D2_N
Q1_P
Q1_N
Q2_P
Q2_N
OUT1
OUT2
IC1BA
IC1BB
IC2B
IC3BA
IC3BB
IC7B
MC100EPT23DTG
TSSOP8
MC100LVEL29DWG
SOIC20
MC100EP195FAG
QFP32
Project/Equipment FMC Delay 1ns 4cha
Document
DELAY
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Check.by -
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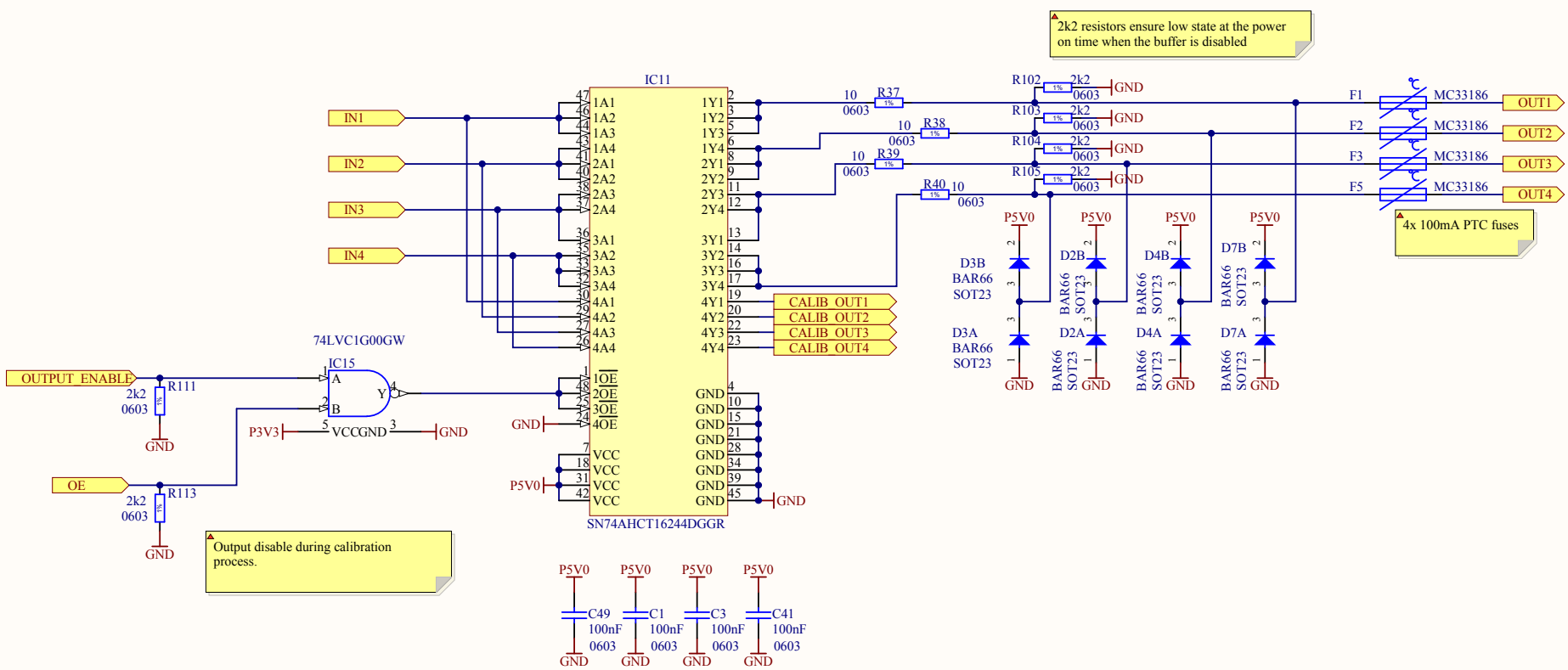

Project/Equipment	FMC Delay 1ns 4cha		
Document	**Output buffer**	Designer GK	
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		Last Mod. -	2010-11-12
		File OUTPUT_BUFFER.SchDoc	
		Print Date 2010-11-12 11:37:01	Sheet 9 of 9
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