FMC Delay 1ns 4cha (Fine Delay)
Long term test report

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1 Introduction

This report provides a summary of tests performed on a specimen of the Fine Delay (FmcDelay1ns4cha, further abbreviated as FD) card [2]. The purpose of these tests was to:

- Check the stability of the card's operation over a long period of time.
- Gather statistics of trigger-to-output delay.

The report does not cover all possible delay values, as it would be impractical due to very wide delay range (up to 120 seconds) supported by the FD. The VHDL was designed and verified on simulation in such a way that passing the long term test at a single delay setting automatically proves stability for other delay values (as the test assumes that trigger pulses are uncorrelated with the card's reference clock).

2 Measurements

2.1 Setup

The measurement system used is depicted in Figure 1. It consists of:

- Pulse source: a HP 33250A waveform generator (S/N: MY40001267).
- Time interval meter: Pendulum CNT-91 [5] (S/N: 205575), measuring the trigger-to-output delay of the FD mezzanine. Only 1 output of the FD was used, as other outputs have an identical structure (and we don't have enough CNT-91's...).
- FD mezzanine (version V5-2 [1], S/N: CR000010) under test with a SVEC carrier [4], hosted in a VME64x crate with a MEN A20 controller.
- PC running Linux for data logging and controlling the CNT-91 TDC.
- Software for the MEN A20 and the PC for data logging (C program and some Python scripts). Temperature and timestamp data were sent from the VME crate to the PC via a TCP connection.

The card's trigger input was fed with 2 microsecond-wide pulses of 3 V amplitude and a 100 Hz rate, with a 50 Ω input termination. The card was configured to introduce a 700 ns delay. A low delay value was chosen to eliminate the drift of the local oscillator from the results (which in the long term could hide random/spurious artifacts such as incorrect FD's TDC timestamps).

For each trigger pulse, the following parameters were recorded:

- Trigger-to-output delay, measured with the CNT-91.
- Board temperature, measured using the integrated temperature sensor.
- TDC timestamp, read by the driver.

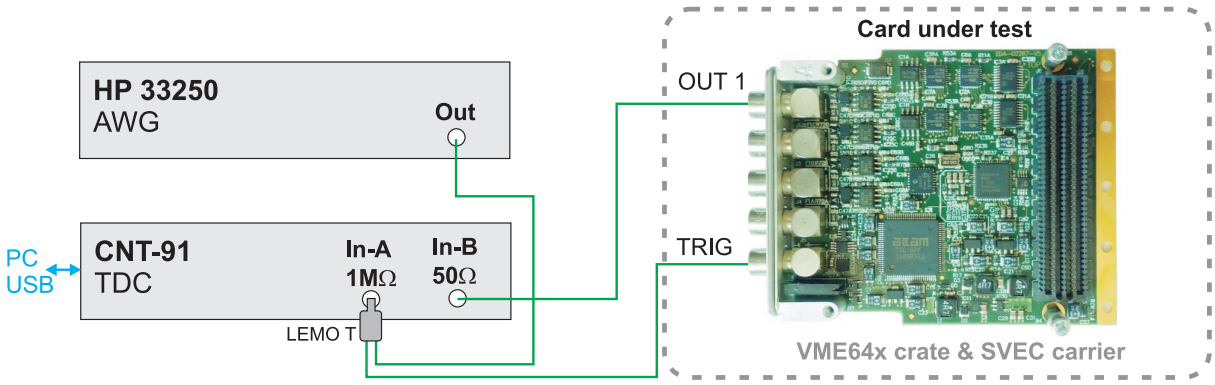

Figure 1: Long term measurement setup.

2.2 Results

The tests consist of two continuous runs, one of 14 days and another of 34.5 days, that is 48.5 days in total. There was a short gap between the two series caused by reconfiguration of the CERN network.

Table 1 summarizes all the samples gathered. The uncorrected jitter value is based on raw delay measurements taken from the CNT-91. The corrected one compensates for the the jitter of the CNT-91 (done by subtracting squared standard deviations assuming that both CNT-91 and FD jitter is of Gaussian shape and independent).

Table 1: Long term delay statistics.

Parameter	**Value**
Total samples	419,157,455
Cabling delay	12.7 ns
Average delay	699.94 ns
Maximum delay	700.54 ns
Minimum delay	699.5 ns
Worst case error	0.59 ns
Uncorrected rms jitter	72 ps
CNT-91 rms jitter	31 ps
Corrected rms jitter	65 ps
CNT-91 maximium delay	-0.12 ns
CNT-91 minimium delay	0.12 ns
Minimum temperature	65 degrees C
Maximum temperature	68 degrees C

Short-term stability was characterized by picking a 1-minute long averaging window. The results are presented in Table 2.

The plot in Figure 2 visualizes the short term average, minimum and maximum delay values.

During the entire test, 3 events outside the specified range were discovered:

- sample 114714751: 697.67 ns (-2.33 ns error)
- sample 391199777: 700.86 ns (0.86 ns error)
- sample 406143035: 702.16 ns (2.16 ns error)

We attribute these errors to the ACAM TDC [6], as they exist both in the timestamps read out by the driver (the input signal is periodic) and in the measured delays. Similar events have been observed for the *FmcTdc* card [7] and in older versions of the FD firmware, where the TDC works in a different mode (respectively, I- and R-modes).

Table 2: Short term delay statistics.

Parameter	**Value**
Number of samples	6000
Average delay	699.93 ns
Maximum delay	700.28 ns
Minimum delay	699.62 ns
Worst case error (wrs to the average delay)	300 ps
Typical ACAM rms jiitter	41 ps
Delay line rms jitter	10 ps
Theoretical rms jitter	42 ps
Measured rms jitter	57 ps

To our knowledge, this test is the first public, long term stability test of the ACAM TDC-GPX chip. Given the size of the statistics data, 3 out of 420 million events are extremely rare (below 7 sigma threshold) and do not exceed 2.5 ns (the typical applications advertised for this chip, such as PET tomography, spectroscopy of laser rangefinders are likely not concerned by such a low error rate).

The plot in Figure 3 shows the histogram of the jitter in the measured delay values. It resembles a gaussian shape. Note that certain bins are empty due to the discrete nature of both the FD and the CNT-91.

3 Summary

Final results have confirmed long term stability and compliance of the card with the specification:

- Absolute delay accuracy is better than 1 ns,
- Input-to-output rms jitter (standard deviation) is better than 100 ps.

Further testing with a climatic chamber could be performed to determine the effects of temperature on the jitter and accuracy, and allow the software to compensate for them, if needed.

References

[1] Official schematics and PCB design (CERN EDMS), `https://edms.cern.ch/nav/EDA-02267-V5-2`

[2] Fine Delay hardware homepage and Wiki, `http://www.ohwr.org/projects/fmc-delay-1ns-8cha`

[3] Official user's manual, `http://www.ohwr.org/documents/179`

[4] SVEC FMC Carrier Project, `http://ohwr.org/projects/svec`

[5] Pendulum CNT-91 TDC/Frequency meter, manufacturer's website

[6] ACAM TDC-GPX TDC chip, `http://www.acam.de/products/time-to-digital-converter/tdc-gpx`

[7] FmcTdc1ns5cha project, `http://www.ohwr.org/projects/fmc-tdc`

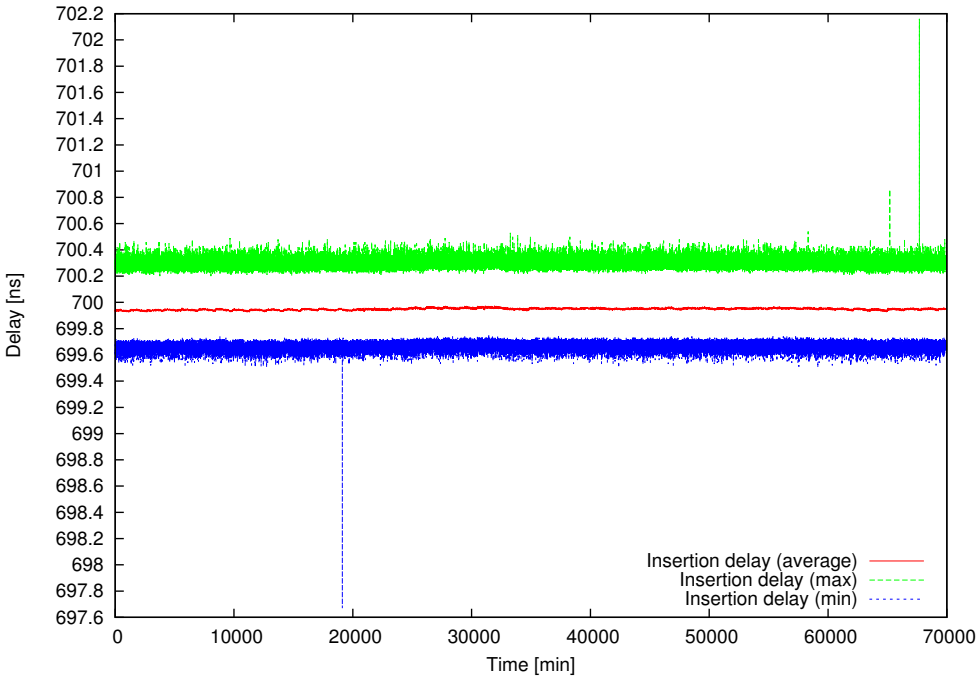

Figure 2: Average, minimum and maximum trigger-to-output delay (sliding average with a 1-minute window).

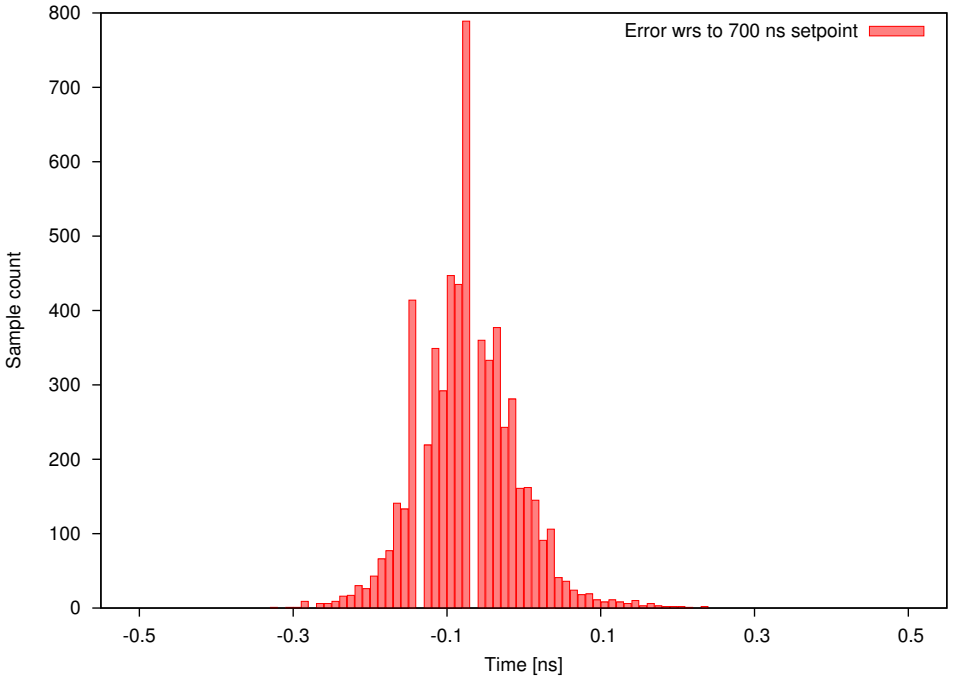

Figure 3: Histogram of trigger-to-output jitter.