

FMC Digital I/O (version 2)

On the hardware design

Tomasz Włostowski (CERN)

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1 Introduction

Note: this is a developers-only informal description of the card. Please don't treat it as official documentation.

The 5-channel Digital I/O FMC mezzanine (further abbreviated as DIO) was designed primarily for the purpose of demonstrating the capabilities of White Rabbit PTP Core (WRPC) running on the SPEC card. The role of the DIO was to provide physical connection and conditioning of timing signals, as SPEC cards do not have any easily-accessible I/O connectors. The DIO can also serve any FMC application as a general purpose digital I/O card.

2 Functional requirements

- 5 input/output ports with independently programmable direction (Lemo 00 connectors).
5 is the maximum number of Lemo or SMx sockets that could be fit on an FMC front panel. Lemo 00 was chosen due to its wide spread in scientific applications.
- Output levels: LVTTTL, capable of driving +2.5 V over a 50 Ω load. At power-up the outputs are in Hi-Z state (V1-2 and higher)
The choice of LVTTTL-level outputs results from +3.3 V FMC supply voltage and difficulties with designing a reasonably simple and cheap output stage capable of driving TTL levels on a 50 Ω load. LVTTTL output levels can also correctly drive 5 volt TTL inputs (since $V_{ih} = 2$ V is same for both standards). Hi-Z state at power up requirement is to avoid damaging any equipment connected to the card when there is no FPGA gateway loaded.
- Input levels: any logic standard from $V_{ih} = 1$ V to $V_{ih} = 5$ V (programmable threshold)
The input switching threshold is programmable by means of a DAC and a comparator. The reason is interoperability with cesium clocks and GPS receivers (sine wave 10 MHz output), low output current drivers incapable of exceeding LVTTTL threshold on a 50 Ω load and low-voltage FPGA outputs (1.2 V LVCMOS and similar).
- Output Rise/fall times: max. 2 ns.
Since the card is mainly a White Rabbit demonstrator, its outputs signals must be sharp enough to clearly show WR's sub-nanosecond accuracy.
- I/O bandwidth: 200 MHz
The card should be capable of inputting/outputting Gigabit Ethernet reference clock (125 MHz). 200 MHz looks like a reasonable safety margin.
- Programmable 50 Ω input termination in each channel
Made programmable because not all sources can correctly drive 50 Ω loads.
- LVDS I/O on the carrier side
The first reason is ensuring good signal integrity. All FMC LAx traces are routed as differential pairs on the carrier, so using them in single-ended mode would result in excessive crosstalk between the adjacent traces. The second reason is Xilinx-specific: only pins configured in differential mode can be used with IOSERDES cells (1 Gbit serdes). These cells can be employed as zero-cost TDCs or programmable pulse generators with 1 ns resolution.
- One of the inputs is capable of driving a global clock net in the carrier's FPGA.
Another FPGA-specific WR PTP Core requirement. When in PTP grandmaster mode, a 10 MHz reference from cesium or GPS clock is multiplied by a digital PLL inside the FPGA to obtain the Sync-E 125 MHz clock. The input to that PLL must be a global clock net to ensure FPGA routability.
- Inputs protected against +15 V pulses with a pulse width of up to 10 us with 50 Hz repetition rate.
Prevents damage of the card when connected, for example, to a blocking driver.

3 The design

3.1 Block diagram

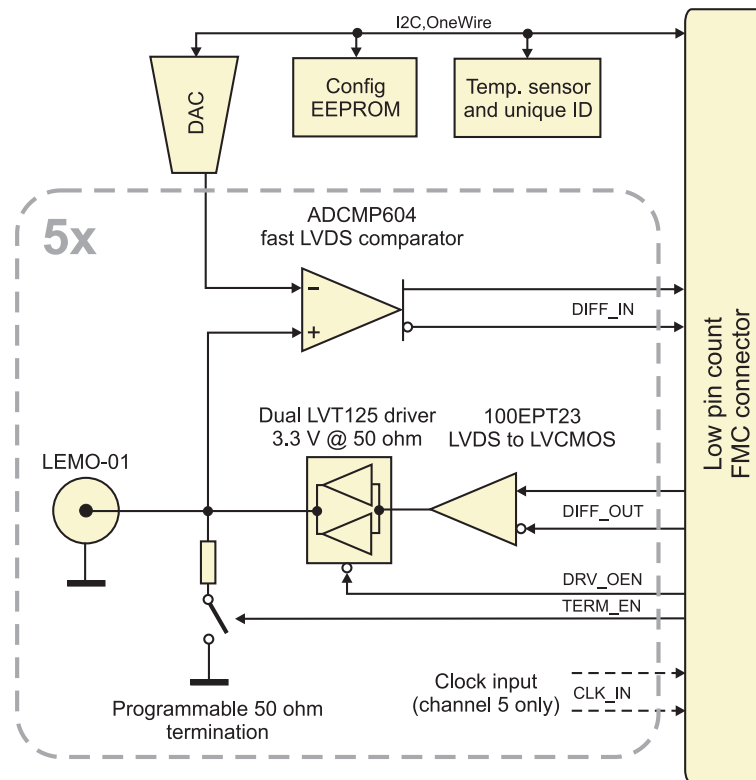


Figure 3.1: Block diagram of the DIO card (irrelevant connections and components such as decoupling capacitors were removed).

3.2 Input/output stage

Figure 3.2 shows the simplified schematic of a single DIO channel. The first obstacle on the way of the input signal is the I/O protection circuit, consisting of the fuse F1, diodes D1A, D1B and the bias voltage generator in the red rectangle. D1 is a fast PIN diode designed for ESD and overvoltage protection (capable of handling short transients of dozens of amperes). It simply clips the input signal to (PROTECT + 1.2 V) on the positive side (= approx. 5.2 V) and -1 V on the negative one. The voltage on PROTECT net is determined by the Zener diode D4. The diode is normally biased from +12 V power supply by R8 and R10. When the card is not powered, D4 works as a shunt voltage limiter. The capacitor C4 shorts fast spikes, where the Zener diode alone would react too slowly. The role of the fuse F1 is to prevent damage when a high-current DC/AC source is connected to the input (for example, a power supply cable). In such case, the fuse will trigger before the D1 maximum sustained current is exceeded (140 mA vs 200 mA). The fuse is resettable - leave the card disconnected for 2 minutes for the fuse to recover.

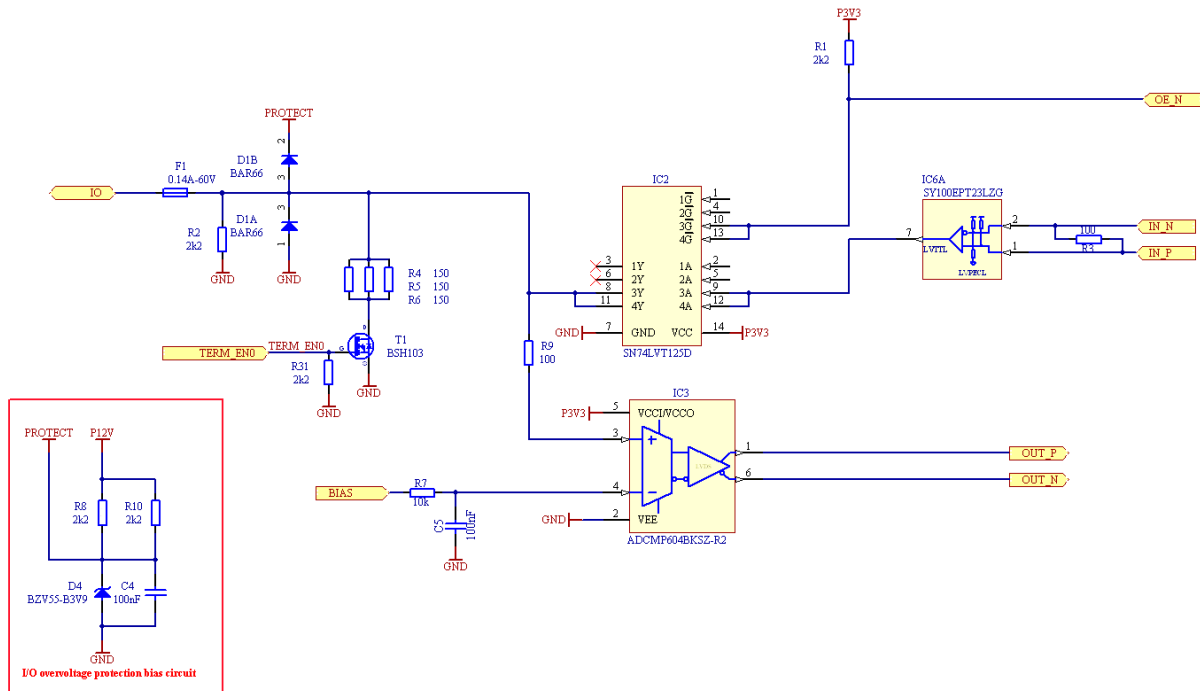


Figure 3.2: Schematic of a single DIO channel.

Figure 3.3 depicts example waveforms on pin 3 of D2 when inputs are clipping. For a 15 V input signal (pulses of 50 ms), the measured thresholds are -0.8 V and 5.7 V. The latter falls within the maximum ratings of both the LVT125 buffer and the ADCMP604 comparator (+7 V and +6.5 V). The former causes input clamping current in LVT125 of approx. 50 mA, because the internal protection diodes of LVT125 have lower voltage dropout than BAR66. Since 50 mA is the maximum allowable value, the specification only guarantees protection against positive pulses (although tests have shown no undervoltage-caused damage).

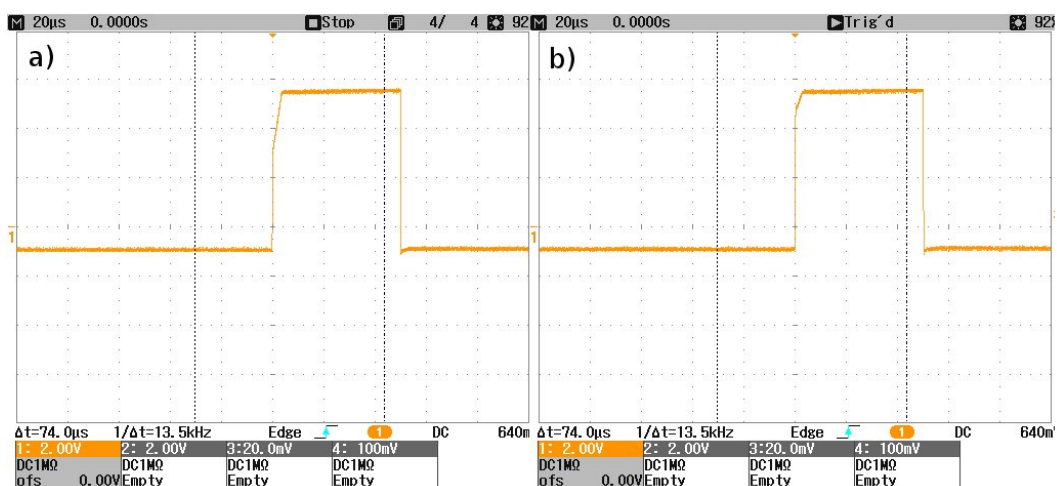


Figure 3.3: Clipping waveforms (a – card is unpowered, b – powered).

If the channel is configured as input, but not connected, R2 ensures it's in low state. R4..R6 and T1 form a programmable 50 Ω termination switch, by default disabled by pulldown R31.

The conditioned input signal is fed to the positive input of comparator IC3 via resistor R9 (to limit input clamping current). The negative input of IC3 is connected to a bias voltage

produced by a DAC. This allows for adapting the input switching threshold to any single ended logic standard between 1 V LVCMOS and 5 V TTL. The RC filter R7-C5 placed right next to the comparator reduces noise in the bias voltage. The LVDS output of the comparator goes straight to the FMC connector pins.

The output stage consists of a dual LVDS to LVTTTL buffer IC6A (SY100EPT23) followed by the main output driver (of IC2, SN74LVT125D). Since each output comprises two LVT125 buffers connected in parallel, it is possible to drive 2.5 V on a 50 Ω load with 2 ns rising edge (see Figure 3.4). Jitter is not critical here, as the outputs are anyway driven by quite jittery FPGA pins. The LVT125D buffers are compatible with 5 V logic levels. Outputs are disabled by default thanks to the pullup R1.

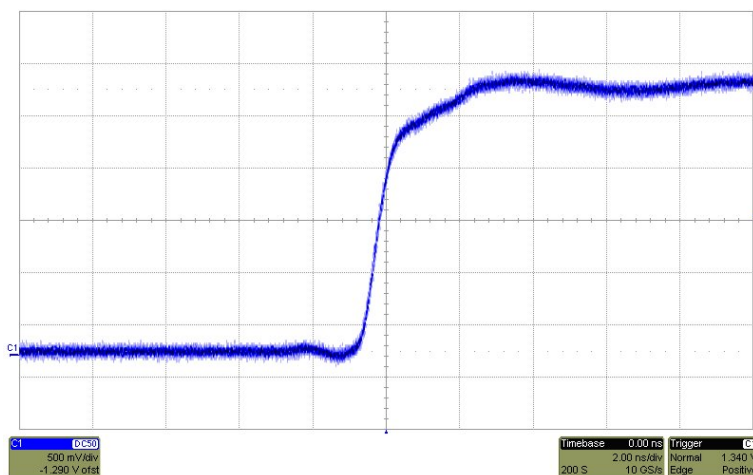


Figure 3.4: Rising edge of the output signal.

3.3 Other components

The only remaining DIO-specific part is IC11 which controls the input switching threshold. It is an 8-bit, 8-channel DAC driven by I2C. The default output value is 1.65 V, therefore even when unprogrammed, outputs will work correctly with LVTTTL25/LVTTTL33/TTL levels.

The rest of the card is standard for FMCs designed in our section: identification EEPROM IC9 (24AA64), 1-Wire temperature sensor IC10 (also acting as the unique ID of the card) and two user-programmable LEDs (LD1).

4 References

1. Project's wiki: <http://www.ohwr.org/projects/fmc-dio-5chttla/wiki>.
2. SPEC Card project: <http://www.ohwr.org/projects/spec>
3. White Rabbit PTP Core: http://www.ohwr.org/projects/wr-cores/wiki/Wrpc_core. Contains example code with I/O differential buffer instantiation.