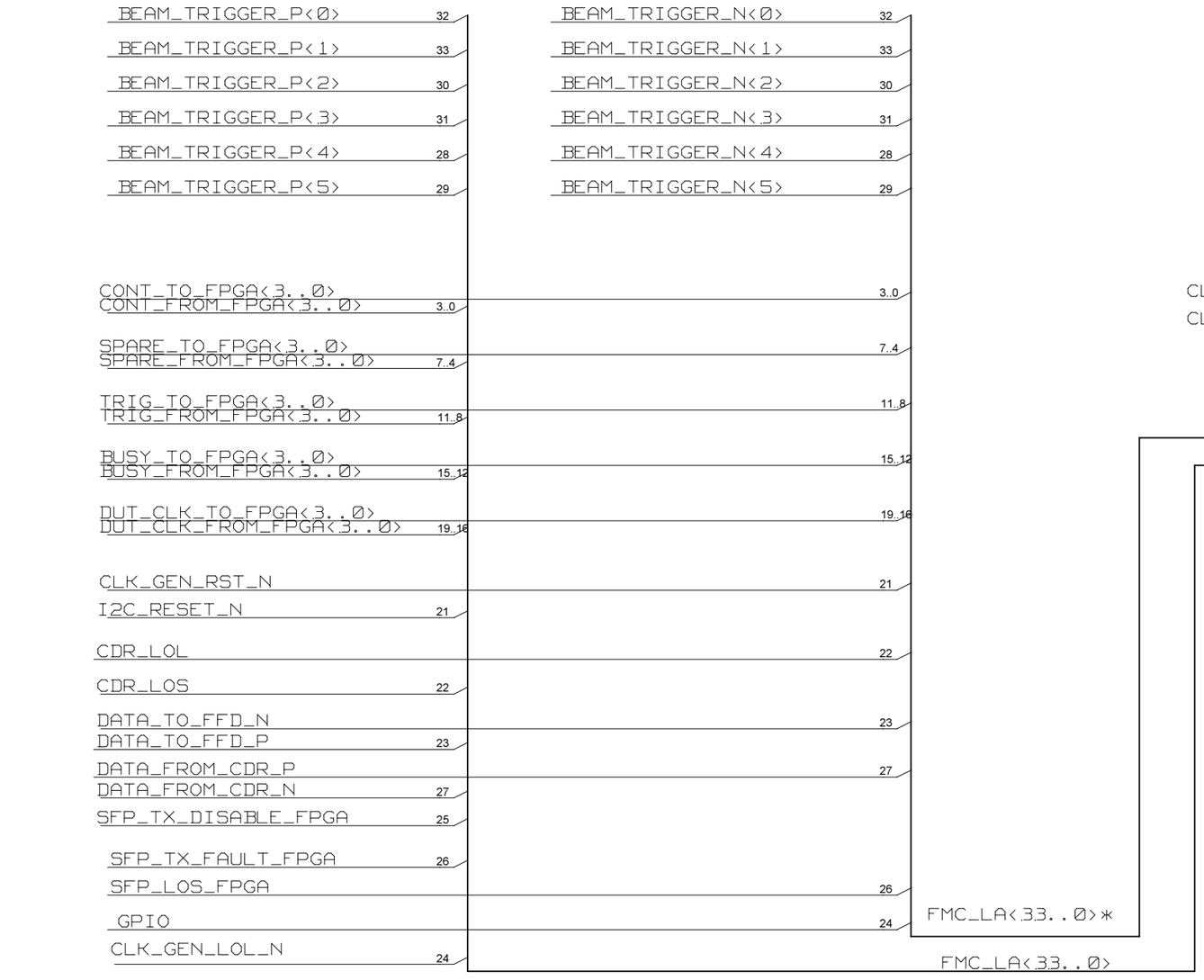
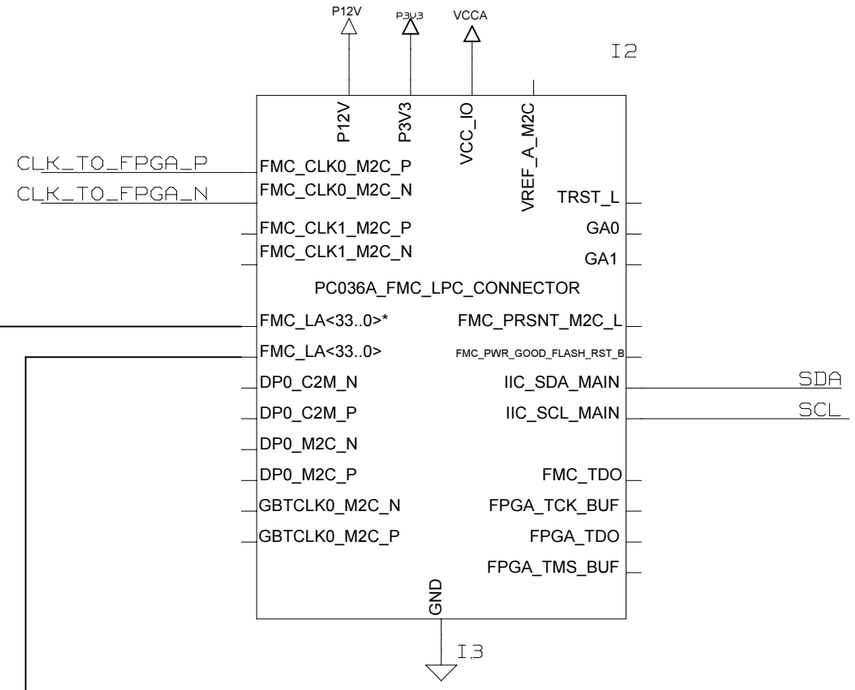
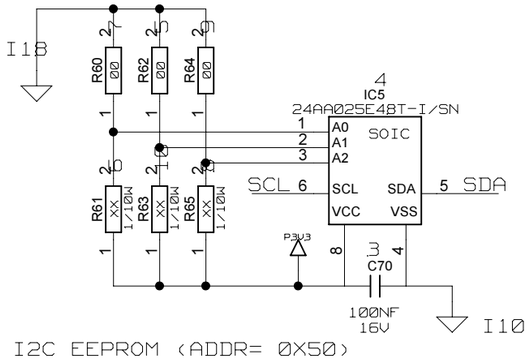
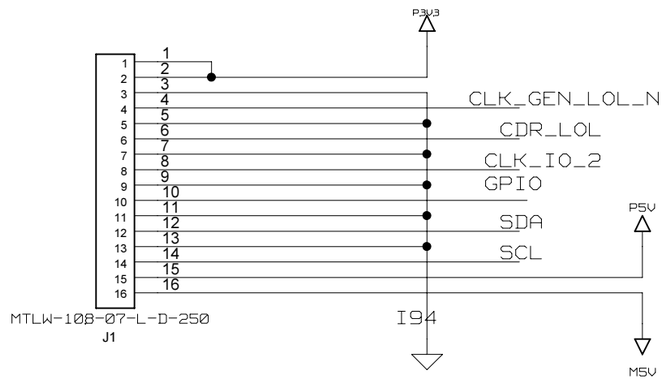


VCC_IO IS DETERMINED BY THE SETTING ON THE FPGA BOARD.
FOR TLU ENSURE IT IS 3.3V





I2C EEPROM (ADDR= 0X50)
CONTAINS PRE-PROGRAMMED
UNIQUE ID CODE



	Mon May 08 11:23:42 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON

© UOB-HEP 2011

UOB-HEP
UNIVERSITY OF BRISTOL
HIGH ENERGY PHYSICS GROUP
H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

TITLE fmc_tlu_v1_lib

MODULE: fmc_tlu_toplevel_e

FMC CONNECTOR

AND I2C EEPROM

LICENSED UNDER THE TAPR OPEN HARDWARE LICENSE (WWW.TAPR.ORG/OHL)

A2

MODULE PAGE: 1 OF 7
OVERALL PAGE: 1 OF 29

TOTAL NO. OF SHEETS

HDMI_DUT_1

I1

ENABLE_CONT_FROM_FPGA<0>
CONT_TO_FPGA<0>
CONT_FROM_FPGA<0>

ENABLE_SPARE_FROM_FPGA<0>
SPARE_TO_FPGA<0>
SPARE_FROM_FPGA<0>

ENABLE_TRIG_FROM_FPGA<0>
TRIG_TO_FPGA<0>
TRIG_FROM_FPGA<0>

ENABLE_BUSY_FROM_FPGA<0>
BUSY_TO_FPGA<0>
BUSY_FROM_FPGA<0>

HDMI_CLK_P<0>
HDMI_CLK_N<0>

HDMI_POWER_ENABLE<0>

ENABLE_CONT_FROM_FPGA
CONT_TO_FPGA
CONT_FROM_FPGA

ENABLE_SPARE_FROM_FPGA
SPARE_TO_FPGA
SPARE_FROM_FPGA

ENABLE_TRIG_FROM_FPGA
TRIG_TO_FPGA
TRIG_FROM_FPGA

ENABLE_BUSY_FROM_FPGA
BUSY_TO_FPGA
BUSY_FROM_FPGA

HDMI_CLK
HDMI_CLK*

HDMI_POWER_ENABLE

FMC_TLU_HDMI_DUT_CONNECTOR

HDMI_DUT_2

I2

ENABLE_CONT_FROM_FPGA<1>
CONT_TO_FPGA<1>
CONT_FROM_FPGA<1>

ENABLE_SPARE_FROM_FPGA<1>
SPARE_TO_FPGA<1>
SPARE_FROM_FPGA<1>

ENABLE_TRIG_FROM_FPGA<1>
TRIG_TO_FPGA<1>
TRIG_FROM_FPGA<1>

ENABLE_BUSY_FROM_FPGA<1>
BUSY_TO_FPGA<1>
BUSY_FROM_FPGA<1>

HDMI_CLK_P<1>
HDMI_CLK_N<1>

HDMI_POWER_ENABLE<1>

ENABLE_CONT_FROM_FPGA
CONT_TO_FPGA
CONT_FROM_FPGA

ENABLE_SPARE_FROM_FPGA
SPARE_TO_FPGA
SPARE_FROM_FPGA

ENABLE_TRIG_FROM_FPGA
TRIG_TO_FPGA
TRIG_FROM_FPGA

ENABLE_BUSY_FROM_FPGA
BUSY_TO_FPGA
BUSY_FROM_FPGA

HDMI_CLK
HDMI_CLK*

HDMI_POWER_ENABLE

FMC_TLU_HDMI_DUT_CONNECTOR

HDMI_DUT_3

I3

ENABLE_CONT_FROM_FPGA<2>
CONT_TO_FPGA<2>
CONT_FROM_FPGA<2>

ENABLE_SPARE_FROM_FPGA<2>
SPARE_TO_FPGA<2>
SPARE_FROM_FPGA<2>

ENABLE_TRIG_FROM_FPGA<2>
TRIG_TO_FPGA<2>
TRIG_FROM_FPGA<2>

ENABLE_BUSY_FROM_FPGA<2>
BUSY_TO_FPGA<2>
BUSY_FROM_FPGA<2>

HDMI_CLK_P<2>
HDMI_CLK_N<2>

HDMI_POWER_ENABLE<2>

ENABLE_CONT_FROM_FPGA
CONT_TO_FPGA
CONT_FROM_FPGA

ENABLE_SPARE_FROM_FPGA
SPARE_TO_FPGA
SPARE_FROM_FPGA

ENABLE_TRIG_FROM_FPGA
TRIG_TO_FPGA
TRIG_FROM_FPGA

ENABLE_BUSY_FROM_FPGA
BUSY_TO_FPGA
BUSY_FROM_FPGA

HDMI_CLK
HDMI_CLK*

HDMI_POWER_ENABLE

FMC_TLU_HDMI_DUT_CONNECTOR

HDMI_DUT_4

I4

ENABLE_CONT_FROM_FPGA<3>
CONT_TO_FPGA<3>
CONT_FROM_FPGA<3>

ENABLE_SPARE_FROM_FPGA<3>
SPARE_TO_FPGA<3>
SPARE_FROM_FPGA<3>

ENABLE_TRIG_FROM_FPGA<3>
TRIG_TO_FPGA<3>
TRIG_FROM_FPGA<3>

ENABLE_BUSY_FROM_FPGA<3>
BUSY_TO_FPGA<3>
BUSY_FROM_FPGA<3>

HDMI_CLK_P<3>
HDMI_CLK_N<3>

HDMI_POWER_ENABLE<3>

ENABLE_CONT_FROM_FPGA
CONT_TO_FPGA
CONT_FROM_FPGA

ENABLE_SPARE_FROM_FPGA
SPARE_TO_FPGA
SPARE_FROM_FPGA

ENABLE_TRIG_FROM_FPGA
TRIG_TO_FPGA
TRIG_FROM_FPGA

ENABLE_BUSY_FROM_FPGA
BUSY_TO_FPGA
BUSY_FROM_FPGA

HDMI_CLK
HDMI_CLK*

HDMI_POWER_ENABLE

FMC_TLU_HDMI_DUT_CONNECTOR

	Thu May 04 13:37:48 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON

© UOB-HEP 20 11

UOB-HEP
UNIVERSITY OF BRISTOL
HIGH ENERGY PHYSICS GROUP

H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

TITLE fmc_tlu_v1_lib

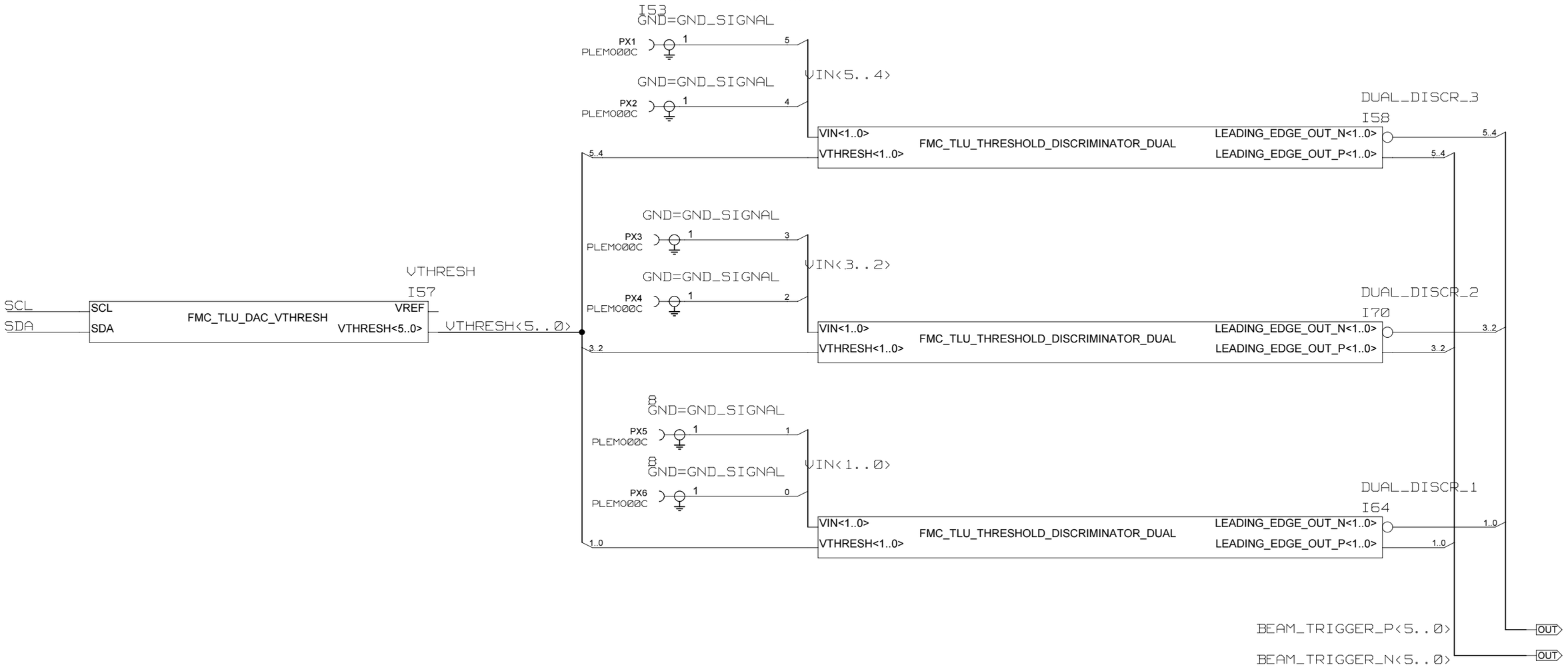
MODULE: fmc_tlu_toplevel_e

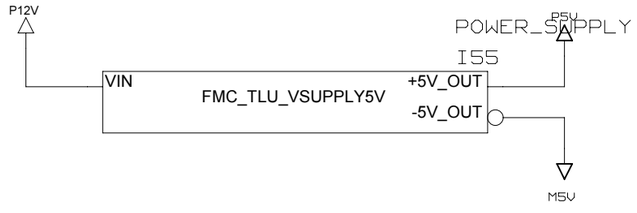
FRONT PANEL DUT CONNECTORS
3 X HDMI (DUT ONLY)
1 X HDMI (DUT OR UPLINK)

LICENSED UNDER THE TAPR OPEN HARDWARE LICENSE (WWW.TAPR.ORG/OHL)

A2

EPK.00.250.NTN





ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS
	Mon Mar 27 17:58:51 2017					

USED ON

© UOB-HEP 20

UOB-HEP
UNIVERSITY OF BRISTOL
HIGH ENERGY PHYSICS GROUP
H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

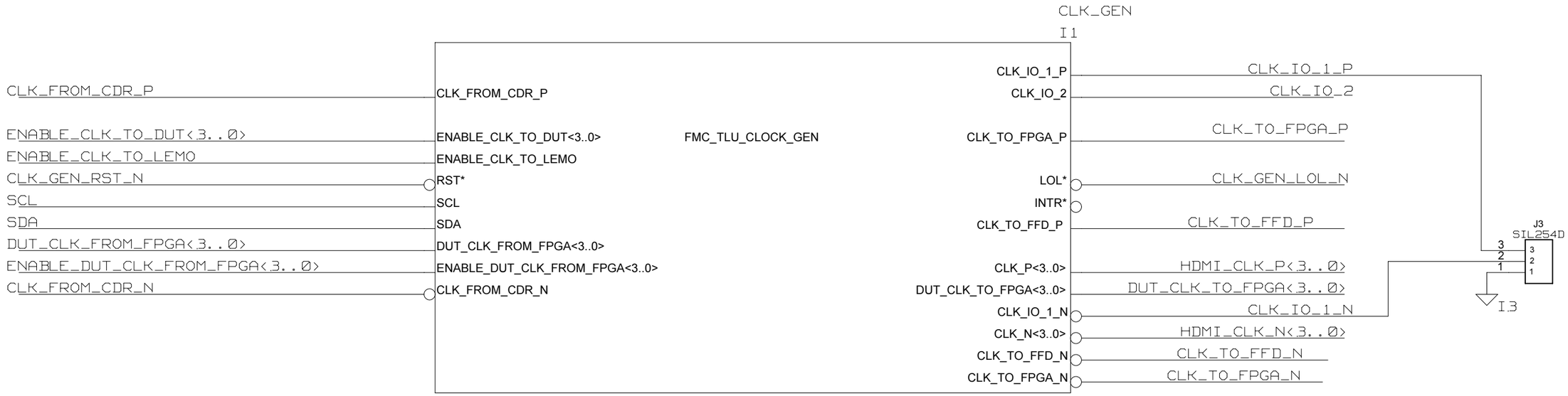
LICENSED UNDER THE TAPR OPEN HARDWARE LICENSE (WWW.TAPR.ORG/OHL)

TITLE fmc_tlu_v1_lib

MODULE: fmc_tlu_toplevel_e

DISCRIMINATORS

A2



	Thu Mar 30 17:10:57 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON

© UOB-HEP 2016

UOB-HEP
UNIVERSITY OF BRISTOL
HIGH ENERGY PHYSICS GROUP

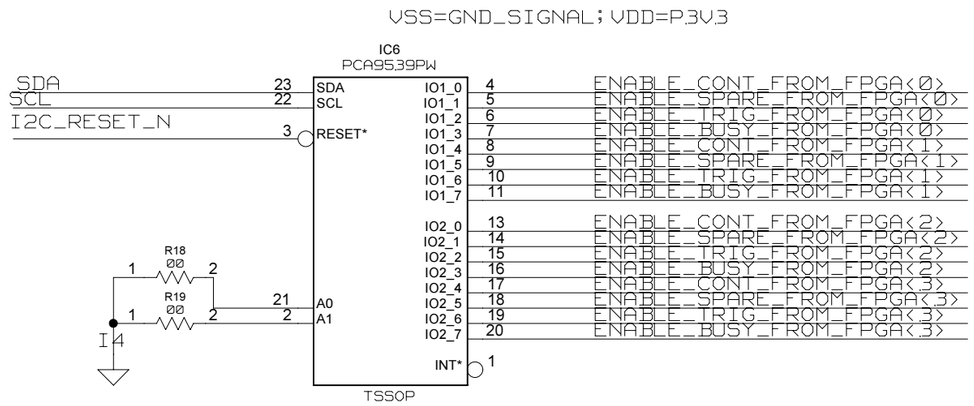
H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

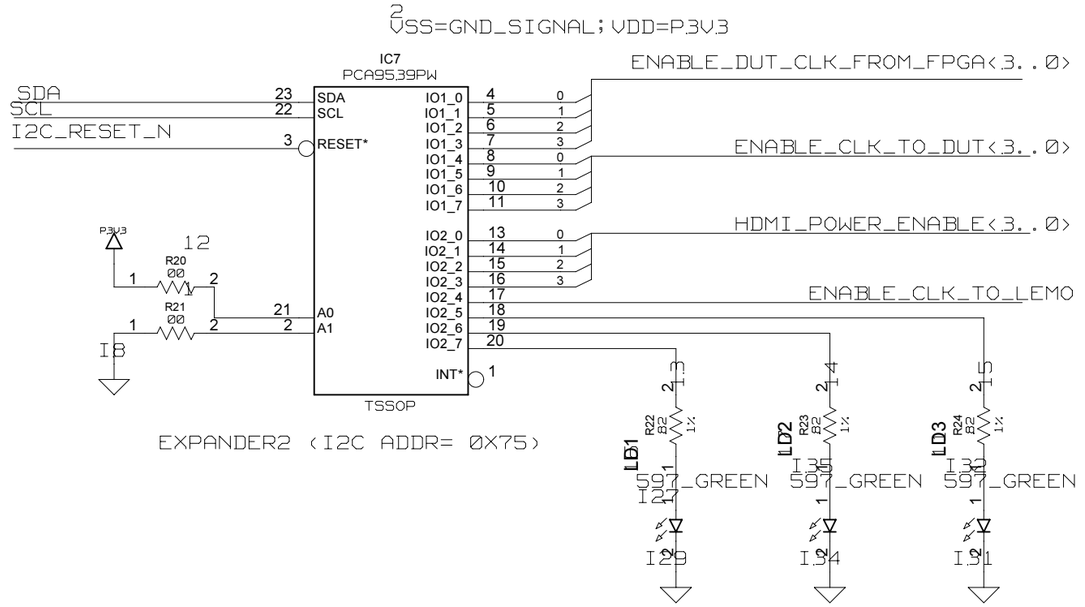
TITLE fmc_tlu_v1_lib CLOCK GENERATION

MODULE: fmc_tlu_toplevel_e

LICENSED UNDER THE TAPR OPEN HARDWARE LICENSE (WWW.TAPR.ORG/OHL)

A2





	Mon Mar 27 17:58:54 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON

© UOB-HEP 20 11

UOB-HEP
UNIVERSITY OF BRISTOL
HIGH ENERGY PHYSICS GROUP
H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

TITLE fmc_tlu_v1_lib

I2C I/O EXTENDERS

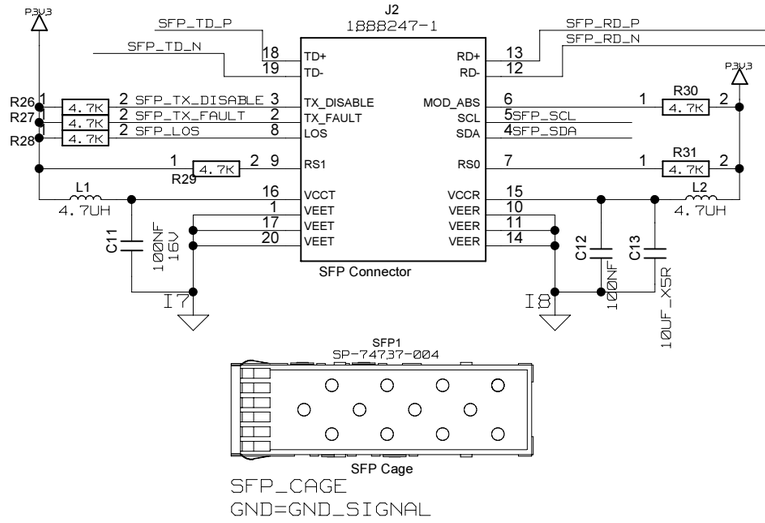
MODULE: fmc_tlu_toplevel_e

LICENSED UNDER THE TAPR OPEN HARDWARE LICENSE (WWW.TAPR.ORG/OHL)

A2

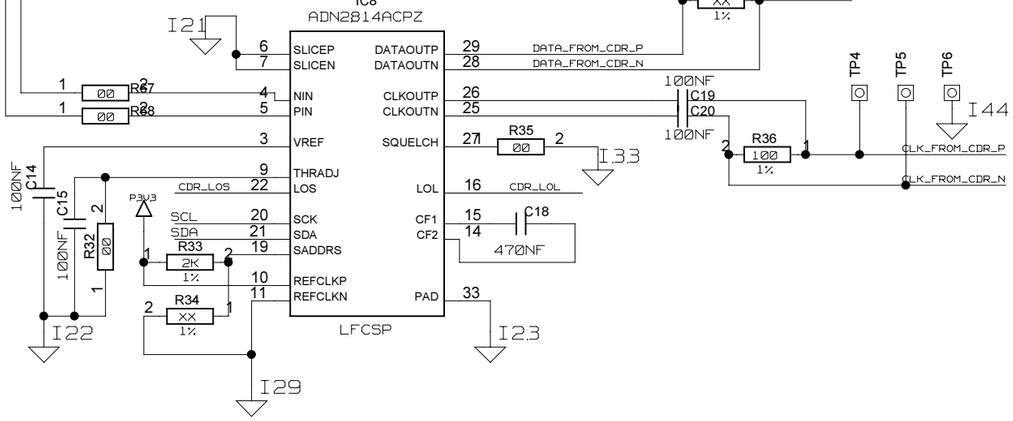
SN65LVDS2 OR SN65LVDT2
SN65LVDT2 HAS TERMINATION.
SN65LVDS2 REQUIRES EXTERNAL TERMINATION.

SFP_CAGE



CDR (I2C ADDR= 0X60)

VEE=GND_SIGNAL; VCC=P3V3



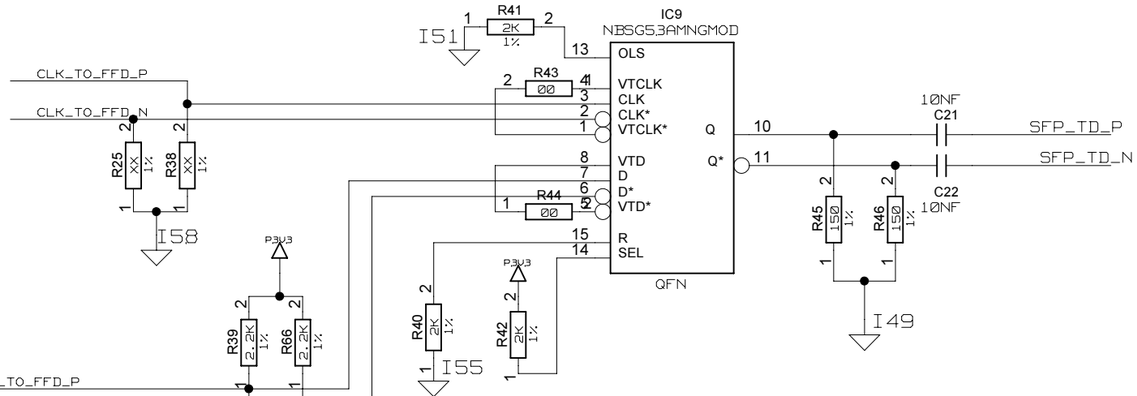
USE TERMINATION IN FPGA IF POSSIBLE

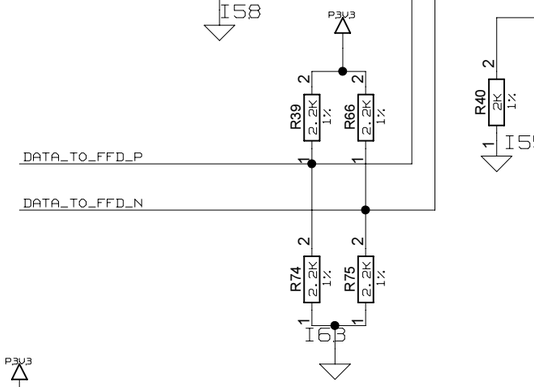
( )

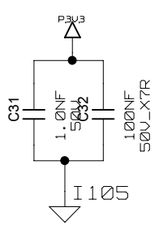
(GND_SIGNAL: 17; VEE: 12; VCC: 9, 16)

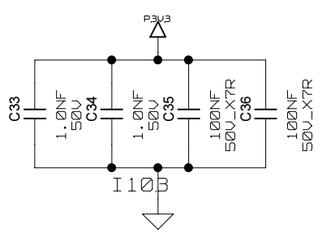
VEE=GND_SIGNAL; VCC=P3V3

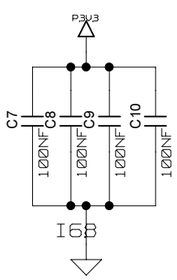
MAKE SURE THE FOOTPRINT FOR THIS IS CORRECT!

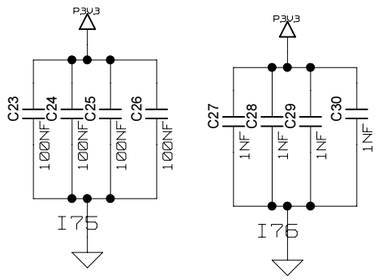












	Fri May 05 14:40:28 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON

© UOB-HEP 20

UOB-HEP
UNIVERSITY OF BRISTOL
HIGH ENERGY PHYSICS GROUP
H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

TITLE fmc_tlu_v1_lib

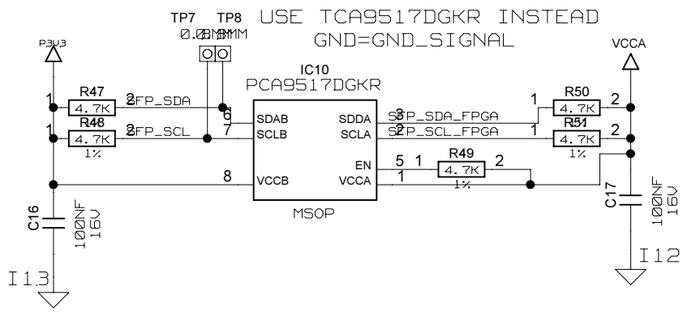
MODULE: fmc_tlu_toplevel_e

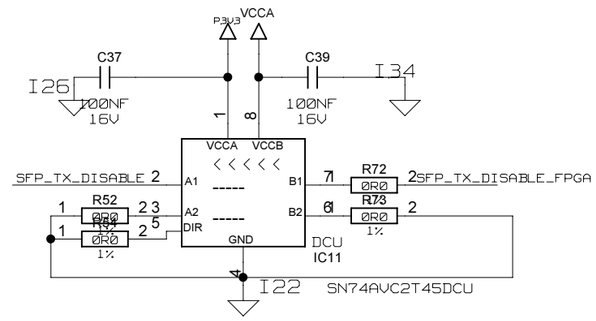
SFP INTERFACE

A2

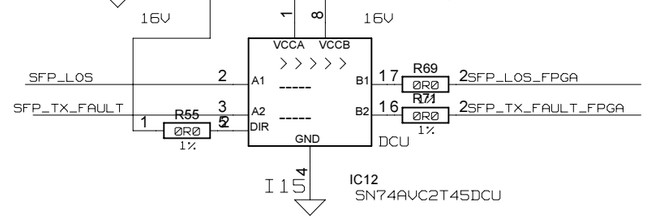
MODULE PAGE: 6 OF 7
OVERALL PAGE: 6 OF 29

TOTAL NO. OF SHEETS





DIR LOW : B -> A
DIR HIGH: A -> B



	Thu Mar 30 17:11:07 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON

© UOB-HEP 20

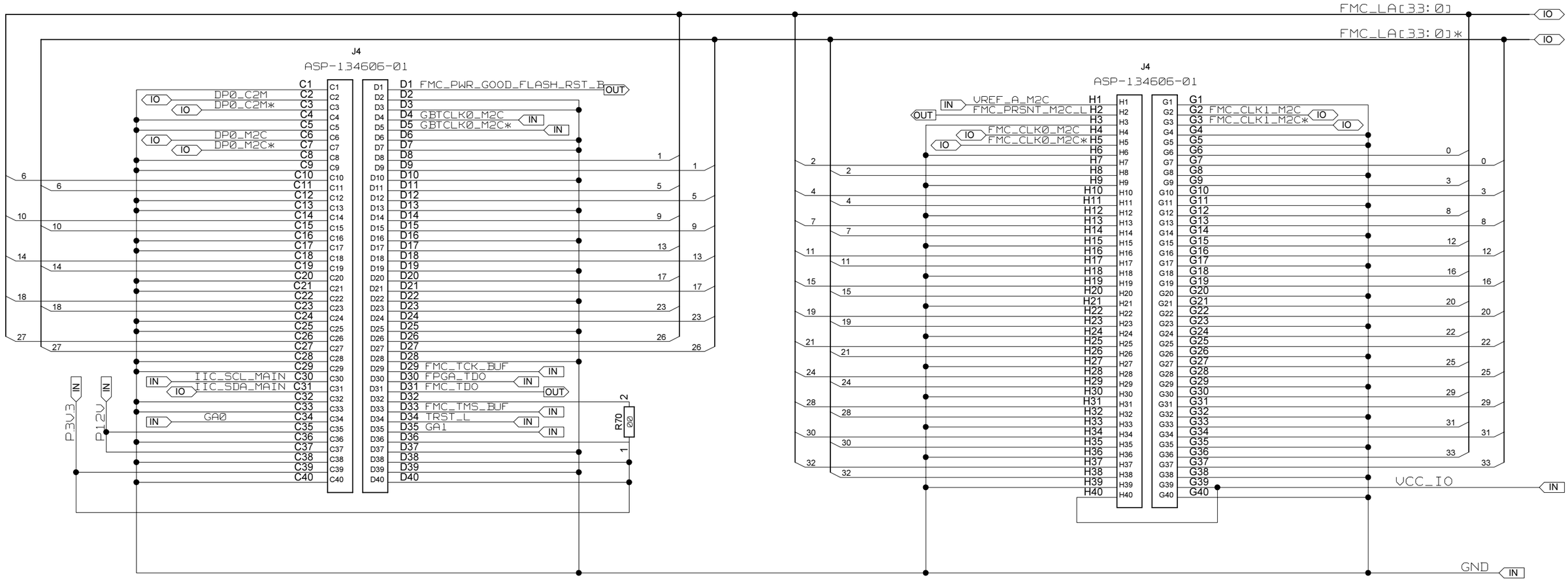
UOB-HEP
UNIVERSITY OF BRISTOL
HIGH ENERGY PHYSICS GROUP
H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

TITLE fmc_tlu_v1_lib

MODULE: fmc_tlu_toplevel_e

LEVEL TRANSLATORS

A2



	Thu Mar 30 11:19:40 2017					
			D. CUSSANS	C. JESKE	D. CUSSANS	
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON

© UOB-HEP 20 10

UOB-HEP
UNIVERSITY OF BRISTOL
HIGH ENERGY PHYSICS GROUP
H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

LICENSED UNDER THE TAPR OPEN HARDWARE LICENSE (WWW.TAPR.ORG/OHL)

TITLE fmc_tlu_v1_lib

MODULE: pc036a_fmc_lpc_connector

FMC LPC

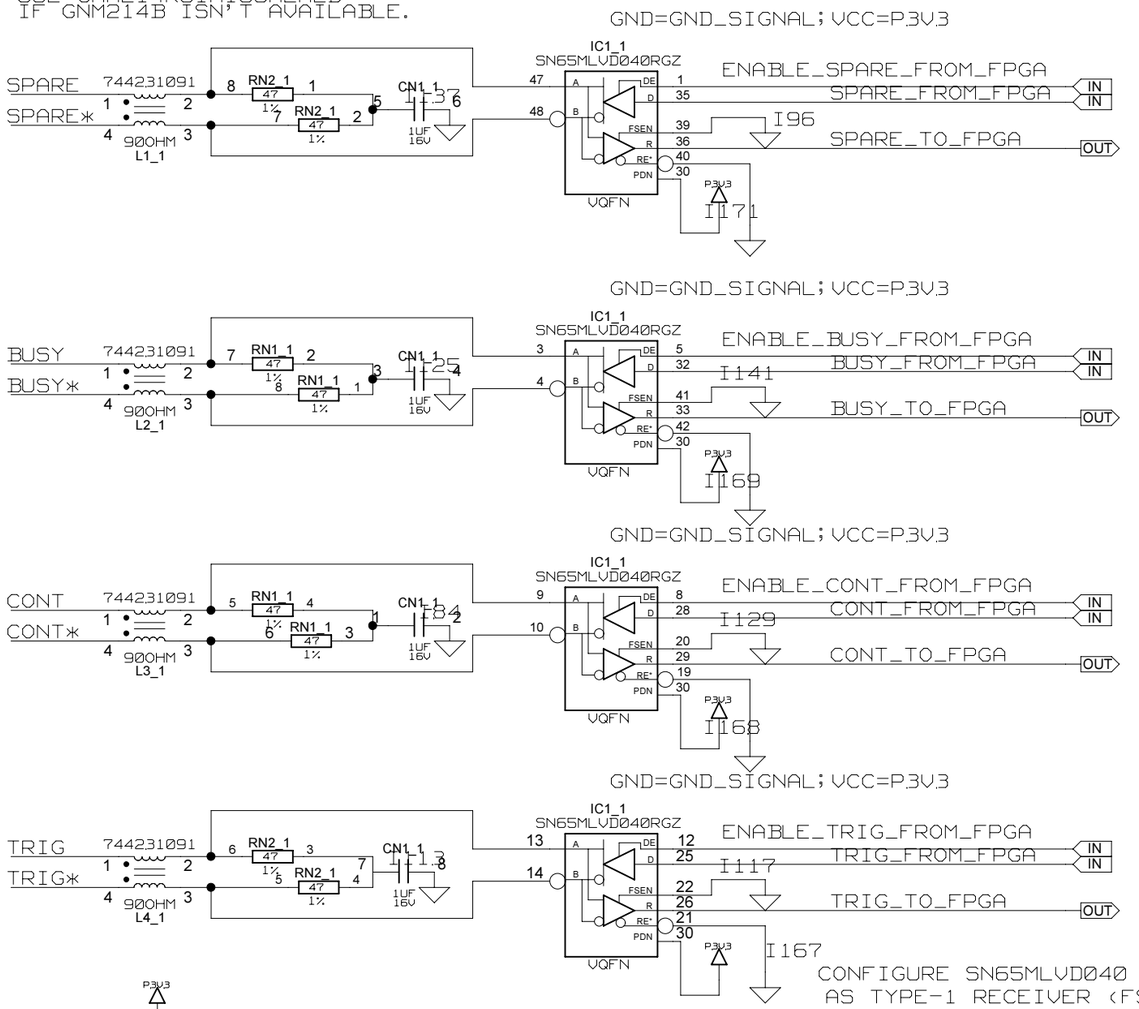
A2

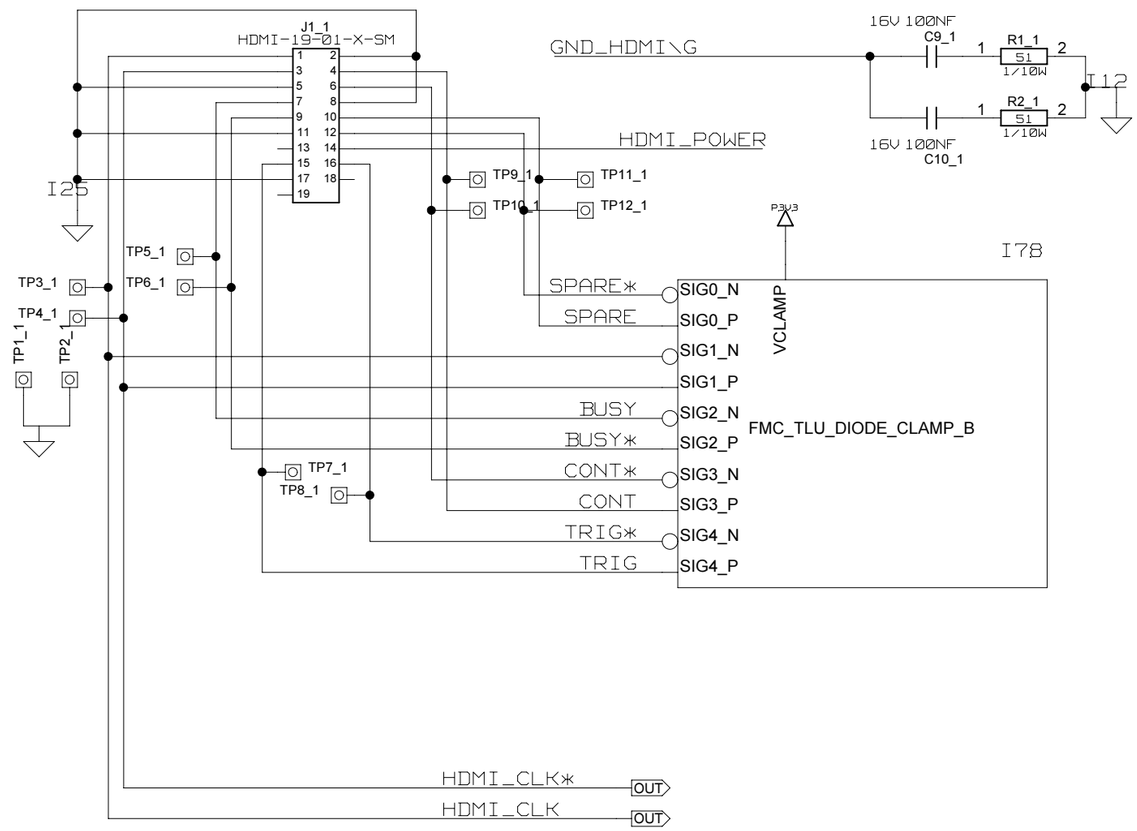
MODULE PAGE: 1 OF 1
OVERALL PAGE: 8 OF 29

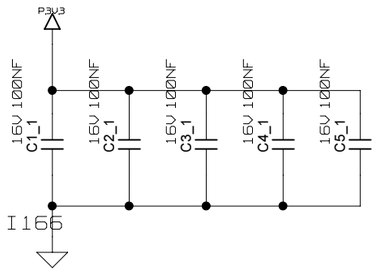
TOTAL NO. OF SHEETS

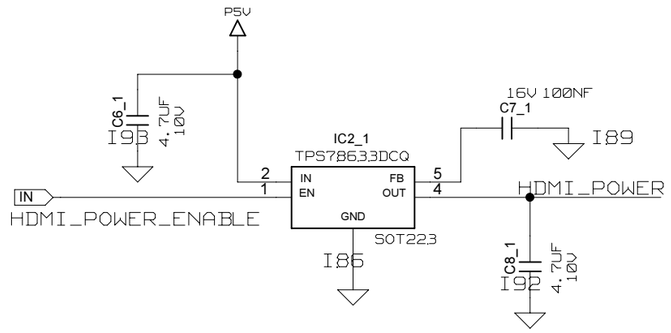
USE GNM214R61A105MEA2D
IF GNM214B ISN'T AVAILABLE.

REPLACE SAMTEC CONNECTOR WITH MOLEX 47151-0002









	Thu Apr 13 16:21:16 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON

© UOB-HEP 20 11

UOB-HEP
UNIVERSITY OF BRISTOL
HIGH ENERGY PHYSICS GROUP
H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

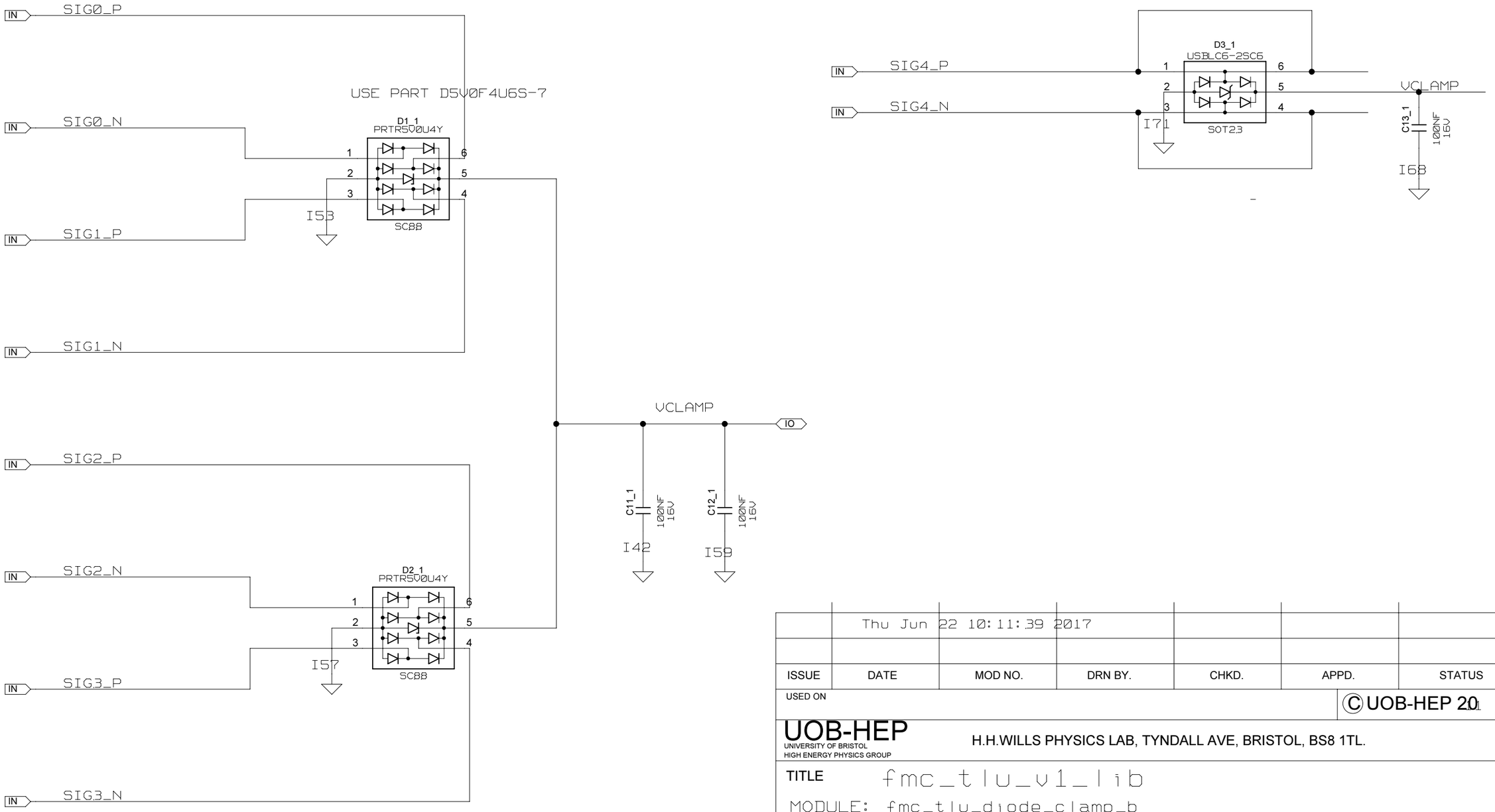
TITLE fmc_tlu_v1_lib

HDMI FRONT PANEL CONNECTOR

MODULE: fmc_tlu_hdmi_dut_connector

LICENSED UNDER THE TAPR OPEN HARDWARE LICENSE (WWW.TAPR.ORG/OHL)

A2



	Thu Jun 22 10:11:39 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON

© UOB-HEP 2017

UOB-HEP
UNIVERSITY OF BRISTOL
HIGH ENERGY PHYSICS GROUP
H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

TITLE fmc_tlu_v1_lib

MODULE: fmc_tlu_diode_clamp_b

LICENSED UNDER THE TAPR OPEN HARDWARE LICENSE (WWW.TAPR.ORG/OHL)

A2

USE GNM214R61A105MEA2D
IF GNM214B ISN'T AVAILABLE.

GND=GND_SIGNAL; VCC=P3V3

SPARE
SPARE*
744231091
900OHM
L1_2
RN2_2
RN1_2
47
1%
CN1_2
1UF
16V
IC1_2
SN65MLVD040RGZ
VQFN
ENABLE_SPARE_FROM_FPGA
SPARE_FROM_FPGA
SPARE_TO_FPGA
IN
OUT
I96
I171

GND=GND_SIGNAL; VCC=P3V3

BUSY
BUSY*
L2_2
I125
I141
ENABLE_BUSY_FROM_FPGA
BUSY_FROM_FPGA
BUSY_TO_FPGA
I169

GND=GND_SIGNAL; VCC=P3V3

CONT
CONT*
L3_2
I84
I129
ENABLE_CONT_FROM_FPGA
CONT_FROM_FPGA
CONT_TO_FPGA
I168

GND=GND_SIGNAL; VCC=P3V3

TRIG
TRIG*
L4_2
ENABLE_TRIG_FROM_FPGA
TRIG_FROM_FPGA
TRIG_TO_FPGA
I117
I167

CONFIGURE SN65MLVD040
AS TYPE-1 RECEIVER (FSEN LOW)

P3V3
16V 100NF
C1_2
C2_2
C3_2
C4_2
C5_2
I166

P5V
C6_2
4.7UF
10V
I93
IC2_2
TPS78633DCQ
SOT223
IN
EN
FB
OUT
GND
HDMI_POWER_ENABLE
C7_2
I89
HDMI_POWER
I86
C8_2
I91

REPLACE SAMTEC CONNECTOR WITH MOLEX 47151-0002

GND=GND_HDMI

J1_2
HDMI-19-01-X-SM
GND_HDMI\G
I25
HDMI_POWER
C9_2
C10_2
R1_2
R2_2
51
1/10W
I12
TP1_2
TP2_2
TP3_2
TP4_2
TP5_2
TP6_2
TP7_2
TP8_2
TP9_2
TP10_2
TP11_2
TP12_2
I78
FMC_TLU_DIODE_CLAMP_B
VCLAMP
SPARE*
SPARE
BUSY
BUSY*
CONT*
CONT
TRIG*
TRIG
SIG0_N
SIG0_P
SIG1_N
SIG1_P
SIG2_N
SIG2_P
SIG3_N
SIG3_P
SIG4_N
SIG4_P
HDMI_CLK*
HDMI_CLK
OUT

ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS
	Thu Apr 13 16:21:16 2017					

USED ON

© UOB-HEP 20 11

UOB-HEP
UNIVERSITY OF BRISTOL
HIGH ENERGY PHYSICS GROUP
H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

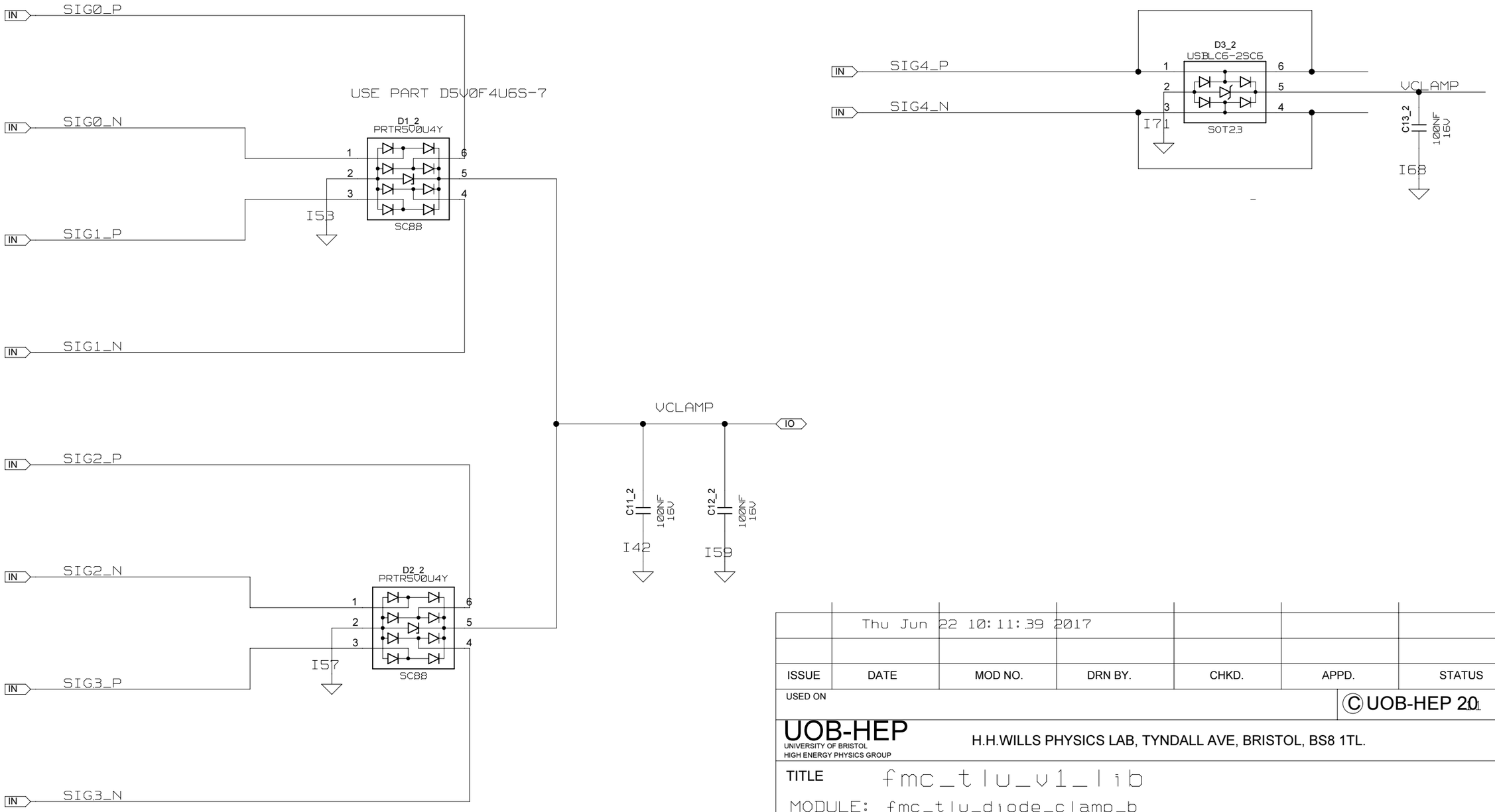
TITLE fmc_tlu_v1_lib

HDMI FRONT PANEL CONNECTOR

MODULE: fmc_tlu_hdmi_dut_connector

LICENSED UNDER THE TAPR OPEN HARDWARE LICENSE (WWW.TAPR.ORG/OHL)

A2



	Thu Jun 22 10:11:39 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON

© UOB-HEP 2011

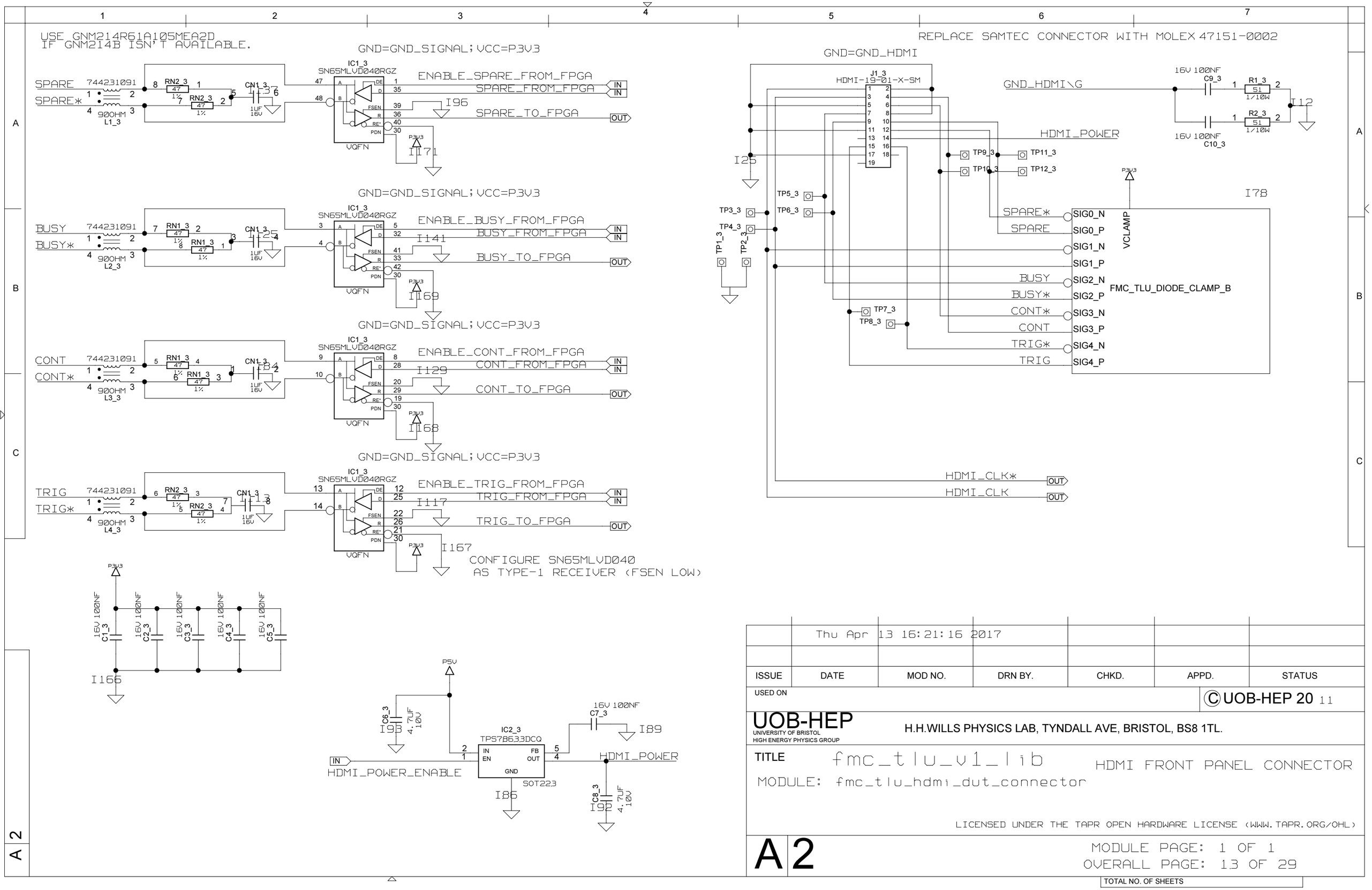
UOB-HEP
UNIVERSITY OF BRISTOL
HIGH ENERGY PHYSICS GROUP
H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

TITLE fmc_tlu_v1_lib

MODULE: fmc_tlu_diode_clamp_b

LICENSED UNDER THE TAPR OPEN HARDWARE LICENSE (WWW.TAPR.ORG/OHL)

A2



	Thu Apr 13 16:21:16 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON

© UOB-HEP 20 11

UOB-HEP
UNIVERSITY OF BRISTOL
HIGH ENERGY PHYSICS GROUP

H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

TITLE fmc_tlu_v1_lib HDMI FRONT PANEL CONNECTOR

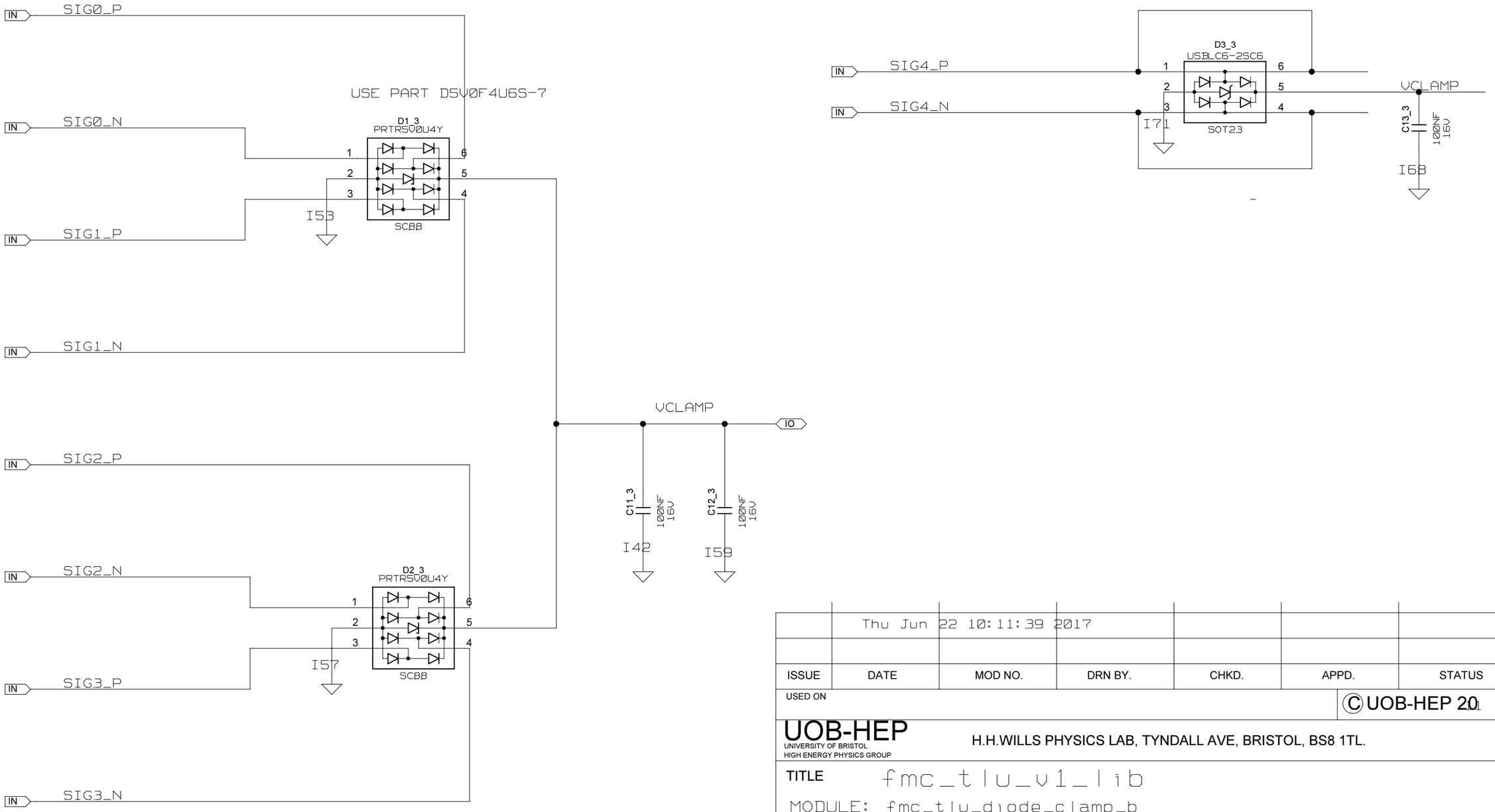
MODULE: fmc_tlu_hdmi_dut_connector

LICENSED UNDER THE TAPR OPEN HARDWARE LICENSE (WWW.TAPR.ORG/OHL)

A2

MODULE PAGE: 1 OF 1
OVERALL PAGE: 13 OF 29

TOTAL NO. OF SHEETS



	Thu Jun 22 10:11:39 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON

© UOB-HEP 2011

UOB-HEP
UNIVERSITY OF BRISTOL
HIGH ENERGY PHYSICS GROUP
H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

TITLE fmc_tlu_v1_lib

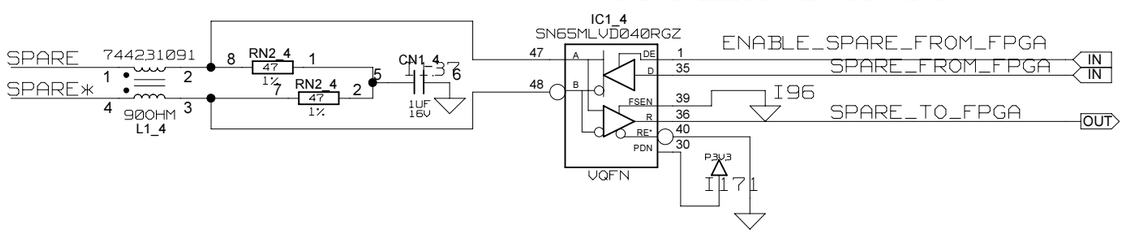
MODULE: fmc_tlu_diode_clamp_b

LICENSED UNDER THE TAPR OPEN HARDWARE LICENSE (WWW.TAPR.ORG/OHL)

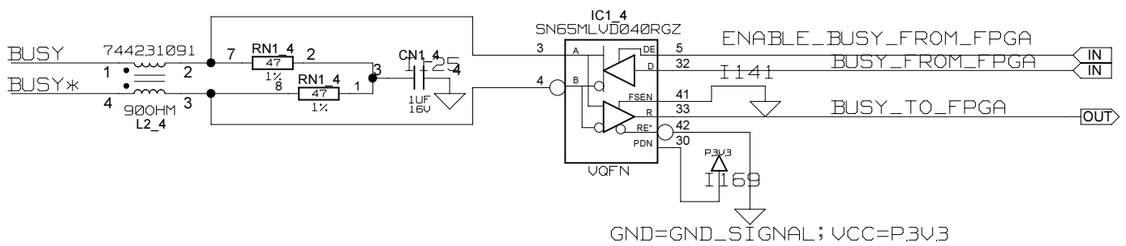
A2

USE GNM214R61A105MEA2D
IF GNM214B ISN'T AVAILABLE.

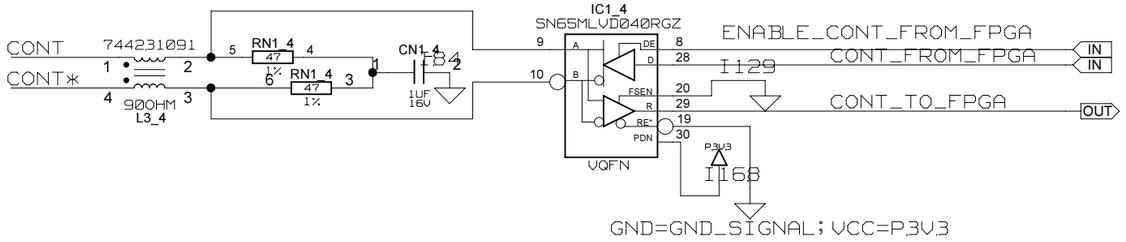
GND=GND_SIGNAL; VCC=P3V3



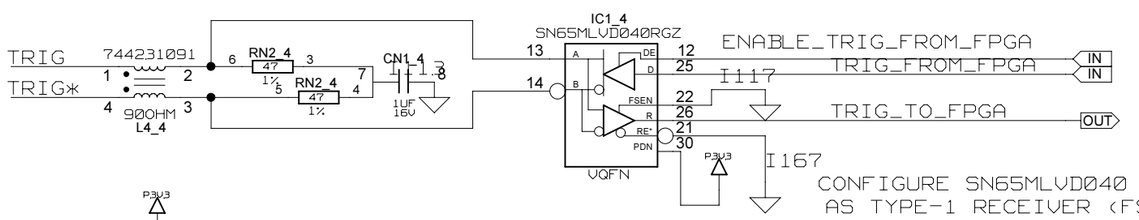
GND=GND_SIGNAL; VCC=P3V3



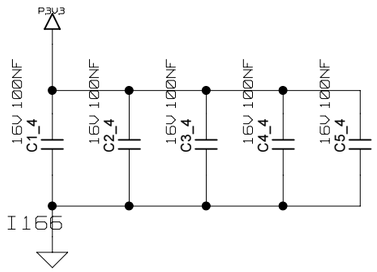
GND=GND_SIGNAL; VCC=P3V3

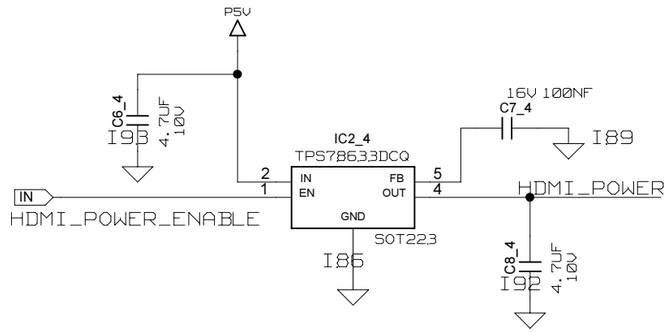


GND=GND_SIGNAL; VCC=P3V3



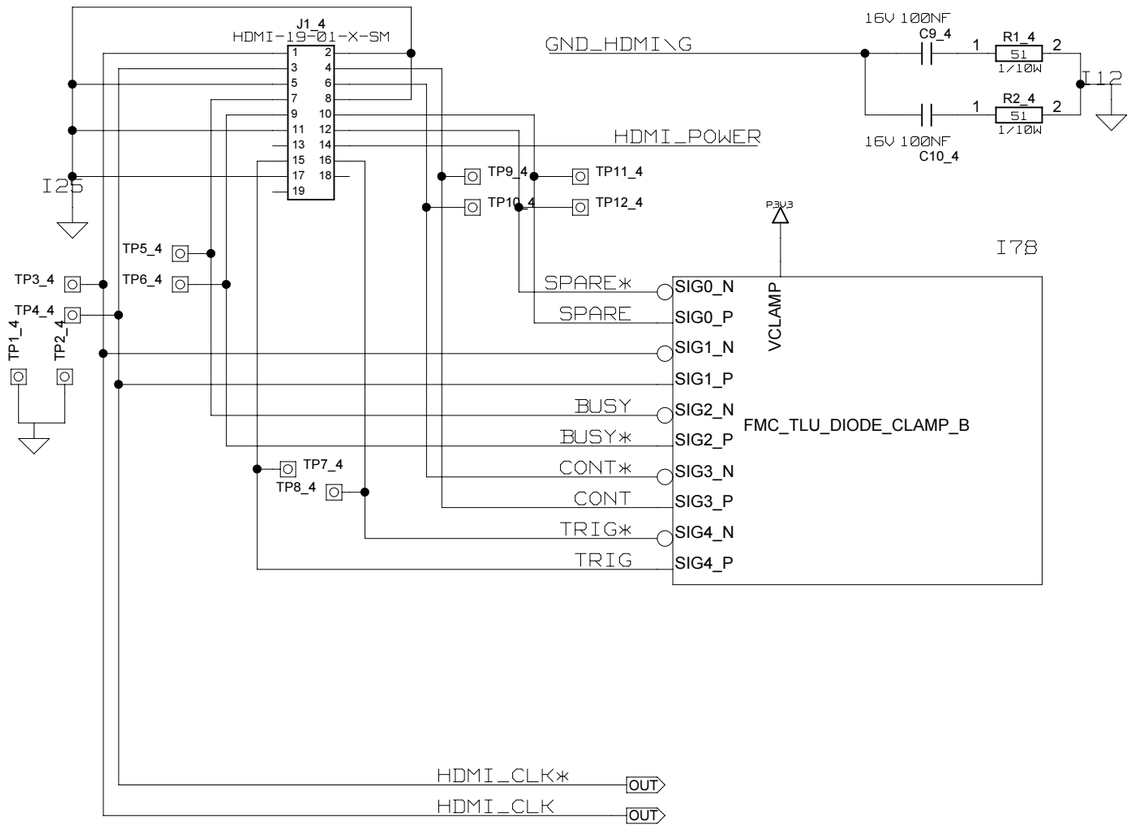
CONFIGURE SN65MLVD040
AS TYPE-1 RECEIVER (FSEN LOW)





REPLACE SAMTEC CONNECTOR WITH MOLEX 47151-0002

GND=GND_HDMI



	Thu Apr 13 16:21:16 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON

© UOB-HEP 20 11

UOB-HEP
UNIVERSITY OF BRISTOL
HIGH ENERGY PHYSICS GROUP

H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

TITLE fmc_tlu_v1_lib

HDMI FRONT PANEL CONNECTOR

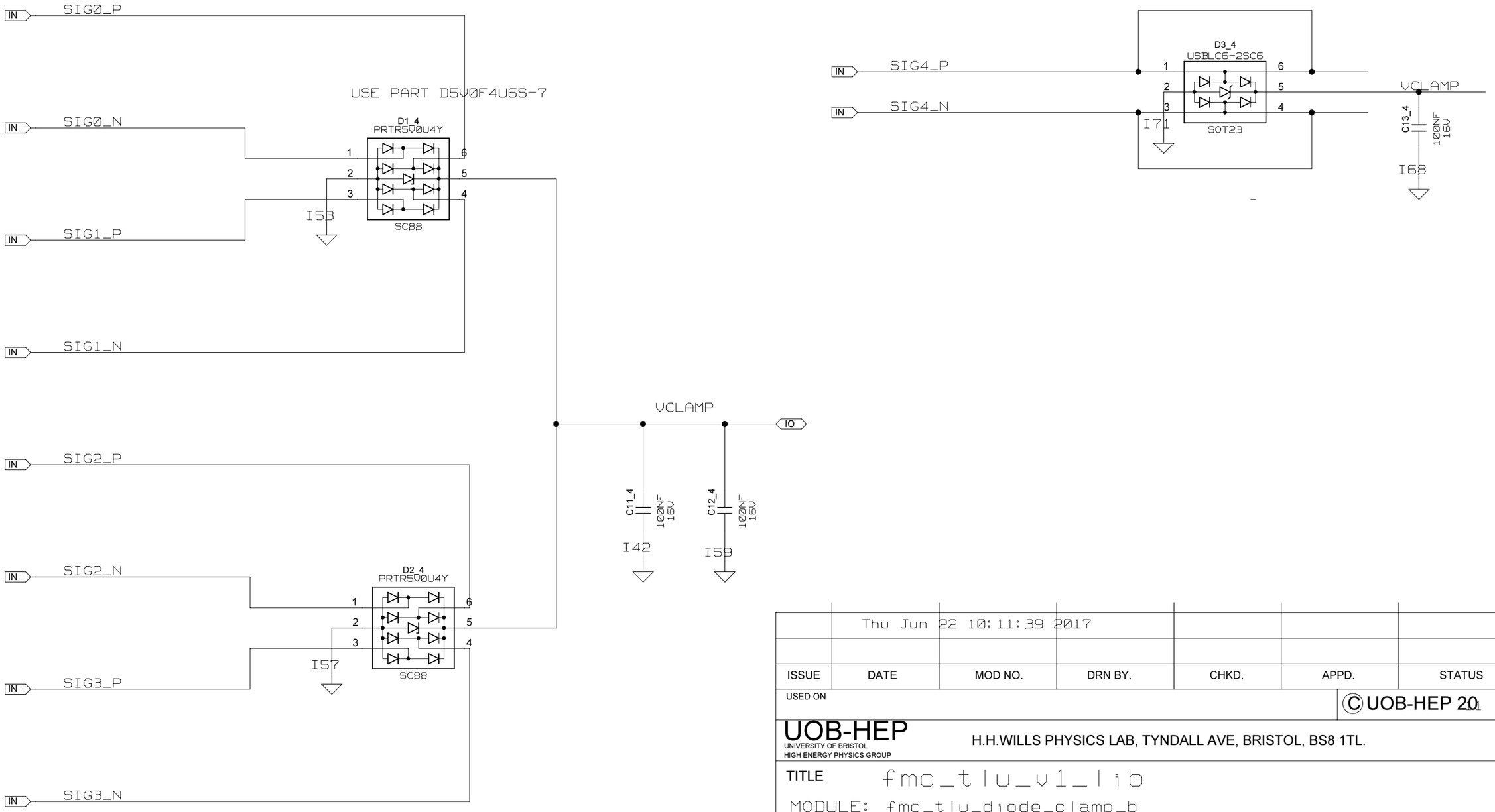
MODULE: fmc_tlu_hdmi_dut_connector

LICENSED UNDER THE TAPR OPEN HARDWARE LICENSE (WWW.TAPR.ORG/OHL)

A2

MODULE PAGE: 1 OF 1
OVERALL PAGE: 15 OF 29

TOTAL NO. OF SHEETS



	Thu Jun 22 10:11:39 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON

© UOB-HEP 2011

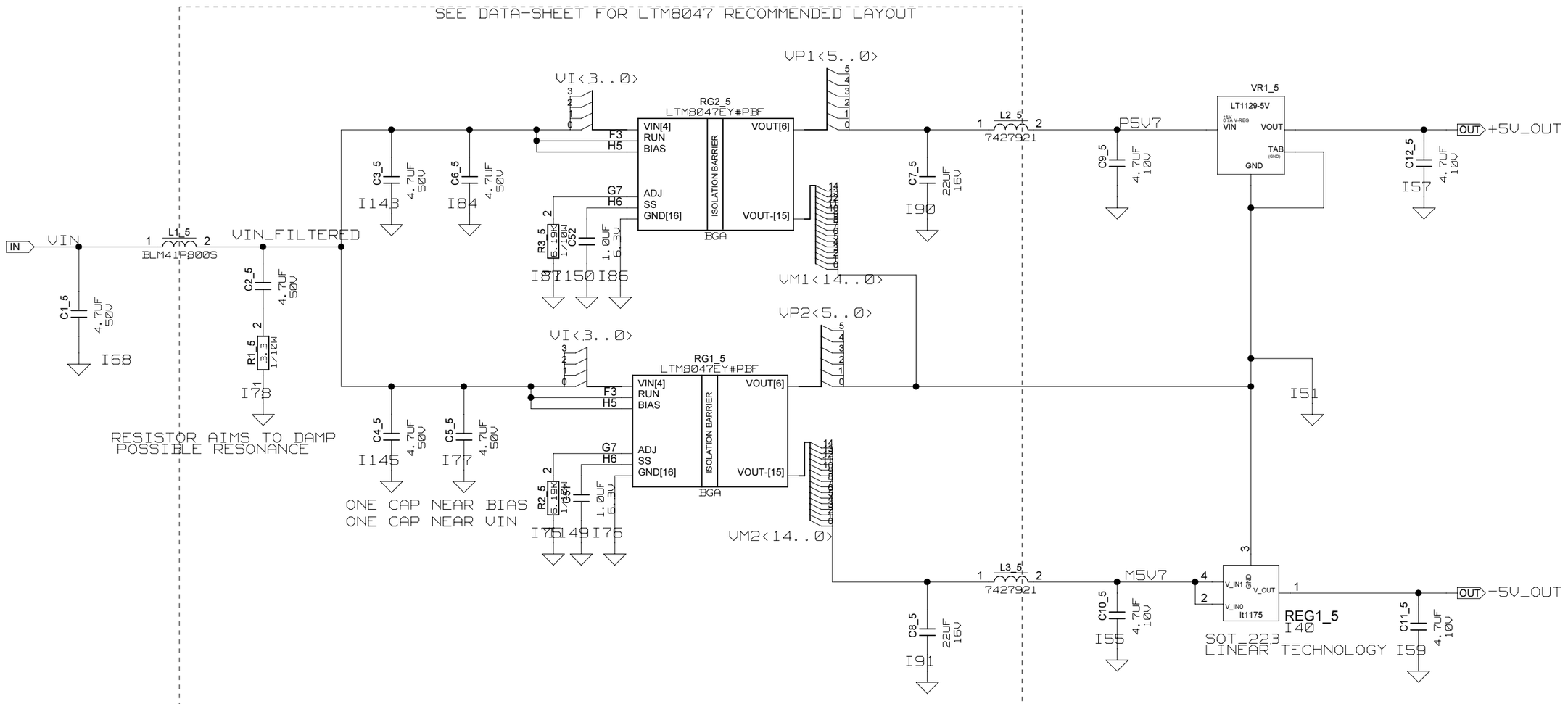
UOB-HEP
UNIVERSITY OF BRISTOL
HIGH ENERGY PHYSICS GROUP
H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

TITLE fmc_tlu_v1_lib

MODULE: fmc_tlu_diode_clamp_b

LICENSED UNDER THE TAPR OPEN HARDWARE LICENSE (WWW.TAPR.ORG/OHL)

A2



	Fri May 05 14:39:22 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON

© UOB-HEP 20

UOB-HEP
UNIVERSITY OF BRISTOL
HIGH ENERGY PHYSICS GROUP
H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

TITLE fmc_tlu_v1_lib

MODULE: fmc_tlu_vsupply5v

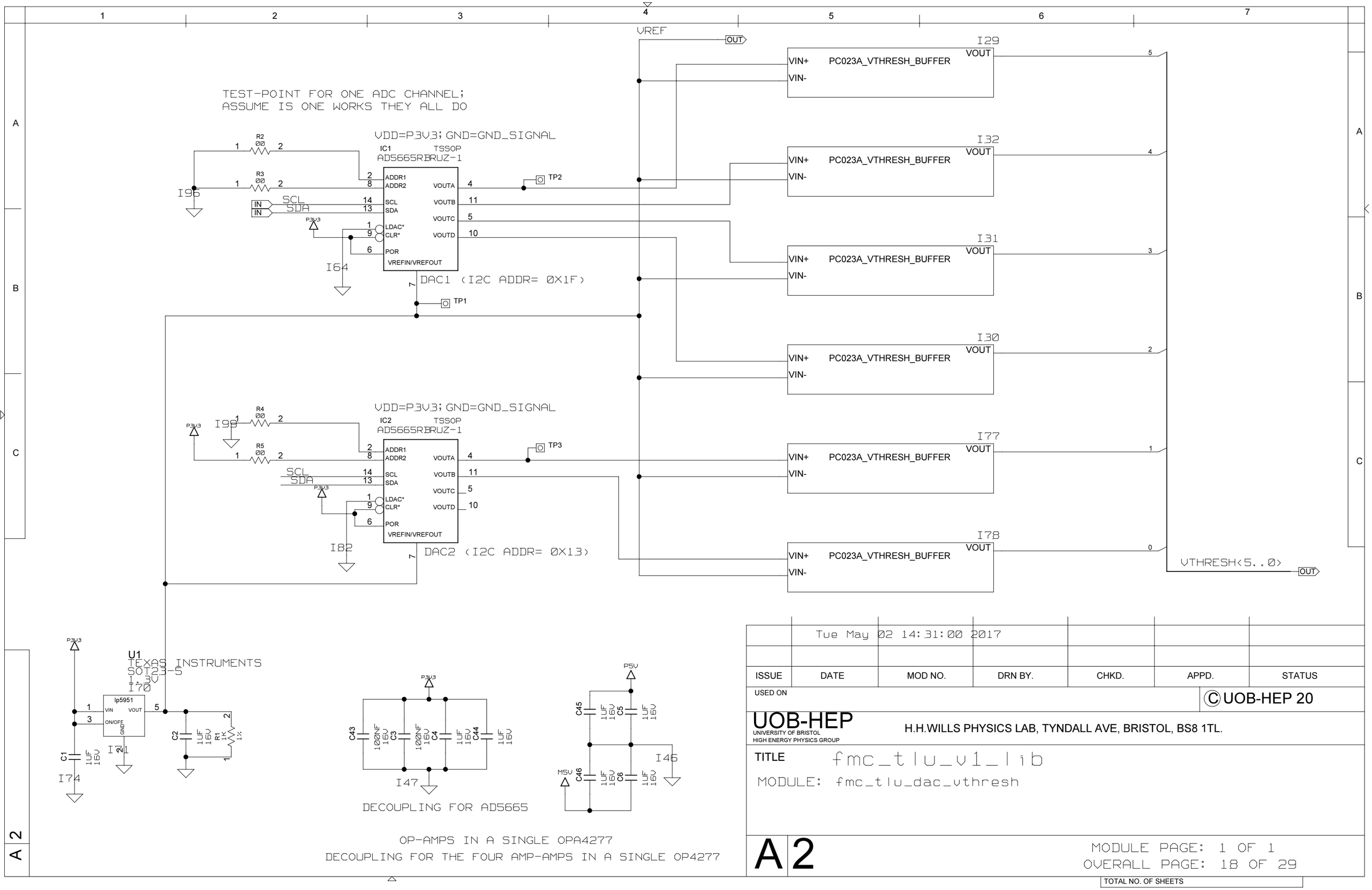
SUPPLY_DIGITAL

OVERALL PAGE: 17 OF 29

A2

MODULE PAGE: 1 OF 1

TOTAL NO. OF SHEETS



	Tue May 02 14:31:00 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON

© UOB-HEP 20

UOB-HEP
UNIVERSITY OF BRISTOL
HIGH ENERGY PHYSICS GROUP

H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

TITLE fmc_tlu_v1_lib

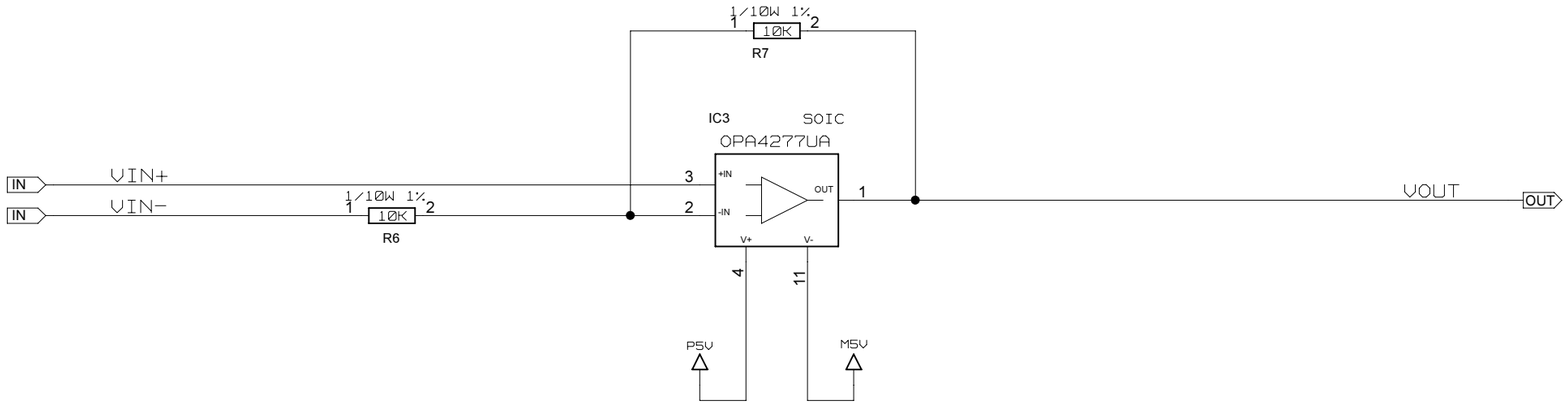
MODULE: fmc_tlu_dac_vthresh

A 2

MODULE PAGE: 1 OF 1
OVERALL PAGE: 18 OF 29

TOTAL NO. OF SHEETS

INVERTING BUFFER WITH X-1 GAIN



	Mon Mar 27 17:58:27 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON

© UOB-HEP 20

UOB-HEP
UNIVERSITY OF BRISTOL
HIGH ENERGY PHYSICS GROUP
H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

TITLE fmc_tlu_v1_lib

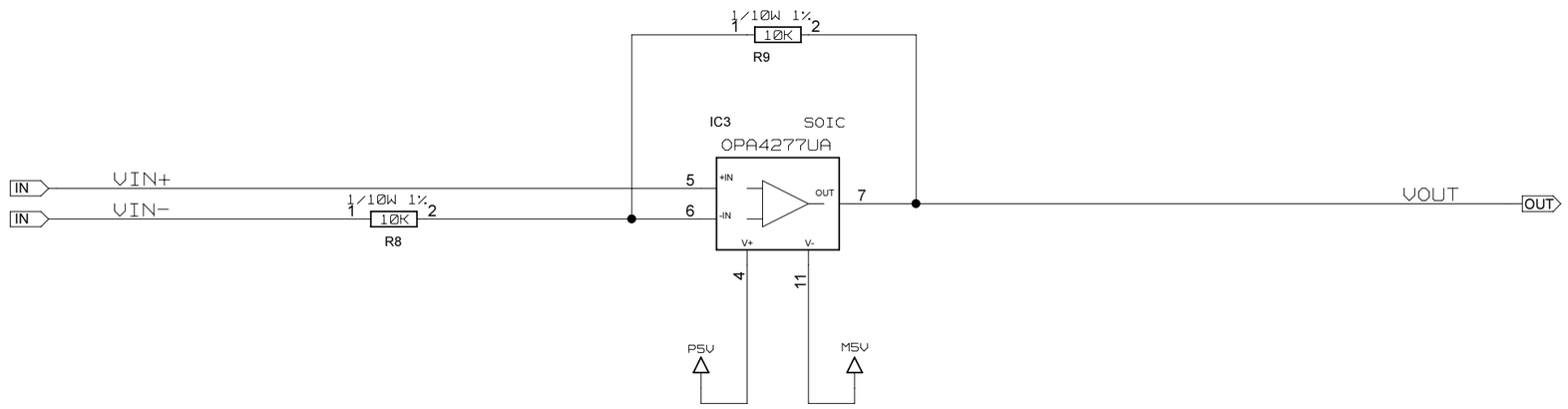
MODULE: pc023a_vthresh_buffer

A2

MODULE PAGE: 1 OF 1
OVERALL PAGE: 19 OF 29

TOTAL NO. OF SHEETS

INVERTING BUFFER WITH X-1 GAIN



	Mon Mar 27 17:58:27 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON

© UOB-HEP 20

UOB-HEP
UNIVERSITY OF BRISTOL
HIGH ENERGY PHYSICS GROUP
H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

TITLE fmc_tlu_v1_lib

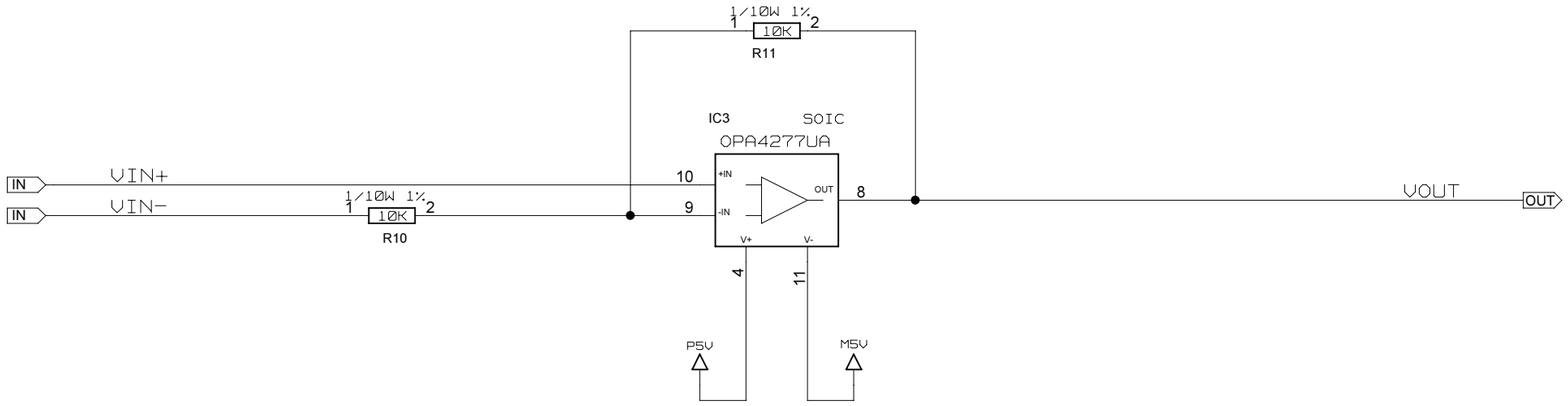
MODULE: pc023a_vthresh_buffer

A2

MODULE PAGE: 1 OF 1
OVERALL PAGE: 20 OF 29

TOTAL NO. OF SHEETS

INVERTING BUFFER WITH X-1 GAIN



	Mon Mar 27 17:58:27 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON

© UOB-HEP 20

UOB-HEP
UNIVERSITY OF BRISTOL
HIGH ENERGY PHYSICS GROUP
H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

TITLE fmc_tlu_v1_lib

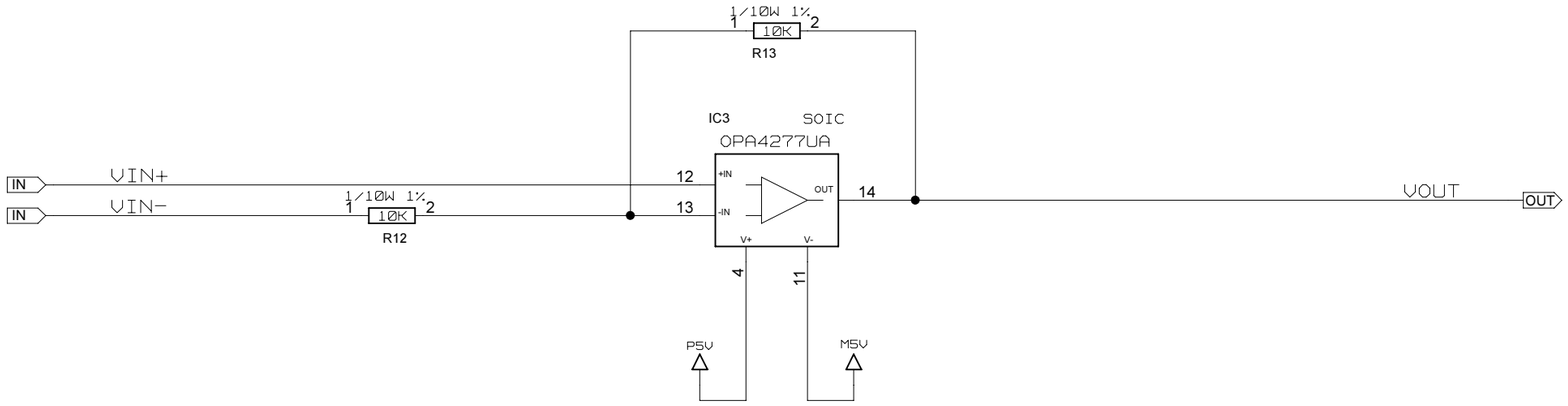
MODULE: pc023a_vthresh_buffer

A2

MODULE PAGE: 1 OF 1
OVERALL PAGE: 21 OF 29

TOTAL NO. OF SHEETS

INVERTING BUFFER WITH X-1 GAIN



	Mon Mar 27 17:58:27 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON

© UOB-HEP 20

UOB-HEP
UNIVERSITY OF BRISTOL
HIGH ENERGY PHYSICS GROUP
H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

TITLE fmc_tlu_v1_lib

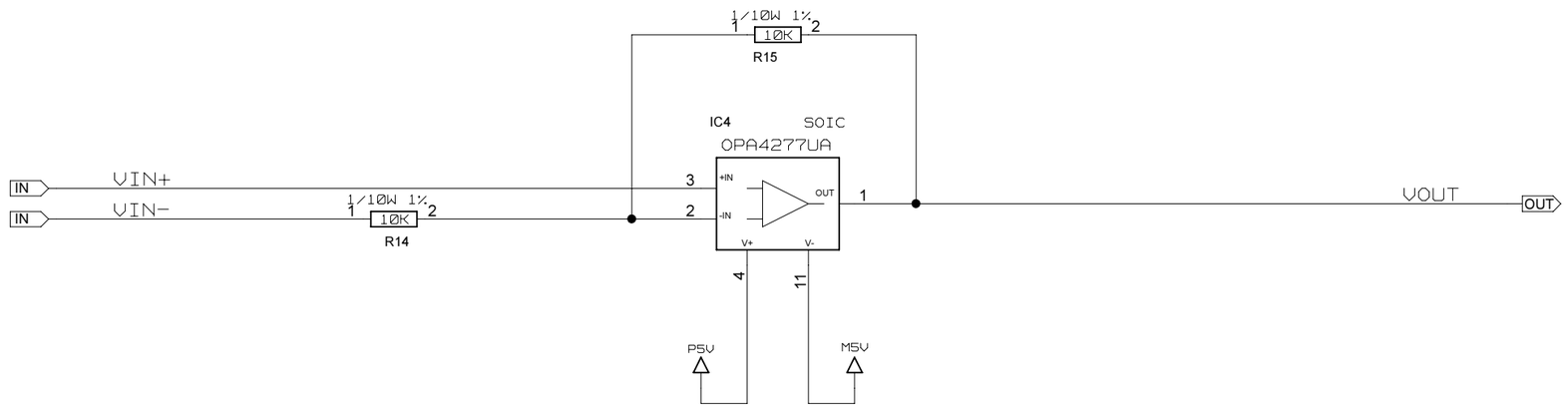
MODULE: pc023a_vthresh_buffer

A2

MODULE PAGE: 1 OF 1
OVERALL PAGE: 22 OF 29

TOTAL NO. OF SHEETS

INVERTING BUFFER WITH X-1 GAIN



	Mon Mar 27 17:58:27 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON

© UOB-HEP 20

UOB-HEP
UNIVERSITY OF BRISTOL
HIGH ENERGY PHYSICS GROUP
H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

TITLE fmc_tlu_v1_lib

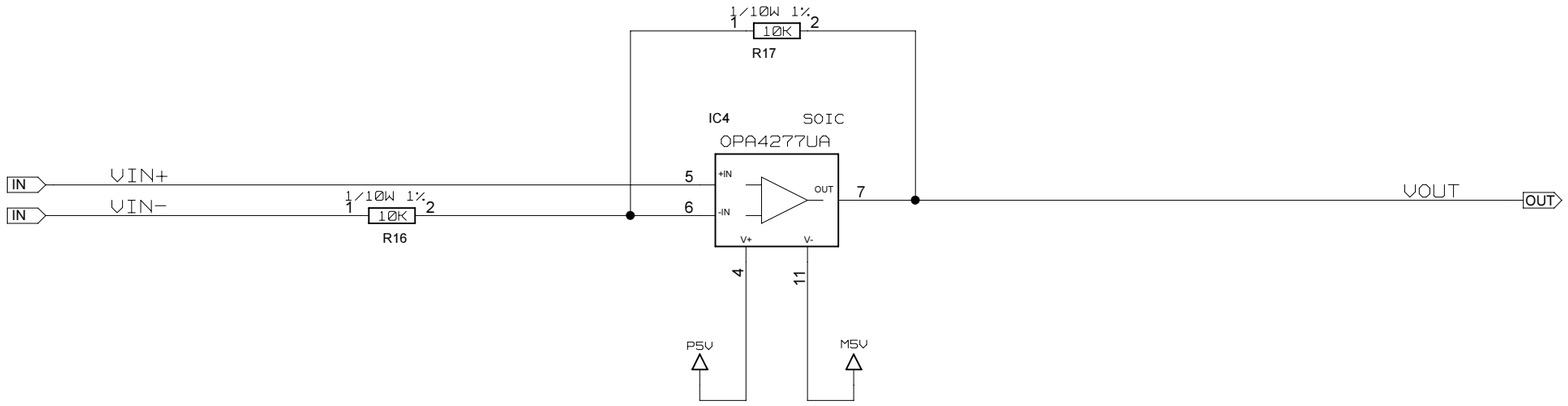
MODULE: pc023a_vthresh_buffer

A2

MODULE PAGE: 1 OF 1
OVERALL PAGE: 23 OF 29

TOTAL NO. OF SHEETS

INVERTING BUFFER WITH X-1 GAIN



	Mon Mar 27 17:58:27 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON

© UOB-HEP 20

UOB-HEP
UNIVERSITY OF BRISTOL
HIGH ENERGY PHYSICS GROUP

H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

TITLE fmc_tlu_v1_lib

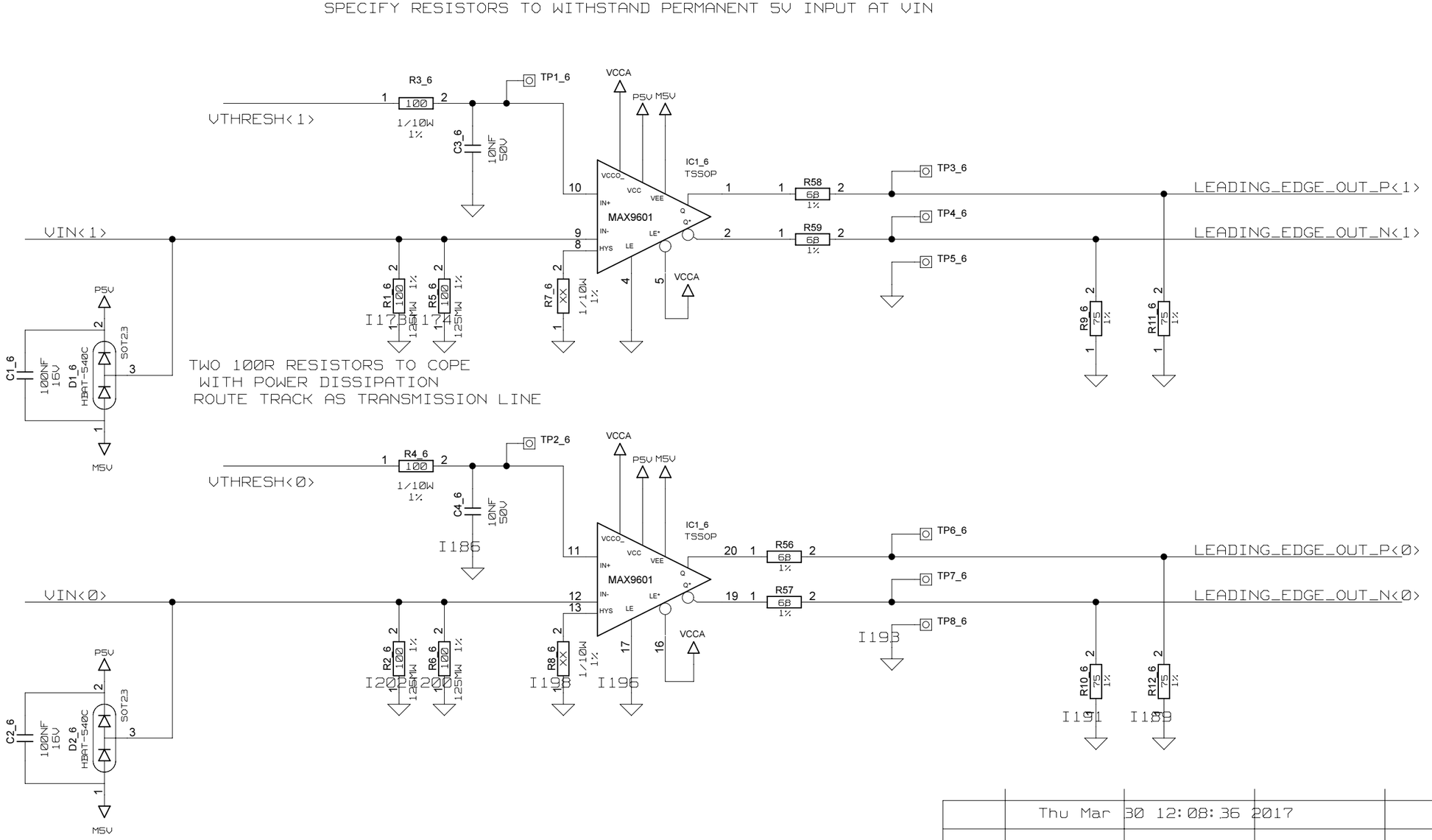
MODULE: pc023a_vthresh_buffer

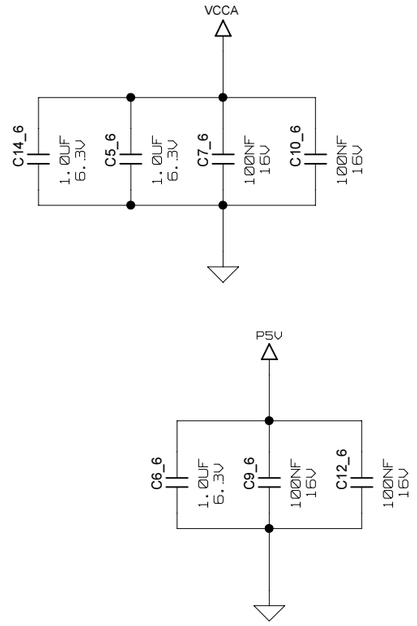
A2

MODULE PAGE: 1 OF 1
OVERALL PAGE: 24 OF 29

TOTAL NO. OF SHEETS

SPECIFY RESISTORS TO WITHSTAND PERMANENT 5V INPUT AT VIN





VTHRESH<1..0> IN

VIN<1..0> IN

LEADING_EDGE_OUT_P<1..0> OUT

LEADING_EDGE_OUT_N<1..0> OUT

	Thu Mar 30 12:08:36 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON

© UOB-HEP 20 12

UOB-HEP
UNIVERSITY OF BRISTOL
HIGH ENERGY PHYSICS GROUP
H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

TITLE fmc_tlu_v1_lib

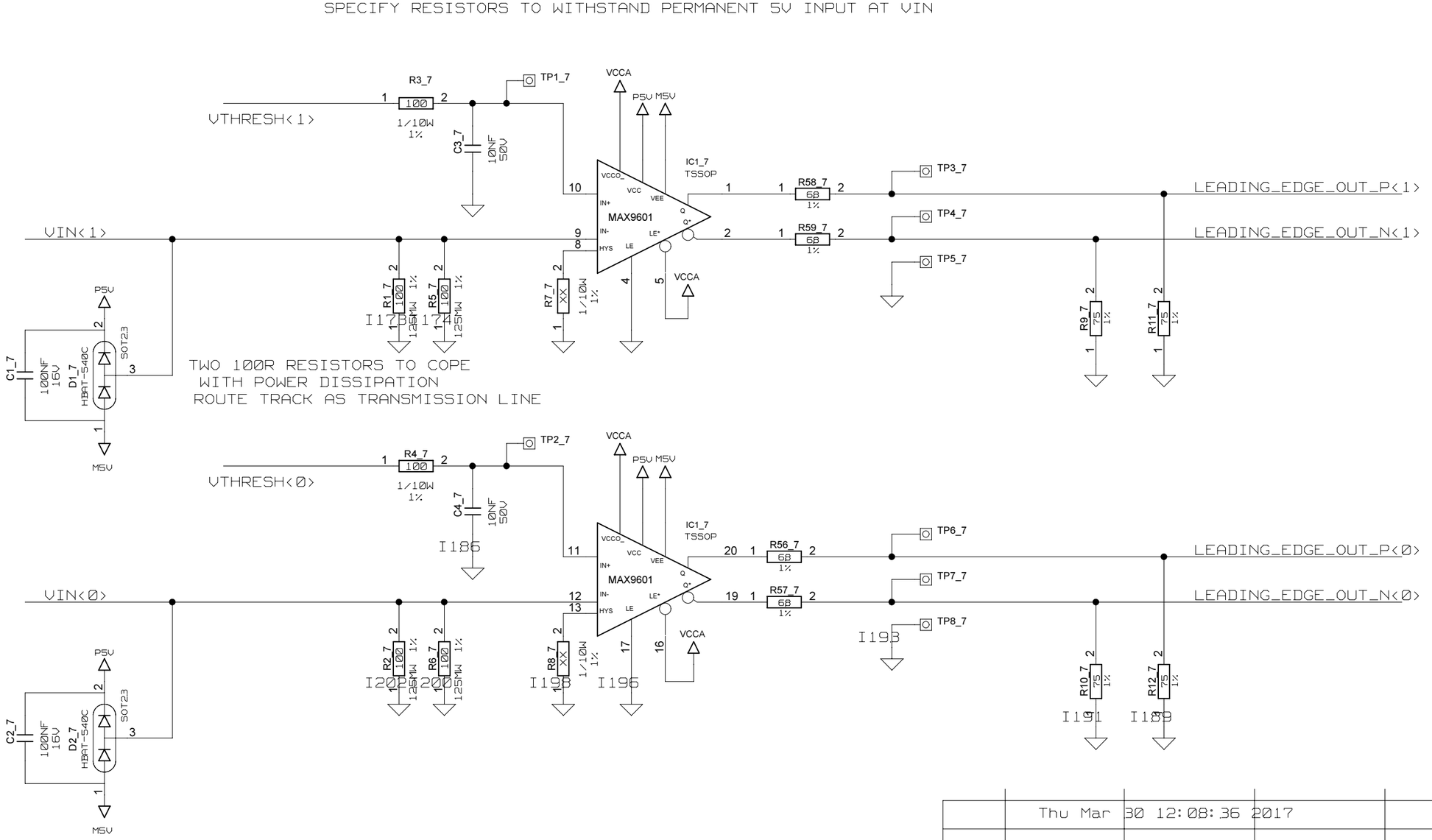
MODULE: fmc_tlu_threshold_discriminator_dual

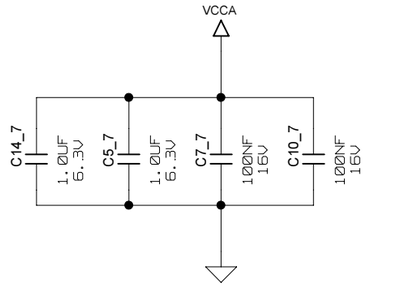
LICENSED UNDER THE TAPR OPEN HARDWARE LICENSE (WWW.TAPR.ORG/OHL)

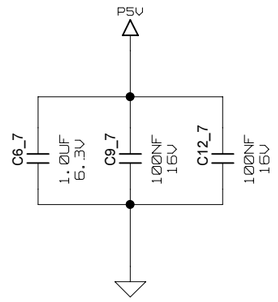
A2 MODULE PAGE: 1 OF 1
OVERALL PAGE: 25 OF 29

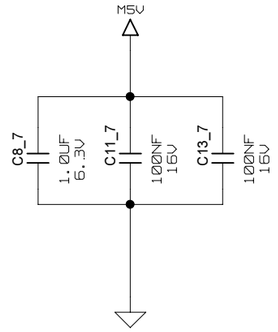
TOTAL NO. OF SHEETS

SPECIFY RESISTORS TO WITHSTAND PERMANENT 5V INPUT AT VIN









VTHRESH<1..0> IN

VIN<1..0> IN

LEADING_EDGE_OUT_P<1..0> OUT

LEADING_EDGE_OUT_N<1..0> OUT

	Thu Mar 30 12:08:36 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON

© UOB-HEP 20 12

UOB-HEP
UNIVERSITY OF BRISTOL
HIGH ENERGY PHYSICS GROUP
H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

TITLE fmc_tlu_v1_lib

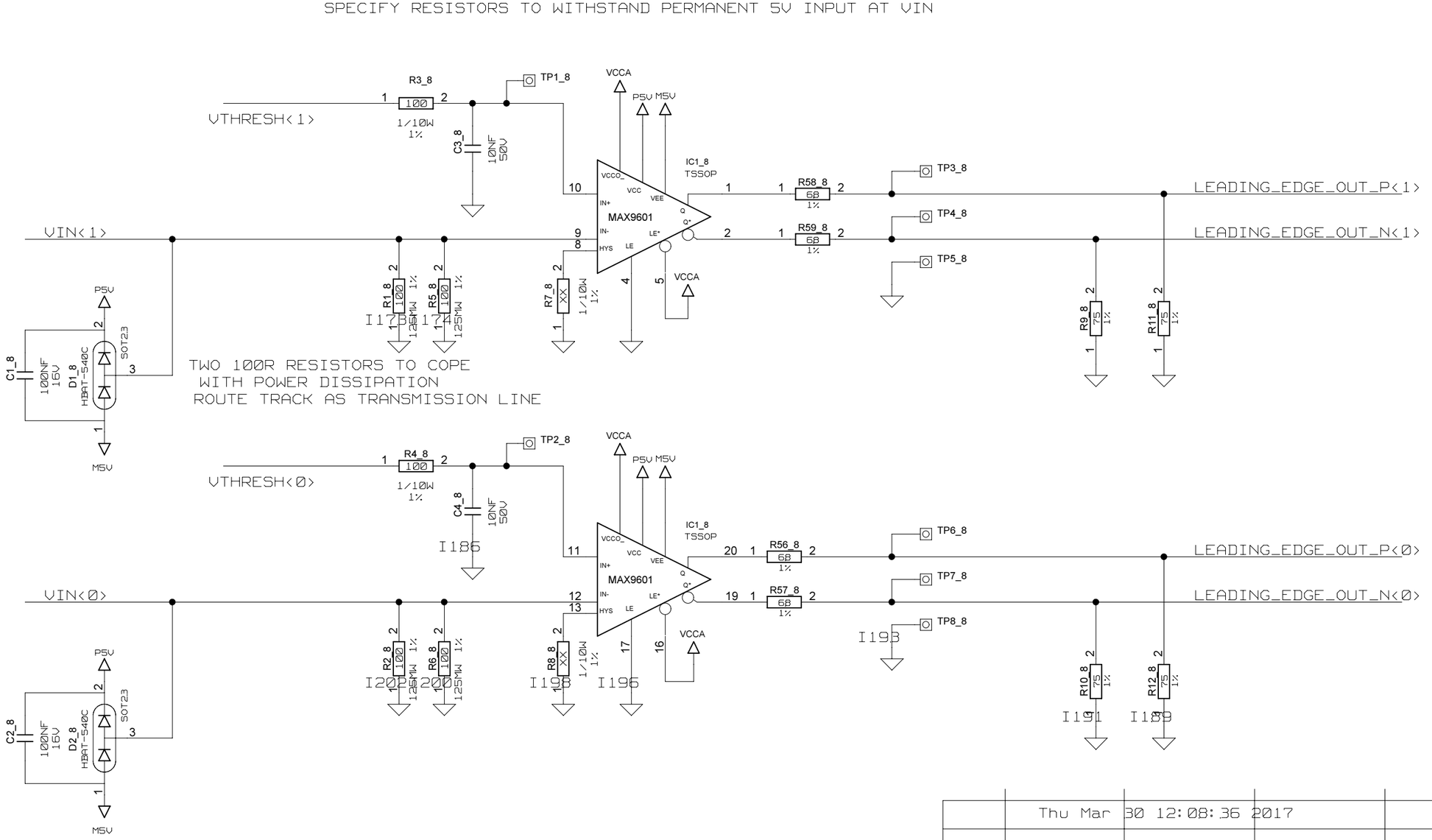
MODULE: fmc_tlu_threshold_discriminator_dual

LICENSED UNDER THE TAPR OPEN HARDWARE LICENSE (WWW.TAPR.ORG/OHL)

A2 MODULE PAGE: 1 OF 1
OVERALL PAGE: 26 OF 29

TOTAL NO. OF SHEETS

SPECIFY RESISTORS TO WITHSTAND PERMANENT 5V INPUT AT VIN



VTHRESH<1..0> IN

VIN<1..0> IN

LEADING_EDGE_OUT_P<1..0> OUT

LEADING_EDGE_OUT_N<1..0> OUT

	Thu Mar 30 12:08:36 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON

© UOB-HEP 20 12

UOB-HEP
UNIVERSITY OF BRISTOL
HIGH ENERGY PHYSICS GROUP
H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

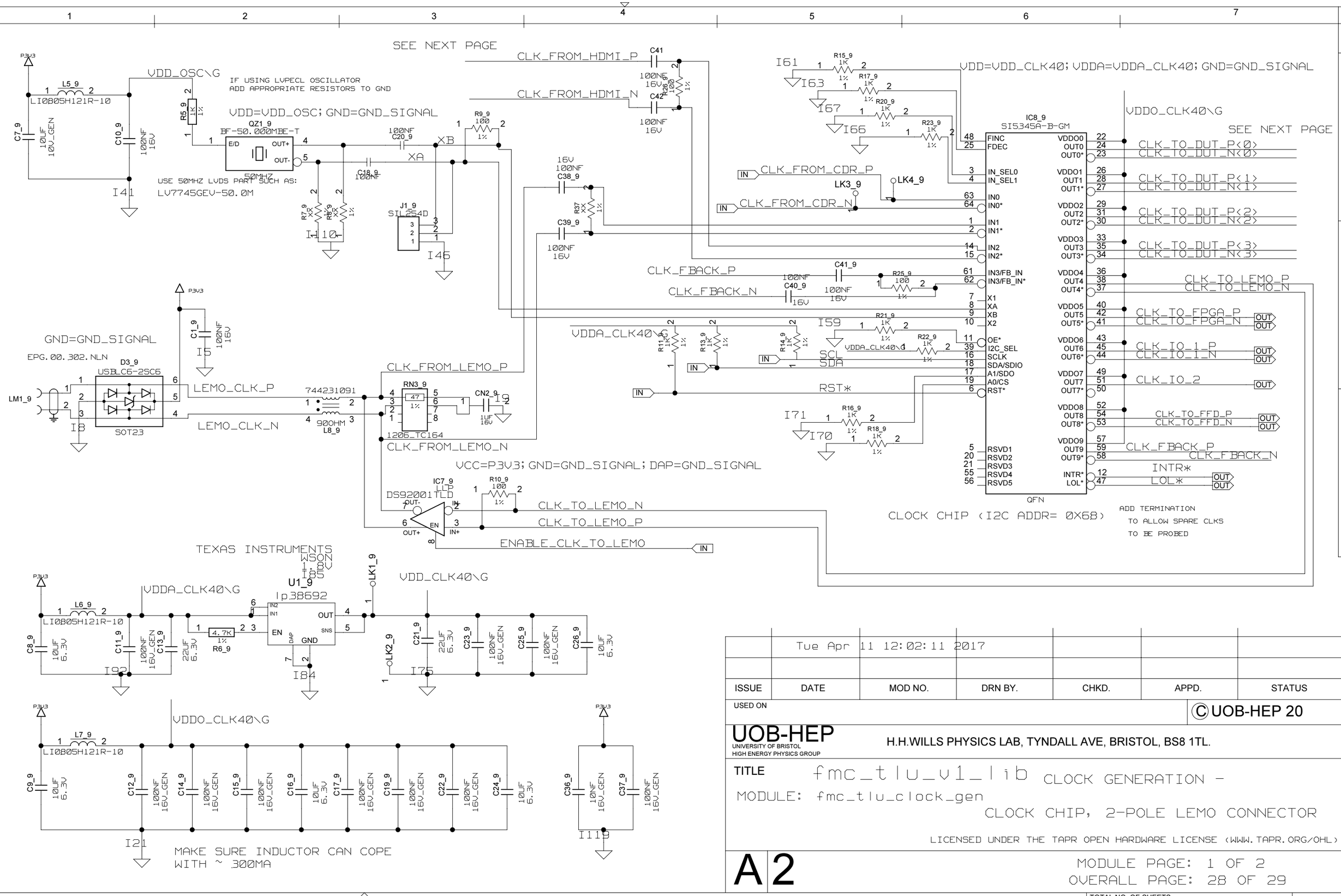
TITLE fmc_tlu_v1_lib

MODULE: fmc_tlu_threshold_discriminator_dual

LICENSED UNDER THE TAPR OPEN HARDWARE LICENSE (WWW.TAPR.ORG/OHL)

A2 MODULE PAGE: 1 OF 1
OVERALL PAGE: 27 OF 29

TOTAL NO. OF SHEETS



	Tue Apr 11 12:02:11 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON

© UOB-HEP 20

UOB-HEP
UNIVERSITY OF BRISTOL
HIGH ENERGY PHYSICS GROUP
H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

TITLE fmc_tlu_v1_lib CLOCK GENERATION -

MODULE: fmc_tlu_clock_gen

CLOCK CHIP, 2-POLE LEMO CONNECTOR

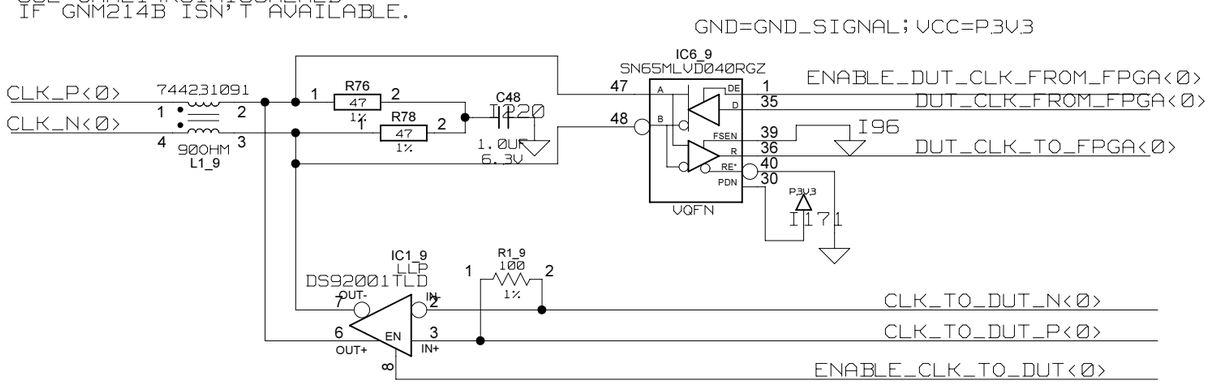
LICENSED UNDER THE TAPR OPEN HARDWARE LICENSE (WWW.TAPR.ORG/OHL)

A2

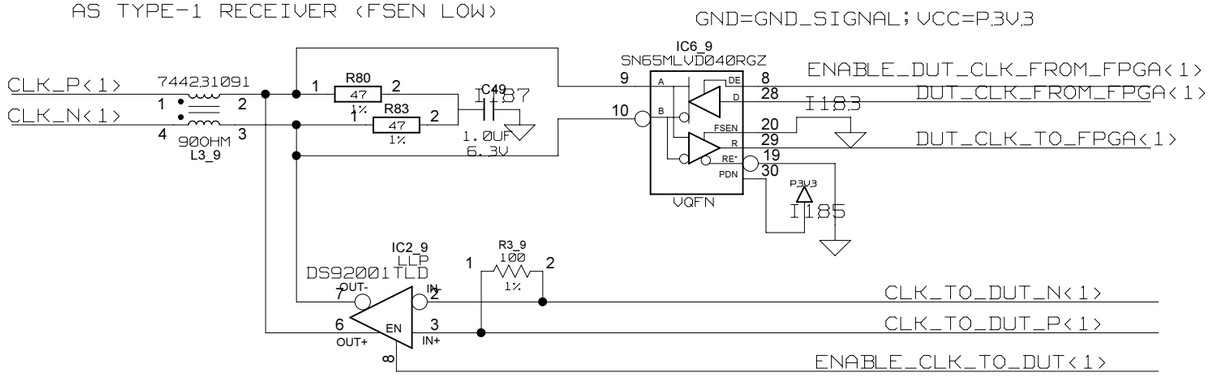
MODULE PAGE: 1 OF 2
OVERALL PAGE: 28 OF 29

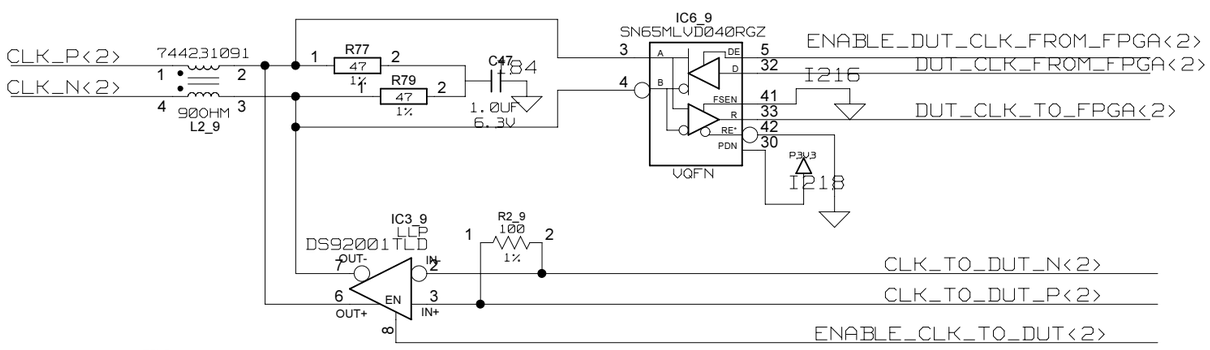
TOTAL NO. OF SHEETS

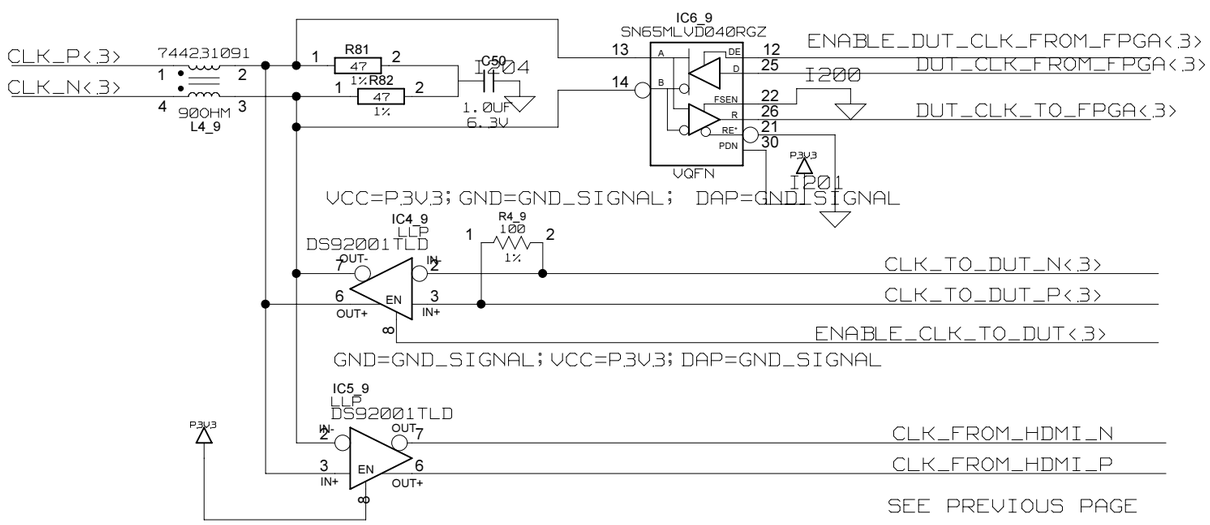
USE GNM214R61A105MEA2D
IF GNM214B ISN'T AVAILABLE.

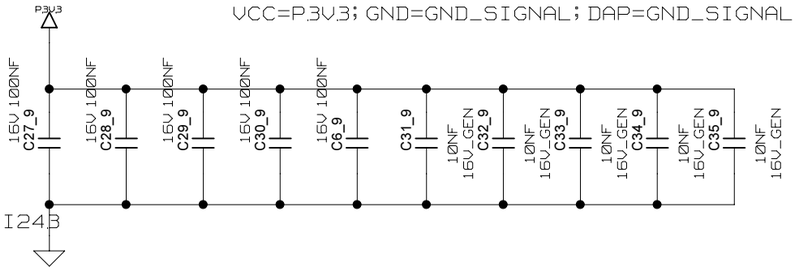


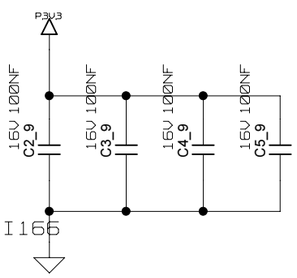
CONFIGURE SN65MLVD040
AS TYPE-1 RECEIVER (FSEN LOW)











CLK_P<3..0> OUT
CLK_N<3..0> OUT

ENABLE_DUT_CLK_FROM_FPGA<3..0> IN
DUT_CLK_FROM_FPGA<3..0> IN
DUT_CLK_TO_FPGA<3..0> OUT

ENABLE_CLK_TO_DUT<3..0> IN

	Fri May 05 14:48:32 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON

© UOB-HEP 20 11

UOB-HEP
UNIVERSITY OF BRISTOL
HIGH ENERGY PHYSICS GROUP
H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

TITLE fmc_tlu_v1_lib CLOCK GENERATION -
MODULE: fmc_tlu_clock_gen
I/O BUFFERS AND LEVEL TRANSLATORS

LICENSED UNDER THE TAPR OPEN HARDWARE LICENSE (WWW.TAPR.ORG/OHL)

A2

MODULE PAGE: 2 OF 2
OVERALL PAGE: 29 OF 29

TOTAL NO. OF SHEETS