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AIDA Trigger logic unit (TLU)

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Board fmc_tlu_v1d.

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Chapter 1

Preparation

Before powering the Trigger Logic Unit (TLU) it is necessary to follow a few steps to ensure the board and the Field Programmable Gate Array (FPGA) work correctly.
The FMC_TLU_v1d is designed to plug onto a carrier FPGA board like any other FPGA Mezzanine Card (FMC) mezzanine board, although its form factor does not comply with the ANSI-VITA-57-1 standard.
The firmware developed at University of Bristol is targeted to work with the Enclustra AX3 board, which must be plugged onto a PM3 base, also produced by Enclustra. The firmware is written on the FPGA using a Joint Test Action Group (JTAG) interface. Typically a breakout board will be required to connect the Xilinx programming cable to the Enclustra PM3.
Currently, it is recommended to use the following:

- MA-PM3-W-R5: Mars PM3 base board
- MA-AX3-35-1I-D8-R3: Marx AX3 module (hosts a Xilinx XC7A35T-1CSG324I)
- MA-PM3-ACC-BASE: Accessory kit, including a JTAG breakout board to connect Xilinx programming cables. Also includes a 12 V power supply to power the PM3.

1.1 I/O voltage setting

The I/O pins of the PM3 can be configured to operate at 2.5 V or 3.3 V; the factory default is 2.5 V but the FMC_TLU_v1d requires 3.3 V logic. The user should make sure to select the appropriate voltage by operating on DIP-switch CFG-A/S1200 (pin 1 set to ON).
For reference, a top view of the board is provided in the appendix at page 21.

Warning

Please double check the PM3 board manual for the correct way to change the I/O voltage setting. Enclustra has been changing their hardware recently.

1.2 Xilinx programming cable

The JTAG pins on the PM3 are located on the header J800 (20-way, 2.54 mm pitch). The breakout board provided by Enclustra sits on top of the header and connects the pins to a 14-way Molex milli-grid header so that it is possible to plug the Xiling programming cable directly onto it. However, when the FMC_TLU_v1d is mounted on a base plate as shown in figure 1.1, the breakout board has to be detached from the PM3 because it interferes with the mounting screws.
The connection between J800 and the breakout can be achieved by using two standard 20-way Insulation-Displacement Contact (IDC) cables as shown in figure 1.2.

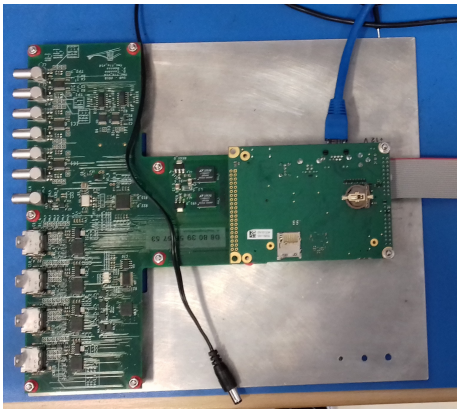

Figure 1.1: FMC_TLU_v1d and PM3 mounted on a base plate: in this configuration it is not possible to install the breakout board on the PM3 because the mountings screws are in the way.

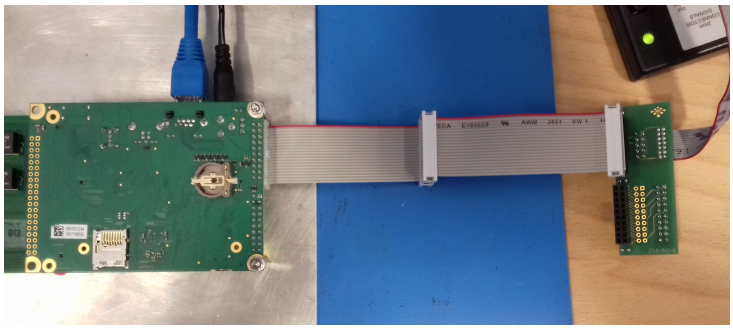

Figure 1.2: Connecting the Xilinx programming cable to the PM3 in an ugly (but effective) way.

Chapter 2

TLU Hardware

Board FMC_TLU_v1d is an evolution of the miniTLU designed at the University of Bristol (UoB). The board shares a few features with the miniTLU but also introduces several improvements. This chapter illustrates the main features of the board to provide a general view of its capabilities and an understanding of how to operate it in order to communicate with the Device Under Test (DUT)s.

2.1 Inputs and interfaces

FMC

The board must be plugged onto a FMC carrier board with an FPGA in order to function correctly. The connection is achieved using a low pin count FMC connector. The list of the pins used is provided in appendix at page 21.

DUT

The DUTs are connected to the TLU using standard size High-Definition Multimedia Interface (HDMI) connectors[1]. In this version of the hardware, up to four DUTs can be connected to the board. In this document the connectors will be referred to as `HDMI_DUT_1`, `HDMI_DUT_2`, `HDMI_DUT_3` and `HDMI_DUT_4`. The connectors expect 3.3 V Low Voltage Differential Signaling (LVDS) signals and are bi-directional, i.e. any differential pair can be configured to be an output (signal from the TLU to the DUT) or an input (signals from the DUT to the TLU) by using half-duplex line transceivers. Figure 2.1 illustrates how the differential pairs are connected to the transceivers.

[1] In the miniTLU hardware there were miniHDMI connectors.

Table 2.1: HDMI pin connections.

HDMI PIN	HDMI Signal Name	Enable Signal Name
1	HDMI_CLK	ENABLE_CLK_TO_DUT or ENABLE_DUT_CLK_FROM_FPGA
2	GND	–
3	HDMI_CLK*	ENABLE_CLK_TO_DUT or ENABLE_DUT_CLK_FROM_FPGA
4	CONT	ENABLE_CONT_FROM_FPGA
5	GND	–
6	CONT*	ENABLE_CONT_FROM_FPGA
7	BUSY	ENABLE_BUSY_FROM_FPGA
8	GND	–
9	BUSY*	ENABLE_BUSY_FROM_FPGA
10	SPARE	ENABLE_SPARE_FROM_FPGA
11	GND	–
12	SPARE*	ENABLE_SPARE_FROM_FPGA
13	n.c.	
14	HDMI_POWER	–
15	TRIG	ENABLE_TRIG_FROM_FPGA
16	TRIG*	ENABLE_TRIG_FROM_FPGA
17	GND	
18	n.c.	
19	n.c.	

Note

The input part of the transceiver is configured to be always on. This means that signals going *into* the TLU are always routed to the logic (FPGA). By contrast, the output transceivers have to be enabled and are off by default: signal sent from the logic to the DUTs cannot reach the devices unless the corresponding enable signal is active.

Table 2.1 shows the pin naming and the corresponding output enable signal. The clock pairs have two different enable signals to select the clock source (see section 3 for more details). In general only one of the clock sources should be active at any time.

The enable signals can be configured by programming two General Purpose Input/Output (GPIO) bus expanders via Inter-Integrated Circuit (I^2C) interface as described in section 2.4. In terms for functionalities, the four HDMI connectors are identical with one exception: the clock signal from

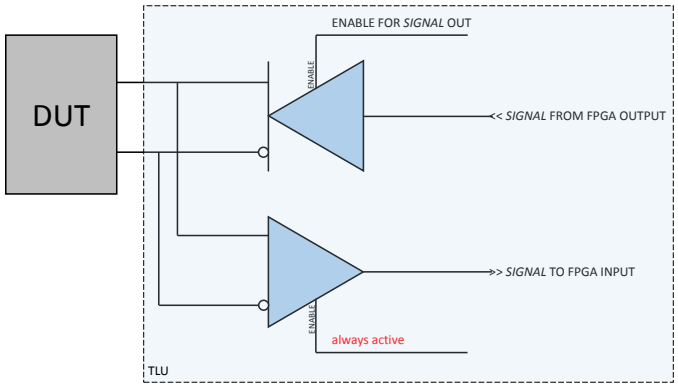

Figure 2.1: Internal configuration of the HDMI pins for the DUTs. The path from the DUT to the FPGA is always active. The path from the FPGA to the DUT can be enabled or disabled by the user.

`HDMI_DUT_4` can be used as reference for the clock generator chip mounted on the hardware. For more details on this functionality refer to section 3.

2.2 Clock LEMO

The board hosts a two-pin LEMO connector that can be used to provide a reference clock to the clock generator (see section 3) or to output the clock from the TLU to the external world, for instance to use it as a reference for another TLU. The signal level is 3.3 V LVDS.
As for the differential pairs of the DUTs, the pins of this connector are wired to a transceiver configured to always accept the incoming signals. The outgoing direction must be enabled by using the `ENABLE_CLK_TO_LEMO` signal, which can be configured using the bus expander described in in section 2.4.

2.3 Trigger inputs

Board FMC_TLU_v1d can accept up to six trigger inputs over the LEMO connectors labelled `IN_1`, `IN_2`, `IN_3`, `IN_4`, `IN_5` and `IN_6`. The FMC_TLU_v1d uses internal high-speed[2] discriminators to detect a valid trigger signal. The voltage thresholds can be adjusted independently for each input in a range from -1.3 V to +1.3 V with 40 μV resolution.
The adjustment is performed by writing to two 16-bit Digital to Analog Converter (DAC)s via I^2C interface as described in section 2.4.
The DACs can either use an internal reference voltage of 2.5 V or an external one of 1.3 V provided by the TLU: it is recommended to choose the external one by configuring the appropriate register in the devices.

[2] 500$\pm$30 ps propagation delay.

Table 2.2: DAC outputs and corresponding threshold inputs.

	Output	
	DAC2(Ic2)	**DAC1 (Ic1)**
Threshold 0	0	
Threshold 1	1	
Threshold 2		0
Threshold 3		1
Threshold 4		2
Threshold 5		3

The correspondence between DAC slave and thresholds is shown in table 2.2.

2.4 I^{2}C slaves

The I^{2}C interface on the FMC_TLU_v1d can be used to configured several features of the board. Table 2.3 lists all the valid addresses and the corresponding slave on the board. The Enclustra lines refer to slaves located on the PM3 board; these slaves can be ignored with the exception of the bus expander. The Enclustra expander is used to enable/disable the I^{2}C lines going to the FMC connector.

Note

After a power cycle the Enclustra expander is configured to disable the I^{2}C interface pins. This means that it is impossible to communicate to any I^{2}C slave on the TLU until the expander has been enabled.
The interface is enable by setting bit 7 to 0 on register 0x01 of the Enclustra expander.

Once the interface is enabled it is possible to read and write to the devices listed in the top part of table 2.3. The user should reference the manual of each individual component to determine the register that must be addressed. The rest of this section is meant to provide an overview of the slave functionalities.

DAC

Each DAC has four outputs that can be configured independently. `DAC1` is used to configure the thresholds of the first four trigger inputs; `DAC2` configures the remaining two thresholds.
The DACs should be configured to use the TLU voltage reference of 1.3 V. In these conditions, writing a value of 0x00000 to a DAC output will set the corresponding threshold to -1.3 V while a value of 0xFFFF will set it to +1.3 V.

Table 2.3: I²C addresses of the TLU.

CHIP	ID	FUNCTION	ADDRESS
IC1	AD5665RBRUZ	DAC1	0x1F
IC2	AD5665RBRUZ	DAC2	0x13
IC5	24AA025E48T	EEPROM	0x50
IC6	PCA9539PW	I2C Expander1	0x74
IC7	PCA9539PW	I2C Expander2	0x75
IC8_9	Si5345A	Clock Generator	0x68
Enclustra slaves			
		Enclustra Bus Expander	0x21
		Enclustra System Monitor	0x21
		Enclustra EEPROM	0x54
		Enclustra slave	0x64

EEPROM

The Electrically Erasable Programmable Read-Only Memory (EEPROM) located on the board contains a factory-set unique number, used to identify each FMC_TLU_v1d unequivocally. The number is comprised of six bytes written in as many memory locations.
The identifier is always in the form: `0xD8 80 39 XX XX XX` with the top three bytes indicating the manufacturer and the bottom three unique to each device.

Bus expander

The expanders are used as electronic switched to enable and disable individual lines. Each expander has two 8-bit banks; the values of the bits, as well as their direction (input/output) can be configured via the I²C interface. For the purpose of the TLU, all the expander pins should be configured as outputs since they must drive the enable signals on the DUT transceivers.

Clock generator

The clock for FMC_TLU_v1d can be generated using various external or internal references (see section 3 for further details). In order to reduce any jitter from the clock source and to provide a stable clock, the board hosts a Si5345 clock generator that needs to be configured via I²C interface.
The configuration involves writing ∼380 register values. A configuration file, containing all the register addresses and the corresponding values, can be generated using the ClockBuilder tool available from Silicon Labs.
The registers addresses between 0x026B and 0x0272 contain user-defined values that can be used to identify the configuration version: it is advisable to check those registers and ensure that they contain the correct code to ensure

that the chip is configured according to the TLU specifications.

TLU Producer

When using the TLU producer to configure hardware, the location of the configuration file can be specified by setting the `CLOCK_CFG_FILE` value in the *conf* file for the producer.
If no value is specified, the software will look for the configuration file `../conf/confClk.txt` i.e. if the `euRun` binary file is located in `./eudaq/bin`, then the default configuration file should reside in `./eudaq/conf`. The configuration will produce an error if the file is not found.

Chapter 3

Clock

The TLU can use various sources to produce a stable 40 MHz clock[1]. A Low-voltage Positive Emitter-Coupled Logic (LVPECL) crystal provides the reference 50 MHz clock for a Si5345A jitter attenuator. The Si5345A can accept up to four clock sources and use them to generate the required output clocks.
In the TLU the possible sources are: pair of external pins LK4_9 and LK3_9, differential LEMO connector LM1_9, FPGA pins (`CLK_FROM_FPGA`) and one of the four HDMI connectors (`HDMI_DUT_4`).
The low-jitter clock generated by the Si5345A can be distributed to up to ten recipients. In the TLU these are: the four DUTs via HDMI connectors, the differential LEMO cable, the FPGA, connector J1 as a differential pair (pins 4 and 6) and as a single ended signal (pin 8), two test resistors R24_9 and R54_9.
The DUTs can receive the clock either from the Si5435A or directly from the FPGA: when provided by the clock generator, the signal name is `CLK\_TO\_DUT` and is enabled by signal `ENABLE_CLK_TO_DUT`; when the signal is provided directly from the FPGA the line used is `DUT_CLK_FROM_FPGA` and is enabled by `ENABLE_DUT_CLK_FROM_FPGA`.
The firmware uses the clock generated by the Si5345A except for the block `enclustra_ax3_pm3_infra` which relies on a crystal mounted on the Enclustra board to provide the IPBus functionalities (in this way, at power up the board can communicate via IPBus even if the Si5345A is not configured).

3.1 Input selection

The Si5345 has four inputs that can be selected to provide the clock alignment; the selection can be automatic or user-defined.

[1] For some applications a 50 MHz clock will be required instead

Table 3.1: Si5345 Input Selection Configuration.

Register Name	**Hex Address [Bit Field]**	**Function**
CLK_SWITCH_MODE	0x0536[1:0]	Selects manual or automatic switching modes. Automatic mode can be revertive or non-reverti Selections are the following: 00 Manual 01 Automatic non-revertive 02 Automatic revertive 03 Reserved
IN_SEL_REGCTRL	0x052A [0]	0 for pin controlled clock selection 1 for register controlled clock selection
IN_SEL	0x052A [2:1]	0 for IN0 1 for IN1 2 for IN2 3 for IN3 (or FB_IN)

3.2 Logic clocks registers

LogicClocksCSR: in the new TLU the selection of the clock source is done by programming the Si5345. As a consequence, there is no reason to write to this register. Reading it back returns the status of the PLL on bit 0, so this should read 0x1.

Chapter 4

DUT signals

In the old firmware the clock signals (`dut_clk_n_o`, `dut_clk_p_o`) were configured as input/output. The new hardware has the lines separated so `dut_clk_p_i` is the input vector and `dut_clk_p_o` the output one.

4.1 Trigger inputs

The status register (SerdesRst) is as follows:

- bit 0: reset the ISERDES
- bit 1: reset the trigger counters
- bit 2: calibrate IDELAY: This seems to be disconnected at the moment.
- bit 3: fixed to 0
- bit 4, 5: status of `thresholdDeserializer(Input0)`. When the IDELAY modules (prompt, delayed) have reached the correct delay, these two bits should read 00.
- bit 6, 7: status of `thresholdDeserializer(Input1)`
- bit 8, 9: status of `thresholdDeserializer(Input2)`
- bit 10, 11: status of `thresholdDeserializer(Input3)`
- bit 12, 13: status of `thresholdDeserializer(Input4)`
- bit 14, 15: status of `thresholdDeserializer(Input5)`
- bit 16, 19: fixed to 0
- bit 20: `s_deserialized_threshold_data(Input0)(7)`
- bit 21: `s_deserialized_threshold_data(Input1)(7)`
- bit 22: `s_deserialized_threshold_data(Input2)(7)`
- bit 23: `s_deserialized_threshold_data(Input3)(7)`
- bit 24: `s_deserialized_threshold_data(Input4)(7)`
- bit 25: `s_deserialized_threshold_data(Input5)(7)`

9 bits are used to determine trigger edges. 8 are from the deserializers, 1 is added as the LSB and is the MSB from the previous word.

4.2 Trigger logic

The TLU has six trigger inputs than can be used to generate a valid trigger event. The number of possible different trigger combinations is $2^6 = 64$ so a 64-bit word can be used to decide the valid combinations. In the hardware the 64-bit word is split into two 32-bit words and the rules to generate the trigger can be specified by the user by writing in the two 32-bit registers `TriggerPattern_highW` and `TriggerPattern_lowW`: the first stores the

32 most significative bits of the trigger word, the latter stores the least significative bits.
The user can select any combination of the trigger inputs and declare it a valid trigger pattern by setting a 1 in the corresponding trigger configuration word. Tables 4.1 and 4.2 show an example of how to determine the trigger configuration words: whenever a valid trigger combination is encountered, the user should put a 1 in the corresponding row under the PATTERN column. The pattern thus obtained is the required word to write in the configuration register.
It is important to note that this solution allows the user to set veto pattern as well: for instance if only word 31 from table 4.1 were picked, then the TLU would only register a trigger when the combination $\overline{I_5} + I_4 + I_3 + I_2 + I_1 + I_0$ was presented at its inputs. In other words, in this specific case I_5 would act as a veto signal.
The default configuration in the firmware is Hi= 0xFFFFFFFF, Low= 0xFFFEFFFE, which means that as long as any trigger input fires, a trigger will be generated. These words are loaded in the FPGA every time the firmware is flushed.

Trigger logic definition

The user should pay attention to what trigger logic they want to define in order to avoid confusion in the data.
A "1" in the logic table means that the corresponding input must be active to produce a valid trigger. Similarly, a "0" indicates that the corresponding input must be inactive (i.e. is a veto, not an ignore). Any change in input configuration will cause the logic to re-assess the trigger status. The following section gives a brief example.

Example

In this example we have connected a pulser to two inputs of the TLU, namely input 0 and input 4. The inputs fire with a small, random delay with respect to each other.
In order to ensure that the signals overlap adequately, we use the *stretch* register (see chapter 7) to increase the length of the pulses: we extend *in0* to 10 clock cycles and *in4* to 8 clock cycles. The resulting signals are shown in figure 4.1.
We can now define the trigger logic to be used to assert a valid trigger: we only consider the lower 32-bits of the trigger word and see how different values can produce very different results.

- Trigger Least Significant Bit (LSB) word= 0x00020000. This indicates that the only valid trigger combination occurs when both *in0* and *in4*

Table 4.1: Example of configuration word for the least significative bits of the trigger registers: the only valid configuration is represented by $\overline{I_5} + I_4 + I_3 + I_2 + I_1 + I_0$, i.e. a trigger is accepted if all the inputs, except I_5, present a logic 1 at the same time. The user would then write the resulting word 0x80000000 in the TriggerPattern_lowW register.

DEC	I5	I4	I3	I2	I1	I0	PATTERN	CONFIG. WORD		2^n
0	0	0	0	0	0	0	0	0	LOWEST 32-bits	1
1	0	0	0	0	0	1	0			2
2	0	0	0	0	1	0	0			4
3	0	0	0	0	1	1	0			8
4	0	0	0	1	0	0	0	0		16
5	0	0	0	1	0	1	0			32
6	0	0	0	1	1	0	0			64
7	0	0	0	1	1	1	0			128
8	0	0	1	0	0	0	0	0		256
9	0	0	1	0	0	1	0			512
10	0	0	1	0	1	0	0			1024
11	0	0	1	0	1	1	0			2048
12	0	0	1	1	0	0	0	0		4096
13	0	0	1	1	0	1	0			8192
14	0	0	1	1	1	0	0			16384
15	0	0	1	1	1	1	0			32768
16	0	1	0	0	0	0	0	0		65536
17	0	1	0	0	0	1	0			131072
18	0	1	0	0	1	0	0			262144
19	0	1	0	0	1	1	0			524288
20	0	1	0	1	0	0	0	0		1048576
21	0	1	0	1	0	1	0			2097152
22	0	1	0	1	1	0	0			4194304
23	0	1	0	1	1	1	0			8388608
24	0	1	1	0	0	0	0	0		16777216
25	0	1	1	0	0	1	0			33554432
26	0	1	1	0	1	0	0			67108864
27	0	1	1	0	1	1	0			134217728
28	0	1	1	1	0	0	0	8		268435456
29	0	1	1	1	0	1	0			536870912
30	0	1	1	1	1	0	0			1073741824
31	0	1	1	1	1	1	1			2147483648

Table 4.2: Example of the most significative word of the register: a valid trigger is obtained when the inputs show the same configuration as row DEC 36, 37, 38, 39, 41, 43 and 63. These configuration are in logic OR with that presented in table 4.1. The resulting configuration word is 0x80000AF0.

DEC	I5	I4	I3	I2	I1	I0	PATTERN	CONFIG. WORD		2^n
32	1	0	0	0	0	0	0 0	0	HIGHEST 32-bits	1
33	1	0	0	0	0	1	0 0			2
34	1	0	0	0	1	0	0 0			4
35	1	0	0	0	1	1	0 0			8
36	1	0	0	1	0	0	1 1	F		16
37	1	0	0	1	0	1	1 1			32
38	1	0	0	1	1	0	1 1			64
39	1	0	0	1	1	1	1 1			128
40	1	0	1	0	0	0	1 0	A		256
41	1	0	1	0	0	1	1 0			512
42	1	0	1	0	1	0	1 0			1024
43	1	0	1	0	1	1	1 0			2048
44	1	0	1	1	0	0	0 0	0		4096
45	1	0	1	1	0	1	0 0			8192
46	1	0	1	1	1	0	0 0			16384
47	1	0	1	1	1	1	0 0			32768
48	1	1	0	0	0	0	0 0	0		65536
49	1	1	0	0	0	1	0 0			131072
50	1	1	0	0	1	0	0 0			262144
51	1	1	0	0	1	1	0 0			524288
52	1	1	0	1	0	0	0 0	0		1048576
53	1	1	0	1	0	1	0 0			2097152
54	1	1	0	1	1	0	0 0			4194304
55	1	1	0	1	1	1	0 0			8388608
56	1	1	1	0	0	0	0 0	0		16777216
57	1	1	1	0	0	1	0 0			33554432
58	1	1	1	0	1	0	0 0			67108864
59	1	1	1	0	1	1	0 0			134217728
60	1	1	1	1	0	0	0 0	8		268435456
61	1	1	1	1	0	1	0 0			536870912
62	1	1	1	1	1	0	1 0			1073741824
63	1	1	1	1	1	1	1 0			2147483648

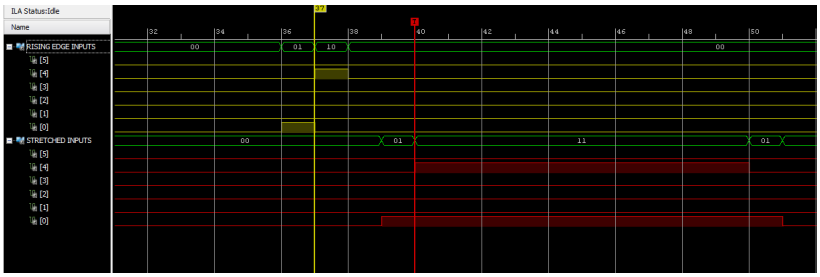

Figure 4.1: Input pulses (yellow) and corresponding stretched signals (red). Input 0 is stretched by 10 cycles, input 4 by 8, hence the difference in pulse widths.

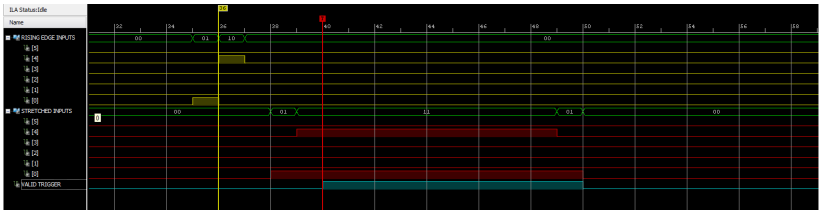

Figure 4.2: Trigger configuration 0x00020000. The valid trigger (blue) is asserted only when both signals are high. This condition occurs at frame 39. The trigger is asserted on the following frame.

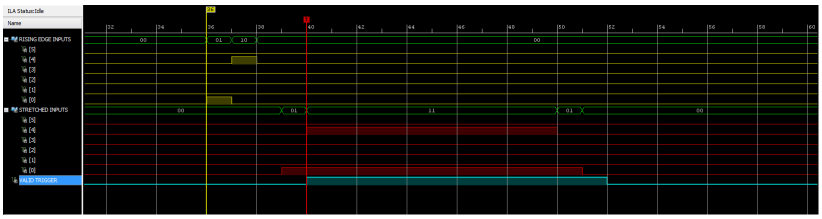

Figure 4.3: Trigger configuration 0x00020002. The valid trigger (blue) is asserted if *in0* is high OR when *in0* and *in4* are both high at the same time.

are high. The valid trigger goes high 1 clock cycle after this condition is met and remains high up to 1 clock cycle after the condition is no longer valid. This is illustrated in figure 4.2.

- Trigger LSB word= 0x00020002. This indicates that a valid trigger is achieved in two separated configurations (in logic OR): when both inputs are high at the same time (as in the previous case) or if *in0* is active on its own. This is illustrated in figure 4.3. It can be seen that the valid trigger is asserted immediately one clock cycle after *in0* is high and remains high as long as this condition is met. One might assume that specifying the combination with input 4 is redundant, but the following example should show that this is not the case.

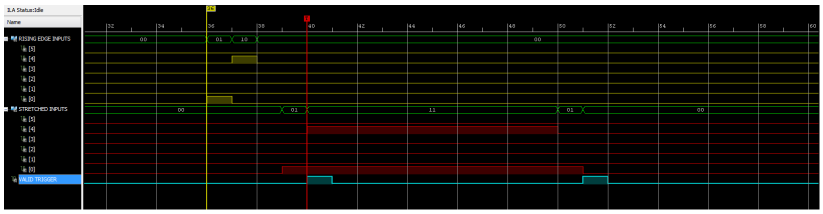

Figure 4.4: Trigger configuration 0x00000002. The valid trigger (blue) is asserted only when *in0* is active on its own. As such, two separated trigger pulses are produced because *in4* goes high and returns low before *in0*.

- Trigger LSB word= 0x00000002. This indicates that the only valid configuration is the one where only *in0* is high. It is important to understand that in this configuration all other inputs act as veto. This might produce unexpected results if the user is not careful[1].
  In figure 4.4 it is possible to see that the logic produces two separated trigger valid pulses, both shorter than the ones in previous examples: the first one is due to *in0* going high while *in4* is low. As soon as *in4* goes high, the trigger condition is no longer met. When *in4* returns low, a trigger condition is met again because *in0* is still high. In this specific case, the double pulse is caused by the different width of the pulses.

[1]Specifically, pulse stretch, pulse delay and trigger logic must be configured correctly to avoid unwanted results.

4.3 Event buffer

The event buffer IPBus slave has four registers. Writing to `EventFifoCSR` will reset the First In First Out (FIFO). Reading from either of the register will put their data on the IPBus data line.
Reading from `EventFifoCSR` returns the following:

- bit 0: FIFO empty flag
- bit 1: FIFO almost empty flag
- bit 2: FIFO almost full flag
- bit 3: FIFO full flag
- bit 4: FIFO programmable full flag
- other bits: 0

Chapter 5

Appendix

2.4 Top view

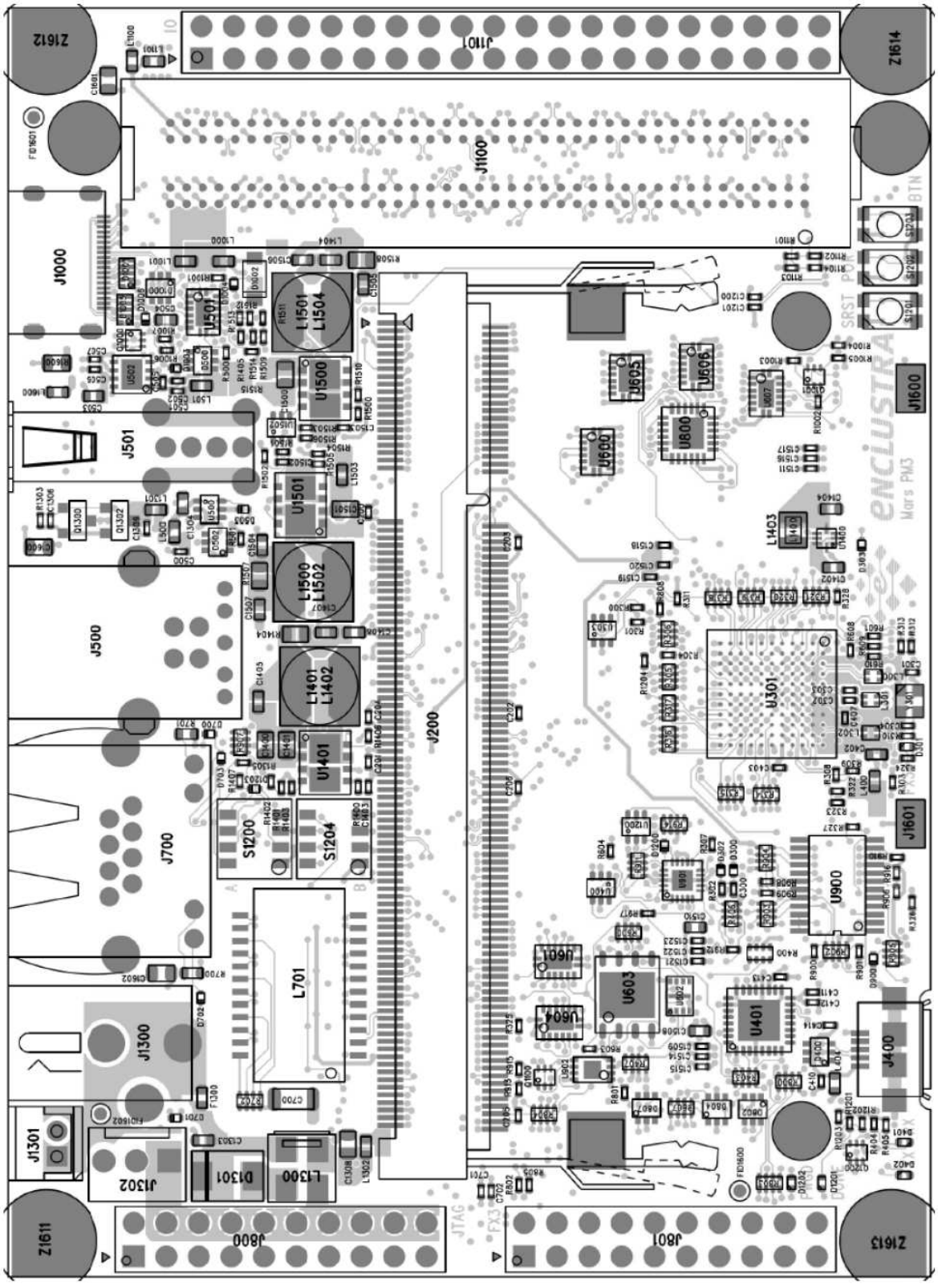

Figure 3: Top view

Schematic side			FPGA Side				
NET NAME	**FMC_LA**	**J4**	**FMC NAME**	**PACKAGE_PIN**	**VDHL NAME**	**FPGA IN/OUT**	**CONSTRAINT INSTRUCTION**
BEAM_TRIGGER_P<0>	FMC_LA<32>	H37	LA32_P	B1	threshold_discr_p_i[0]	In	set_property PACKAGE_PIN B1 [get_ports {threshold_discr_p_i[0]}]
BEAM_TRIGGER_P<1>	FMC_LA<33>	G36	LA33_P	C4	threshold_discr_p_i[1]	In	set_property PACKAGE_PIN C4 [get_ports {threshold_discr_p_i[1]}]
BEAM_TRIGGER_P<2>	FMC_LA<30>	H34	LA30_P	K2	threshold_discr_p_i[2]	In	set_property PACKAGE_PIN K2 [get_ports {threshold_discr_p_i[2]}]
BEAM_TRIGGER_P<3>	FMC_LA<31>	G33	LA31_P	C6	threshold_discr_p_i[3]	In	set_property PACKAGE_PIN C6 [get_ports {threshold_discr_p_i[3]}]
BEAM_TRIGGER_P<4>	FMC_LA<28>	H31	LA28_P	J4	threshold_discr_p_i[4]	In	set_property PACKAGE_PIN J4 [get_ports {threshold_discr_p_i[4]}]
BEAM_TRIGGER_P<5>	FMC_LA<29>	G30	LA29_P	H1	threshold_discr_p_i[5]	In	set_property PACKAGE_PIN H1 [get_ports {threshold_discr_p_i[5]}]
BEAM_TRIGGER_N<0>	FMC_LA*<32>	H38	LA32_N	A1	threshold_discr_n_i[0]	In	set_property PACKAGE_PIN A1 [get_ports {threshold_discr_n_i[0]}]
BEAM_TRIGGER_N<1>	FMC_LA*<33>	G37	LA33_N	B4	threshold_discr_n_i[1]	In	set_property PACKAGE_PIN B4 [get_ports {threshold_discr_n_i[1]}]
BEAM_TRIGGER_N<2>	FMC_LA*<30>	H35	LA30_N	K1	threshold_discr_n_i[2]	In	set_property PACKAGE_PIN K1 [get_ports {threshold_discr_n_i[2]}]
BEAM_TRIGGER_N<3>	FMC_LA*<31>	G34	LA31_N	C5	threshold_discr_n_i[3]	In	set_property PACKAGE_PIN C5 [get_ports {threshold_discr_n_i[3]}]
BEAM_TRIGGER_N<4>	FMC_LA*<28>	H32	LA28_N	H4	threshold_discr_n_i[4]	In	set_property PACKAGE_PIN H4 [get_ports {threshold_discr_n_i[4]}]
BEAM_TRIGGER_N<5>	FMC_LA*<29>	G31	LA29_N	G1	threshold_discr_n_i[5]	In	set_property PACKAGE_PIN G1 [get_ports {threshold_discr_n_i[5]}]
				P17	enclustra_clk	In	
CLK_TO_FPGA_P	FMC_CLK0_M2C_P	H4	CLK0_M2C_P	T5	sysclk_40_i_p	In	set_property PACKAGE_PIN T5 [get_ports {sysclk_40_i_p}]
CLK_TO_FPGA_N	FMC_CLK0_M2C_N	H5	CLK0_M2C_N	T4	sysclk_40_i_n	In	set_property PACKAGE_PIN T4 [get_ports {sysclk_40_i_n}]
CLK_FROM_FPGA_P	FMC_CLK1_M2C_P	G2	CLK1_M2C_P	E3	sysclk_50_o_p	Out	set_property PACKAGE_PIN E3 [get_ports {sysclk_50_o_p}]
CLK_FROM_FPGA_N	FMC_CLK1_M2C_N	G3	CLK1_M2C_N	D3	sysclk_50_o_n	Out	set_property PACKAGE_PIN D3 [get_ports {sysclk_50_o_n}]
I2C_RESET_N	FMC_LA<21>	H25	LA21_P	C2	i2c_reset	Out	set_property PACKAGE_PIN C2 [get_ports {i2c_reset}]
GPIO	FMC_LA*<24>	H29	LA24_N	F6	gpio	In/Out	set_property PACKAGE_PIN F6 [get_ports {gpio}]
CLK_GEN_RST_N	FMC_LA*<21>	H26	LA21_N	C1	clk_gen_rst	Out	set_property PACKAGE_PIN C1 [get_ports {clk_gen_rst}]
CLK_GEN_LOL_N	FMC_LA<0>	G6	LA00_P_CC			In	
CONT_TO_FPGA<0>	FMC_LA*<0>	G7	LA00_N_CC	P5	cont_i[0]	In	set_property PACKAGE_PIN P5 [get_ports {cont_i[0]}]
CONT_TO_FPGA<1>	FMC_LA*<1>	D9	LA01_N_CC	P3	cont_i[1]	In	set_property PACKAGE_PIN P3 [get_ports {cont_i[1]}]
CONT_TO_FPGA<2>	FMC_LA*<2>	H8	LA02_N	N6	cont_i[2]	In	set_property PACKAGE_PIN N6 [get_ports {cont_i[2]}]
CONT_TO_FPGA<3>	FMC_LA*<3>	G10	LA03_N	L5	cont_i[3]	In	set_property PACKAGE_PIN L5 [get_ports {cont_i[3]}]
SPARE_TO_FPGA<0>	FMC_LA*<4>	H11	LA04_N	M1	spare_i[0]	In	set_property PACKAGE_PIN M1 [get_ports {spare_i[0]}]
SPARE_TO_FPGA<1>	FMC_LA*<5>	D12	LA05_N	N4	spare_i[1]	In	set_property PACKAGE_PIN N4 [get_ports {spare_i[1]}]
SPARE_TO_FPGA<2>	FMC_LA*<6>	C11	LA06_N	N1	spare_i[2]	In	set_property PACKAGE_PIN N1 [get_ports {spare_i[2]}]
SPARE_TO_FPGA<3>	FMC_LA*<7>	H14	LA07_N	M2	spare_i[3]	In	set_property PACKAGE_PIN M2 [get_ports {spare_i[3]}]
TRIG_TO_FPGA<0>	FMC_LA*<8>	G13	LA08_N	R5	triggers_i[0]	In	set_property PACKAGE_PIN R5 [get_ports {triggers_i[0]}]
TRIG_TO_FPGA<1>	FMC_LA*<9>	D15	LA09_N	R2	triggers_i[1]	In	set_property PACKAGE_PIN R2 [get_ports {triggers_i[1]}]
TRIG_TO_FPGA<2>	FMC_LA*<10>	C15	LA10_N	T1	triggers_i[2]	In	set_property PACKAGE_PIN T1 [get_ports {triggers_i[2]}]
TRIG_TO_FPGA<3>	FMC_LA*<11>	H17	LA11_N	V1	triggers_i[3]	In	set_property PACKAGE_PIN V1 [get_ports {triggers_i[3]}]
BUSY_TO_FPGA<0>	FMC_LA*<12>	G16	LA12_N	T6	busy_i[0]	In	set_property PACKAGE_PIN T6 [get_ports {busy_i[0]}]
BUSY_TO_FPGA<1>	FMC_LA*<13>	D18	LA13_N	U3	busy_i[1]	In	set_property PACKAGE_PIN U3 [get_ports {busy_i[1]}]
BUSY_TO_FPGA<3>	FMC_LA*<14>	C19	LA14_N	T8	busy_i[2]	In	set_property PACKAGE_PIN T8 [get_ports {busy_i[2]}]

BUSY_TO_FPGA<2>	FMC_LA*<15>	H20	LA15_N	L4	busy_i[3]	In	set_property PACKAGE_PIN L4 [get_ports {busy_i[3]}]
DUT_CLK_TO_FPGA<0>	FMC_LA*<16>	G19	LA16_N	L3	dut_clk_i[0]	In	set_property PACKAGE_PIN L3 [get_ports {dut_clk_i[0]}]
DUT_CLK_TO_FPGA<1>	FMC_LA*<17>	D21	LA17_N_CC	F3	dut_clk_i[1]	In	set_property PACKAGE_PIN F3 [get_ports {dut_clk_i[1]}]
DUT_CLK_TO_FPGA<2>	FMC_LA*<18>	C23	LA18_N_CC	D2	dut_clk_i[2]	In	set_property PACKAGE_PIN D2 [get_ports {dut_clk_i[2]}]
DUT_CLK_TO_FPGA<3>	FMC_LA*<19>	H23	LA19_N	G3	dut_clk_i[3]	In	set_property PACKAGE_PIN G3 [get_ports {dut_clk_i[3]}]
CONT_FROM_FPGA<0>	FMC_LA<0>	G6	LA00_P_CC	N5	cont_o[0]	Out	set_property PACKAGE_PIN N5 [get_ports {cont_o[0]}]
CONT_FROM_FPGA<1>	FMC_LA<1>	D8	LA01_P_CC	P4	cont_o[1]	Out	set_property PACKAGE_PIN P4 [get_ports {cont_o[1]}]
CONT_FROM_FPGA<2>	FMC_LA<2>	H7	LA02_P	M6	cont_o[2]	Out	set_property PACKAGE_PIN M6 [get_ports {cont_o[2]}]
CONT_FROM_FPGA<3>	FMC_LA<3>	G9	LA03_P	L6	cont_o[3]	Out	set_property PACKAGE_PIN L6 [get_ports {cont_o[3]}]
SPARE_FROM_FPGA<0>	FMC_LA<4>	H10	LA04_P	L1	spare_o[0]	Out	set_property PACKAGE_PIN L1 [get_ports {spare_o[0]}]
SPARE_FROM_FPGA<1>	FMC_LA<5>	D11	LA05_P	M4	spare_o[1]	Out	set_property PACKAGE_PIN M4 [get_ports {spare_o[1]}]
SPARE_FROM_FPGA<2>	FMC_LA<6>	C10	LA06_P	N2	spare_o[2]	Out	set_property PACKAGE_PIN N2 [get_ports {spare_o[2]}]
SPARE_FROM_FPGA<3>	FMC_LA<7>	H13	LA07_P	M3	spare_o[3]	Out	set_property PACKAGE_PIN M3 [get_ports {spare_o[3]}]
TRIG_FROM_FPGA<0>	FMC_LA<8>	G12	LA08_P	R6	triggers_o[0]	Out	set_property PACKAGE_PIN R6 [get_ports {triggers_o[0]}]
TRIG_FROM_FPGA<1>	FMC_LA<9>	D14	LA09_P	P2	triggers_o[1]	Out	set_property PACKAGE_PIN P2 [get_ports {triggers_o[1]}]
TRIG_FROM_FPGA<2>	FMC_LA<10>	C14	LA10_P	R1	triggers_o[2]	Out	set_property PACKAGE_PIN R1 [get_ports {triggers_o[2]}]
TRIG_FROM_FPGA<3>	FMC_LA<11>	H16	LA11_P	U1	triggers_o[3]	Out	set_property PACKAGE_PIN U1 [get_ports {triggers_o[3]}]
BUSY_FROM_FPGA<0>	FMC_LA<12>	G15	LA12_P	R7	busy_o[0]	Out	set_property PACKAGE_PIN R7 [get_ports {busy_o[0]}]
BUSY_FROM_FPGA<1>	FMC_LA<13>	D17	LA13_P	U4	busy_o[1]	Out	set_property PACKAGE_PIN U4 [get_ports {busy_o[1]}]
BUSY_FROM_FPGA<2>	FMC_LA<14>	C18	LA14_P	R8	busy_o[2]	Out	set_property PACKAGE_PIN R8 [get_ports {busy_o[2]}]
BUSY_FROM_FPGA<3>	FMC_LA<15>	H19	LA15_P	K5	busy_o[3]	Out	set_property PACKAGE_PIN K5 [get_ports {busy_o[3]}]
DUT_CLK_FROM_FPGA<0>	FMC_LA<16>	G18	LA16_P	K3	dut_clk_o[0]	Out	set_property PACKAGE_PIN K3 [get_ports {dut_clk_o[0]}]
DUT_CLK_FROM_FPGA<1>	FMC_LA<17>	D20	LA17_P_CC	F4	dut_clk_o[1]	Out	set_property PACKAGE_PIN F4 [get_ports {dut_clk_o[1]}]
DUT_CLK_FROM_FPGA<2>	FMC_LA<18>	C22	LA18_P_CC	E2	dut_clk_o[2]	Out	set_property PACKAGE_PIN E2 [get_ports {dut_clk_o[2]}]
DUT_CLK_FROM_FPGA<3>	FMC_LA<19>	H22	LA19_P	G4	dut_clk_o[3]	Out	set_property PACKAGE_PIN G4 [get_ports {dut_clk_o[3]}]

Chapter 6

Functions

The following is a list of files containing the code for the TLU:

- `./eudaq2/user/eudet/misc/fmctlu_runcontrol.ini`:
  initialization file for the hardware. The location of the file can be passed to the EUDAQ code in the Graphic User Interface (GUI).

- `./eudaq2/user/eudet/misc/fmctlu_runcontrol.conf`:
  configuration file. It contains all the parameters to be loaded in the TLU at the beginning of the run. If this file is not found, EUDAQ will use a list of default settings. The location of the file (and its name) can be passed to the EUDAQ code in the GUI.

- `./eudaq2/user/eudet/misc/fmctlu_connection.xml`:
  define the IP address and address map of the TLU. The one listed is the default location for the file. A different location can be specified with the `ConnectionFile` option in the *conf* file for the TLU.

- `./eudaq2/user/eudet/misc/fmctlu_address.xml`:
  address map for the TLU. The location of the file is specified in the `fmctlu_connection.xml` file.

- `./eudaq2/user/eudet/misc/fmctlu_clock_config.txt`:
  configuration for the Si5345 clock chip. In order for the hardware to work a configuration file must be present. Those listed are the default name and location for the file; a different file can be specified with the `CLOCK_CFG_FILE` option in the *conf* file for the TLU.

- `./eudaq2/user/eudet/module/src/FMCTLU_Producer.cc`:
  eudaq producer for the TLU. Contains the methods to initialize, configure, start, stop the TLU producer.

- `./eudaq2/user/eudet/hardware/src/FmctluController.cc`:
  Contains the definition of the hardware class for the TLU and the methods to set and read from its hardware, such as clock chip, DAC, etc. This

lever is abstract with respect to the actual hardware, so that if a future version of the board uses different components it should be possible to re-use this code.

- `./eudaq2/user/eudet/hardware/include/FmctluController.hh`: Headers for the controller.
- `./eudaq2/user/eudet/hardware/src/FmctluController.cxx`: Executable for the controller.
- `./eudaq2/user/eudet/hardware/src/FmctluHardware.cc`: This is the code that deals with the actual hardware on the TLU, and contains specific instructions for the chips mounted in the current version. It contains several classes for the ADC, the clock chip, the I/O expanders etc.
- `./eudaq2/user/eudet/hardware/include/FmctluHardware.hh`: Header for the hardware.
- `./eudaq2/user/eudet/hardware/src/FmctluI2c.cc`: core functions used to read and write from I^2C compatible slaves.
- `./eudaq2/user/eudet/hardware/include/FmctluI2c.hh`: Headers for the I^2C core.

6.1 Functions

enableClkLEMO Enable or disable the output clock to the differential LEMO connector.

enableHDMI Set the status of the transceivers for a specific HDMI connector. When enable= False the transceivers are disabled and the connector cannot send signals from FPGA to the outside world. When enable= True then signals from the FPGA will be sent out to the HDMI.
In the configuration file use `HDMIx_on = 0` to disable a channel and `HDMI1_on = 1` to enable it (x can be 1, 2, 3, 4).
NOTE: the other direction is always enabled, i.e. signals from the DUTs are always sent to the FPGA.
NOTE: Clock source must be defined separately using SetDutClkSrc (DUTClkSrc in python script).
NOTE: this is called `DUTOutputs` on the python scripts.

GetFW dsds

getSN dsd

I2C_enable dsd

InitializeClkChip

InitializeDAC

InitializeIOexp

InitializeI2C

PopFrontEvent

ReadRRegister

ReceiveEvents

ResetEventsBuffer

SetDutClkSrc Set the clock source for a specific HDMI connector. The source can be set to 0 (no clock), 1 (Si5345) or 2 (FPGA). In the configuration file use `HDMIx_on = N` to select the source (x can be 1, 2, 3, 4, N is the clock source).
NOTE: this is called `DUTClkSrc` on python scripts.

SetPulseStretchPk Takes a vector of six numbers, packs them (5-bits each) and sends them to the PulseStretch register.

SetThresholdValue

setTrgPattern Writes two 32-bit words to define the trigger pattern for the inputs. See section 4.1 for details.

SetWRegister

SetUhalLogLevel

Chapter 7

IPBus Registers

version Returns the current version of firmware used to program the TLU

DUTINTERFACES

DUTMaskW Writing to this register allows to define which DUTs are active when in AIDA mode. The lower 4 bits of the register can be used to define the status of the DUTs: 1 for active, 0 for masked. `hdmi1` is defined by bit 0, `hdmi2` is defined by bit 1, `hdmi3` is defined by bit 2, `hdmi4` is defined by bit 3.

IgnoreDUTBusyW Writing to this register allows to ignore the busy signal from a particular DUT while in AIDA mode. The lower 4 bits are used to define the status for each device. A 1 indicates that the logic should ignore busy signals from the specific DUT.

IgnoreShutterVetoW The LSB of this register can be written to define whether the DUT should ignore the shutter veto signal. Normally, when the shutter signal is asserted the DUT reports busy. If this bit is flag the DUT will ignore the shutter signal.

DUTInterfaceModeW Write register to define the mode of operation for a DUT. Two bits per device can be used to define the mode; currently only two modes are available (AIDA, EUDET).
The bit pairs are packed from the LSB starting with `hdmi1` (bits 0, 1), `hdmi2` (bits 2, 3), `hdmi3` (bits 4, 5), `hdmi4` (bits 6, 7).

- bit pair X0: EUDET
- bit pair X1: AIDA

DUTInterfaceModeModifierW Write register. This register only affects the EUDET mode of operation. For each DUT two bits can be configured although cyrrently only the lower of the pair is considere. The bit packing

Table 7.1: IPBus register

NODE	SUBNODE	ADDRESS	MASK	PERMISSION
version		0x1		r
DUTInterfaces		**0x1000**		
	DUTMaskW	0x0		w
	IgnoreDUTBusyW	0x1		w
	IgnoreShutterVetoW	0x2		w
	DUTInterfaceModeW	0x3		w
	DUTInterfaceModeModifierW	0x4		w
	DUTInterfaceModeR	0xB		r
	DUTInterfaceModeModifierR	0xC		r
	DUTMaskR	0x8		r
	IgnoreDUTBusyR	0x9		r
	IgnoreShutterVetoR	0xA		r
Shutter		**0x2000**		
	ShutterStateW	0x0		w
	PulseT0	0x1		w
i2c_master		**0x3000**		
	i2c_pre_lo	0x0	0xFF	r/w
	i2c_pre_hi	0x1	0xFF	r/w
	i2c_ctrl	0x2	0xFF	r/w
	i2c_rxtx	0x3	0xFF	r/w
	i2c_cmdstatus	0x4	0xFF	r/w
eventBuffer		**0x4000**		
	EventFifoData	0x0		r
	EventFifoFillLevel	0x1		r
	EventFifoCSR	0x2		r/w
	EventFifoFillLevelFlags	0x3		r
Event_Formatter		**0x5000**		
	Enable_Record_Data	0x0		r/w
	ResetTimestampW	0x1		w
	CurrentTimestampLR	0x2		r
	CurrentTimestampHR	0x3		r
triggerInputs		**0x6000**		
	SerdesRstW	0x0		w
	SerdesRstR	0x8		r
	ThrCount0R	0x9		r
	ThrCount1R	0xA		r
	ThrCount2R	0xB		r
	ThrCount3R	0xC		r
	ThrCount4R	0xD		r
	ThrCount5R	0xE		r
triggerLogic		**0x7000**		
	PostVetoTriggersR	0x10		r
	PreVetoTriggersR	0x11		r
	InternalTriggerIntervalW	0x02		w
	InternalTriggerIntervalR	0x12		r
	TriggerVetoW	0x04		w
	TriggerVetoR	0x14		r
	ExternalTriggerVetoR	0x15		r
	PulseStretchW	0x06		w
	PulseStretchR	0x16		r
	PulseDelayW	0x07		w
	PulseDelayR	0x17		r
	TriggerHoldOffW	0x08		w
	TriggerHoldOffR	0x18		r
	AuxTriggerCountR	0x19		r
	TriggerPattern_lowW	0x0A		w
	TriggerPattern_lowR	0x1A		r
	TriggerPattern_highW	0x0B		w
	TriggerPattern_highR	0x1B		r
logic_clocks		**0x8000**		
	LogicClocksCSR	0x0		r/w
	LogicRst	0x1		w

is done in a manner similar to the DUTInterfaceMode. Set bit high to allow asynchronous veto using `DUT_CLK` when in EUDET mode.

DUTInterfaceModeR Read the content of the DUTInterfaceMode register.

DUTInterfaceModeModifierR Read status of the DUTInterfaceMode register.

DUTMaskR Read the status of the DUTMask register.

IgnoreDUTBusyR Read the status of the IgnoreDUTBusy register.

IgnoreShutterVetoR Read the status of the IgnoreShutterVeto word (only the last bit is meanigful).

SHUTTER

ShutterStateW The LSB of this register is propagated to the DUTs as shutter signal. This is the signal that the DUTs receive on the `cont` line.

PulseT0 Writing to this register will cause the firmware to generate a T0 signal.

I2C_MASTER This section includes registers used to talk to the I^2C bus.

i2c_pre_lo Lower part of the clock pre-scaler value. The pre-scaler is used to reduce the clock frequency of the bus and make it compatible with the I^2C slaves on the board.

i2c_pre_hi Higher part of the clock pre-scaler value.

i2c_ctrl

i2c_rxtx

i2c_cmdstatus

EVENTBUFFER

EventFifoData Returns the content of the FIFO. In the current firmware implementation the memory can hold 8192 words (32-bit).

EventFifoFillLevel Read register. Returns the number of words written in the FIFO. The lowest 14-bits are the actual data.

EventFifoCSR Read or write register. When read it returns the status of the FIFO. Five flags are returned:

- bit 0: empty. Asserted when the FIFO is empty.
- bit 1: almost empty. Asserted when one word remains in the FIFO.
- bit 2: almost full. Asserted when the FIFO can only accept one more word before becoming full.
- bit 3: full. In the current firmware the FIFO can hold 8192 words before filling up.
- bit 4: programmable full. This signal is asserted when the number of words in the FIFO is greater than or equal to the assert threshold (8181). It is de-asserted when the number of words in the FIFO is less than the negate threshold (8180).

When any value is written to this register the FIFO is reset.

EventFifoFillLevelFlags Does not do anything? REMOVE CHECK

EVENT_FORMATTER

Enable_Record_Data Read and write register. When written, CHECK
When read returns the content of the enable record word.

ResetTimestampW Write register. Writing any value to this register will cause the firmware to produce a retest timestamp signal (high for one clock cycle of clk_4x_logic). At the moment it does not seems to be connected to anything. CHECK

CurrentTimestampLR CHECK

CurrentTimestampHR CHECK

TRIGGERINPUTS

SerdesRstW Write register for the SerDes control.

- bit 0: set this bit to reset the ISERDES
- bit 1: set this bit to reset the input trigger counters
- bit 2: `s_calibrate_delay`

SerdesRstR Read register for the SerDes control.

ThrCount0R Read register. Returns the number of pulses above threshold for the trigger input.

ThrCount1R Read register. Returns the number of pulses above threshold for the trigger input.

ThrCount2R Read register. Returns the number of pulses above threshold for the trigger input.

ThrCount3R Read register. Returns the number of pulses above threshold for the trigger input.

ThrCount4R Read register. Returns the number of pulses above threshold for the trigger input.

ThrCount5R Read register. Returns the number of pulses above threshold for the trigger input.

TRIGGERLOGIC

PostVetoTriggersR Read register. Returns the number of triggers recorded in the TLU after the veto is applied. These are the triggers actually sent to the DUTs.

PreVetoTriggersR Read register. Returns the number of triggers recorded in the TLU before the veto is applied. This is used for debugging purposes.

InternalTriggerIntervalW Write the number of clock cycles to be used as period for the internal trigger generator. If this number is smaller than 5 then the triggers are disabled. Otherwise the period is number -2.

InternalTriggerIntervalR Read the value written in InternalTriggerIntervalW.

TriggerVetoW Write register. The value written to the LSB of this register is used to generate a veto signal. This can be used to put switch the TLU status: if the bit is asserted the logic will not send new triggers to the DUTs. If the bit is reset the board will process new triggers.

TriggerVetoR Read the content of the TriggerVeto register.

ExternalTriggerVetoR Read register. Bit 0 of this register reports the `veto` status (1 for veto active, 0 for no veto). The veto is active if the TLU buffer is full or if one of the DUTs is sending a veto signal.

PulseStretchW Write the stretch word for the trigger pulses. The original trigger pulses collected at a trigger input can be stretched by N cycles of the 4x clock (160 MHz, 6.25 ns). N is a number between 0 and 31. The stretched pulse is always at least as long as the original input.
The stretch values can be written in the `conf` file using the parameters `inX_STR` (X= [0 ... 5]).
The six words for the inputs are packed in a single 32-bit word written to this register according to the format shown in table 7.2.

PulseStretchR Returns the content of the PulseStretch word.

PulseDelayW Write the delay word for the trigger pulses. The original pulse is delayed by *N* clycles of the 4x clock (160 MHz, 6.25 ns). *N* is a number between 0 and 31. The six words for the inputs are packed in a single 32-bit word written to this register according to the format shown in table 7.2.
The delay values can be written in the `conf` file using the parameters `inX_DEL` (X= [0 ... 5]).

PulseDelayR Returns the content of the PulseDelay word.

TriggerHoldOffW Does not do anything? CHECK

TriggerHoldOffR Read the previous register... CHECK

AuxTriggerCountR Auxiliary trigger counter. Used for debug.

TriggerPattern_lowW Write register for the lower 32-bits of the trigger pattern. This pattern is used to select the combinations of trigger signals that produce a valid trigger in the TLU. See section 7 for details.

TriggerPattern_lowR Read register for the lower 32-bits of the trigger pattern. This pattern is used to select the combinations of trigger signals that produce a valid trigger in the TLU. See section 7 for details.

TriggerPattern_highW Write register for the higher 32-bits of the trigger pattern. This pattern is used to select the combinations of trigger signals that produce a valid trigger in the TLU. See section 7 for details.

TriggerPattern_highR Read register for the higher 32-bits of the trigger pattern. This pattern is used to select the combinations of trigger signals that produce a valid trigger in the TLU. See section 7 for details.

LOGIC_CLOCKS

LogicClocksCSR This is a read/write register. The write function is now obsolete and should be removed. Reading from this register returns the status of the PLL lock: bit 0 is the locked value of the pll (1= locked).

LogicRst Writing a 1 in the LSB of this register will reset the PLL and the clocks used by the TLU firmware. It needs to be checked for bugs.

Table 7.2: Packing scheme for values in registers used to define the pulse stretch and delay.

Register value																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	Input 5					Input 4					Input 3					Input 2					Input 1					Input 0				
x	x	b4	b3	b2	b1	b0	b4	b3	b2	b1	b0	b4	b3	b2	b1	b0	b4	b3	b2	b1	b0	b4	b3	b2	b1	b0	b4	b3	b2	b1	b0