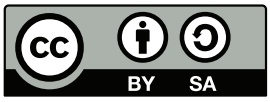

Paolo Baesso
David Cussans

AIDA Trigger logic unit (TLU v1E-F)

Friday 29th October, 2021

Documentation for FMC_TLU_v1E and FMC_TLU_v1F .
Firm(Gate)ware version 1e000026

Paolo Baesso, David Cussans - October, 2021
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An up-to-date version of this document can be found at:
https://ohwr.org/project/fmc-mtlu

Please report any errors or omissions to the authors.

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Contents

Chapter 1

Introduction

Congratulations on acquiring an AIDA-2020 TLU!
We hope that the unit will help you to collect lots of useful data during your hardware tests.
This manual describes the TLU designed for the AIDA-2020 project by David Cussans[1] and Paolo Baesso[2].
The unit is designed to be used in High Energy Physics beam-tests and provides a simple and flexible interface for fast timing and triggering signals at the AIDA pixel sensor beam-telescope.
The current version of the hardware is an evolution of the EUDET-TLU and the miniTLU and is shipped in a metal enclosure that includes an Field Programmable Gate Array (FPGA) board, the TLU Printed Circuit Board (PCB) and an additional power module: the FPGA is responsible for all the logic functions of the unit, while the PCB contains the clock chip, discriminator and interface blocks needed to communicate with other devices. The power module contains programmable Digital to Analog Converter (DAC) to power photomultipliers and Light Emitting Diode (LED) indicators.
The current version of the PCB is FMC_TLU_v1F and is designed to plug onto a carrier FPGA board like any other FPGA Mezzanine Card (FMC) mezzanine board, although its form factor does not comply with the ANSI-VITA-57-1 standard.

[1] University of Bristol, Particle Physics group
[2] University of Bristol, Particle Physics group

1.1 Reference publication for the AIDA-2020 TLU

Please consider citing the TLU reference paper in your publications. This will help us making a case to continue the support and development of the TLU. The article[3] is available open access on JINST (Journal of Instrumentation):

"The AIDA-2020 TLU: a Flexible Trigger Logic Unit for Test Beam Facilities."

BibTEX reference:

```
@article{AIDATLU_2019,
    title = {The {AIDA}-2020 {TLU}: a flexible trigger logic unit
                for test beam facilities},
    author = {P. Baesso and D. Cussans and J. Goldstein},
    doi = { 10.1088/1748-0221/14/09/p09019 },
    url = { https://doi.org/10.1088%2F1748-0221%2F14%2F09%2Fp09019 },
    journal = {Journal of Instrumentation}
    year = 2019,
    month = {sep},
    publisher = {{IOP} Publishing},
    volume = {14},
    number = {09},
    pages = {P09019--P09019},
}
```

1.2 Licences

The design information for the AIDA-2020 TLU is published with Open Source / Hardware licences in the hope that this will allow its widest possible use.

The hardware portions of this project are licenced under the CERN Permissive Open Hardware Licence.

The firmware(gateware) and software portions of this project are licenced under GPL v3.0

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1.3 Overview

The AIDA-2020 TLU provides timing and synchronization signals to test-beam readout hardware.
When used for within AIDA-2020 specifications, the hardware generates a low-jitter 40 MHz clock or can accept an external clock reference. The external reference clock frequency is not required to be 40 MHz but other

[3] doi = 10.1088/1748-0221/14/09/p09019

values require a dedicated configuration of the clock circuitry on the board. Similarly, by changing the configuration file it is possible to operate the hardware at different clock frequencies.
The TLU accepts asynchronous trigger signals from up to six external sources, such as beam-scintillators, and generate synchronous signals (including global trigger or control signals) to send to up to four Device Under Test (DUT). The logic function used to generate the trigger can be defined by the user among all the possible logic combinations of the inputs.
Depending on the chosen mode of operation, the TLU can accept busy signals or other veto signals from DUTs and react accordingly, for instance avoiding any further trigger until all the busy signals have been de-asserted.
Whenever a global trigger is generated by the unit, a 48-bit coarse time-stamp is attached to it. This time stamp is based on the internal 40 MHz clock. The unit also records a fine-grain time stamp with 1.56 ns resolution for each signal involved in the trigger decision.
The configuration parameters and data are sent and received via the IPbus protocol which provides a simple way to control and communicate TCA-based hardware via the UDP/IP protocol.
The TLU is shipped with an FPGA board already programmed with the latest version of the firmware needed to operate the unit. New features and bug fixes are continuously being implemented by the developing team and it is possible to flash the unit with a new firmware as described in section 1.6.
The internal electronics of the TLU require 12 V to operate and will dissipate about 12 W during normal operation.
Power should be provided using the socket located on the back panel. See section 1.4 and 1.4 for details on compatible connectors.

1.4 Hardware modules

The unit is provided in two different configurations: a table-top enclosure (figure 1.1) and a 19"-rack mount enclosure (figure 1.2). The difference is only cosmetic; the hardware inside the unit is identical[4] so the information contained in the rest of this document apply to both types of TLU unless otherwise specified.

Table-top unit: front panel

The front panel of the TLU is shown in figure 1.1 (top); from left to right, the main elements are:

- Small Form-factor Pluggable (SFP) cage. This port can be used to provide timing signals via optical/copper interface. Do not attempt to use

[4] With the only exception that the 19"-rack unit has and additional Liquid Crystal Display (LCD) and is powered using 220 V.

this to communicate with the TLU as the firmware does not support this mode of operation.

- 4 High-Definition Multimedia Interface (HDMI) connectors for devices under test. Each connector has a Red Green Blue (RGB) LED used to indicate the port status (see section **??**).
- 1 LEMO connector for Low Voltage Differential Signaling (LVDS) clock input/output. This is a 2-pin LEMO series 00 connector[5]. A RGB LED indicator is used to signal whether the port is configured as input or output.
- 6 LEMO Trigger inputs. These are standard 1-pin LEMO connectors[6]. Each input has a RGB LED indicator.
- 4 LEMO connectors to provide power to photomultipliers. This is a 4-pin connector with 9-mm diameter[7]. For the pin-out see section 2.5.

Note

To reduce the cost of a unit, some modules are not equipped with these connectors and the front panel holes are blanked by a plastic board.
If necessary, it is possible to solder the connectors at a later stage, since all the necessary circuitry is present. This requires disassembling the unit, removing the top cover. See section 1.7 for details.

- Green LED indicators for power (+12 V) and regulators (+5 V and -5 V). These indicators should always be lit when the unit is powered.

Table-top unit: back panel

The TLU back panel is shown in figure 1.1 (bottom); from left to right, the main elements are:

- RJ45 connector: this is the connector used to communicate with the hardware using IPBus.
- Universal Serial Bus (USB)-B port used to flash the internal logic with a new version of the firmware. See section1.6 for details.

Note

This port should be left disconnected if planning to use the self-boot capability of the internal logic. If a cable is detected, the FPGA will not load the pre-flashed firmware at power-up.

[5]Part number EPG.00.302.NLN. An example of mating part is LEMO FGG.00.302.CLAD35
[6]LEMO EPK.00.250.NN. Mates with any LEMO 00.250 connector
[7]LEMO part number EXP.0S.304.HLN. Mates with LEMO part FFA.0S.304.CLAC44 or similar.

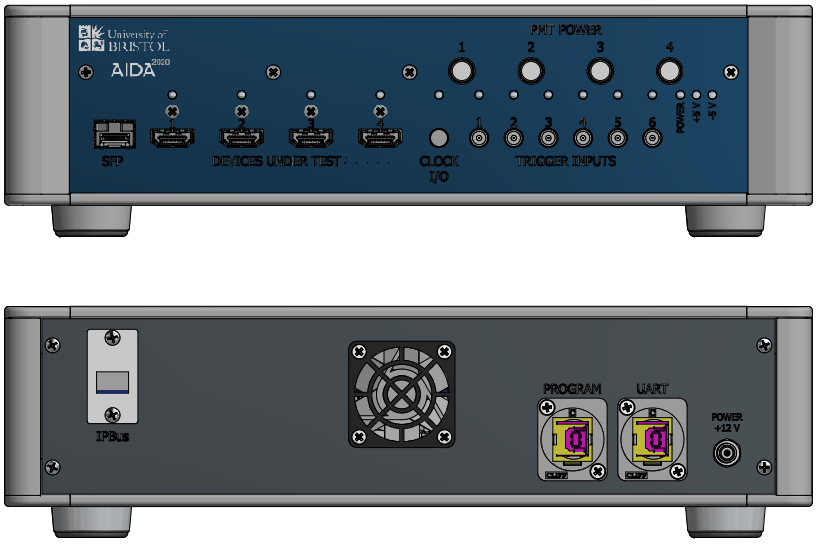


Figure 1.1: View of the table-top TLU front (top) and back (bottom) panels.

- USB-B port used to communicate with the FPGA universal asynchronous receiver-transmitter (UART) port.
- Power connector[8]. Central pin is +12 V. It is recommended to use a power supply capable of providing at least 1 A.

A cooling fan is also mounted on the back panel.

Rack mount unit: front and back panels

The front and back panels for the 19"-rack unit are shown in figure 1.2. All the components are identical to those of the table-top enclosure with the following exceptions:

- this version has a LCD used to display information.
- the unit is powered with 220 VAC (110 VAC can also be used); an internal AC-DC converter is used to provide the required 12 V (DC) to the electronics. A standard mains lead[9] is required.

[8] All TLUs shipped after 17/06/2018 use Switchcraft 721A; mates with a ϕ 5.5 mm jack with ϕ 2.5 mm central pin. For instance use Lumberg 1634 02.
TLUs shipped before that date use Switchcraft 722A instead, which mates with a ϕ 5.5 mm jack with ϕ 2.1 mm central pin. For instance use Lumberg 1633 02. Only 3 units are currently still using the 2.1 mm connector.

[9] IEC 60320 type C13.

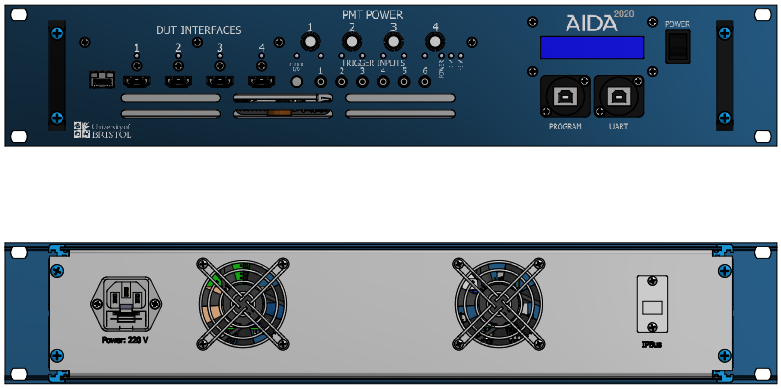


Figure 1.2: View of the 19"-rack mount TLU front (top) and back (bottom) panels.

- The USB ports are placed on the front of the unit leaving only the RJ45 and power connectors on the back.
- A power switch is located on the front panel.

1.5 Setup

At the moment of shipping, each TLU is pre-configured with the most recent version of the firmware. It is therefore possible to power the unit and start using it almost immediately. The following steps are required to use the unit:

1. Ensure no USB cable is plugged in the unit
2. Power the unit. The pre-configured firmware will automatically load.
3. Plug an Ethernet cable in the RJ45 socket located on the back panel and connect it to the computer used to run the control software. The socket is labeled `IPBus` on figure 1.1 and figure 1.2.
   Note that currently the unit uses a pre-defined IP address of 192.168.200.30. In future version of the firmware the address will be configurable. Try to ping the IP address of the unit: if the unit responds then the firmware is correctly loaded.

4. Use the control software to configure the unit. In particular, after each power up it is necessary to re-configure the clock chip. See chapter 11 for details on the software and chapter 3 for details on the clock chip.

Communication with the TLU

The only way to communicate with the unit is over IPBus protocol and via the RJ45 connector located on the back panel of the TLU.

1.6 FPGA and firmware

The firmware developed at University of Bristol is targeted to work with the Enclustra AX3 board, which must be plugged onto a PM3 base, also produced by Enclustra. The firmware is loaded on the FPGA using a Joint Test Action Group (JTAG) interface. Typically a breakout board will be required to connect the Xilinx programming cable to the Enclustra PM3. All these components are included in the TLU enclosure so the user can upload a new version of the firmware by simply connecting a USB-B cable in the back panel of the unit.
At the time of writing this document[10] the AX3 is the only FPGA for which a firmware has been developed.
Each unit is shipped with the latest version of the firmware written onto its boot loader Electrically Erasable Programmable Read-Only Memory (EEPROM); at power up, the unit will automatically retrieve the firmware from the EEPROM and program itself.

Note

If the FPGA detects a programming cable connected it will not load the firmware from its memory after a power cycle.
It is recommended to leave the USB cable disconnected from the back panel unless there is the intention to re-program the firmware.

The latest version of the firmware can be found on the project Open Hardware (OHWR) github repository (AIDA-2020 TLU - Gateware).
The user can decide to configure the unit with a new version of the firmware that will remain active until the TLU is powered off (see standard programming, described below). It is also possible to re-program the EEPROM to permanently replace the boot program with a new one (see configuration memory programming, described below).
Programming the FPGA requires the Vivado Lab Tools, available free on the on the Xilinx website[11]. Depending on the hardware installed internally, some additional drivers might be required to correctly use the JTAG cable.
At the time of writing, the preferred cable for the table-top TLU is the Digilent HS2[12]; the corresponding driver package is ADEPT 2, available on the Digilent website[13].
For the 19-inch rack mount unit, the cable used is the Trenz TE0790-02[14]. This cable is compatible with Xilinx products and does not require additional software.

[10] October, 2021
[11] https://www.xilinx.com/support/download.html
[12] https://store.digilentinc.com/jtag-hs2-programming-cable/
[13] https://reference.digilentinc.com/reference/software/adept/start
[14] https://shop.trenz-electronic.de/en/TE0790-02-XMOD-FTDI-JTAG-Adapter-Xilinx-compatible?c=318

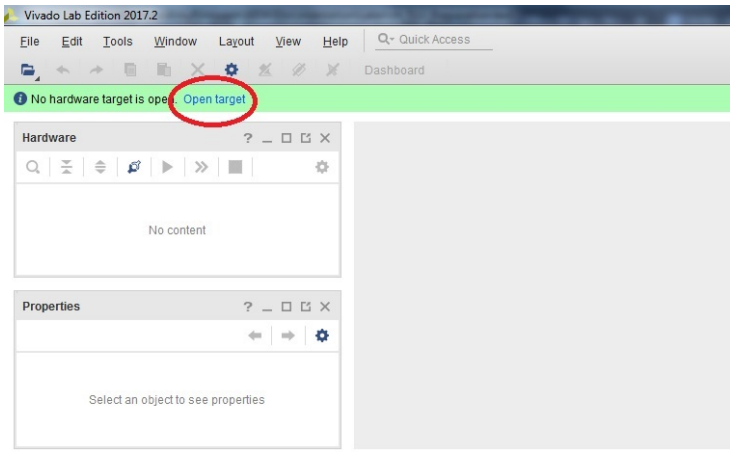


Figure 1.3: Vivado interface.

Standard programming

Updating the firmware on the TLU requires writing a bit stream file to its FPGA. This operation is performed using the left USB port located on the back panel, labelled `FPGA PROGRAMMING` in figure 1.4.
Once the Vivado tools have been installed the user should also install the drivers for the programming cable in the enclosure (see previous section for software sources).
The bit stream is provided as a `.bit` file and can be found on the firmware OHWR repository for the TLU[15].
Once these prerequisites are met, the procedure is as follows:

1. Open the Vivado tools and select "Hardware manager", figure1.3
2. Select open target
3. Identify the cable corresponding to the unit to be written and click open. The cable identifier is generally written on the back panel of the TLU. If only one programming cable is connected to the computer, it is possible to use the auto-connect option.
   Once done, the Vivado window will be populated, showing the cable and the FPGA attached to it.
4. Right click on the FPGA (typically xc7...) and select `Program device` (see figure 1.4)
5. Locate the `.bit` file to be used and program

[15] https://ohwr.org/project/fmc-mtlu-gw/wikis/Firmware%20Releases

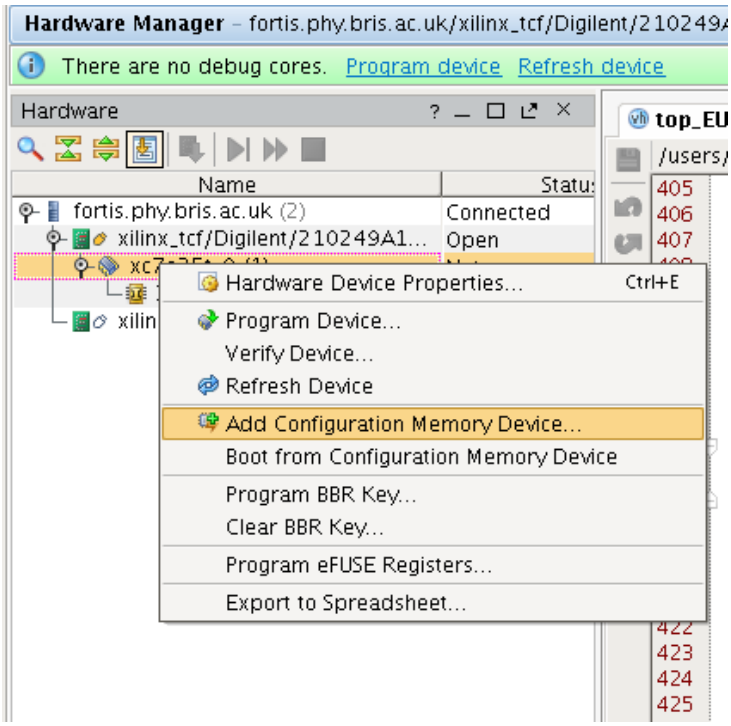


Figure 1.4: Program interface.

Configuration memory programming

The procedure to write a permanent program in the EEPROM is very similar to the one followed to write a bit stream file, with the exception that the user should select `Add configuration memory device` in the options, as shown in figure 1.4. This will open a new window, shown in figure 1.5, from which it is possible to indicate the file to use (with extension `.mcr`). Make sure that the options are set as shown in figure 1.5.
The firmware loaded this way will overwrite any pre-existing firmware and will be loaded automatically whenever the unit is powered up.

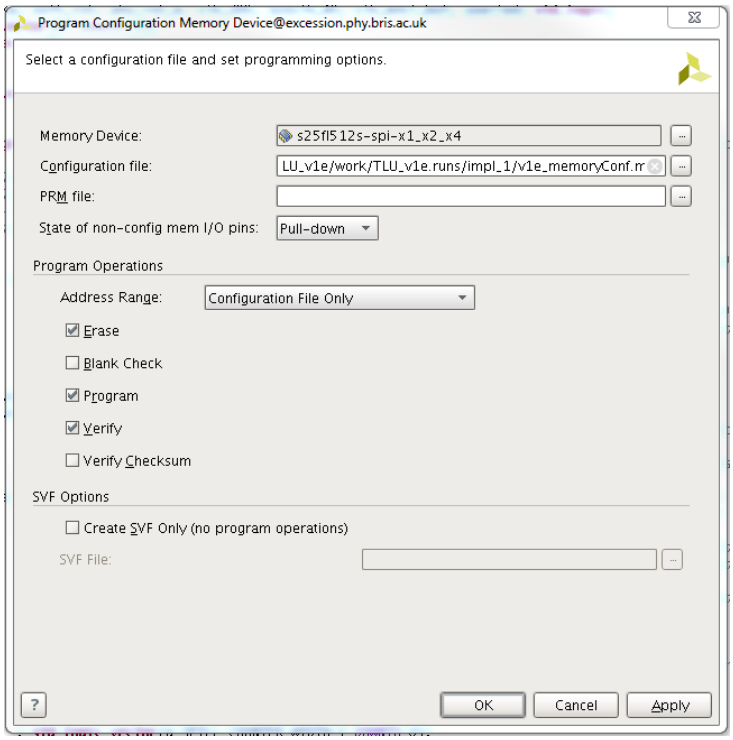


Figure 1.5: EEPROM interface. The options shown in the picture are suitable to configure the device correctly.

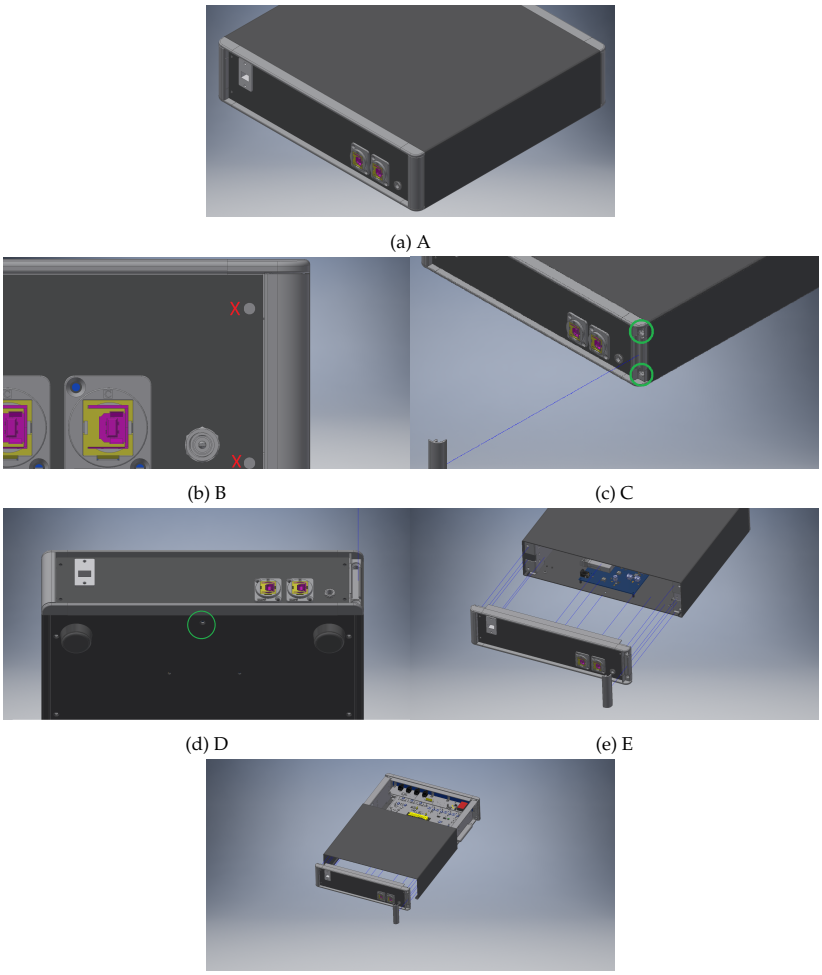
1.7 Inspection (table top unit)

Accessing the internal electronics of the unit requires removing the top cover of the enclosure; this can only slide away when either the front or back frame are removed.

Note

Simply removing the corner screws on the panels will only allow to remove the plates but not accessing the inside of the unit.

The frames are held in place by 4 screws hidden behind the corner covers.
Figure 1.6 shows the correct procedure to remove the cover:
A) the easiest way to remove the cover is by removing the back frame, rather than the front one.
B) Do not remove the corner screws in the plate.
C) Remove the two corner covers from the frame. They are only held in place by pressure and can be removed pulling by hand. Once done, remove the 4 Philips screws located behind (green circles).



(a) A

(b) B

(c) C

(d) D

(e) E

(f) F

Figure 1.6: Steps to remove the cover from the unit. The screws to take the unit apart are hidden behind the corner plates. The plates can be removed by pulling.

D) unscrew the Philips screw at the bottom of the unit holding the frame in place.
E) remove the frame and the back panel. Be careful to not damage the cables connecting the panel to the electronics.
F) Slide the top cover away.
The same procedure can be repeated with the front frame, if necessary. In this case, the user must also disconnect the front panel from the electronics by removing the countersunk screws connected to the HDMI ports and the powermodule.

1.8 Inspection (19"-rack unit)

Accessing the hardware on the 19"-unit is straightforward: simply remove the four M2.5 screws located on the top panel and slide the panel back. Please note that this unit has an internal AC-DC converter that can potentially store an harmful amount of energy even when powered-off and disconnected from the mains: always use care when accessing the unit.

Danger

Before disassembling the 19-inch rack mounted TLU disconnect the mains cable from the back and leave sufficient time for the internal capacitors to discharge.

Chapter 2

TLU Hardware

Board FMC_TLU_v1F is an evolution of the miniTLU designed at the University of Bristol (UoB). The board shares a few features with the miniTLU but also introduces several improvements. This chapter illustrates the main features of the board to provide a general view of its capabilities and an understanding of how to operate it in order to communicate with the DUTs.

2.1 Inputs and interfaces

FMC

The board must be plugged onto a FMC carrier board with an FPGA in order to function correctly. The connection is achieved using a low pin count FMC connector. The list of the pins used and the corresponding signal within the FPGA are provided in appendix at page 69.
In normal conditions (such as a test beam) this connector is not accessible to users.

Device under test

The DUTs are connected to the TLU using standard size HDMI connectors[1].
In the current version of the hardware, up to four DUTs can be connected to the board. In this document the connectors will be referred to as `HDMI1`, `HDMI2`, `HDMI3` and `HDMI4`.
The connectors operate with 3.3 V LVDS signals and are bi-directional, i.e. any differential pair can be configured to be an output (signal from the TLU to the DUT) or an input (signals from the DUT to the TLU) by using half-duplex line transceivers. Figure 2.2 illustrates how the differential pairs are connected to the transceivers.

[1] In the miniTLU hardware these were mini HDMI connectors.

HDMI PIN	HDMI Signal Name	Enable Signal Name
1	HDMI_CLK	ENABLE_CLK_TO_DUT or ENABLE_DUT_CLK_FROM_FPGA
2	GND	–
3	HDMI_CLK *	ENABLE_CLK_TO_DUT or ENABLE_DUT_CLK_FROM_FPGA
4	CONT	ENABLE_CONT_FROM_FPGA
5	GND	–
6	CONT*	ENABLE_CONT_FROM_FPGA
7	BUSY	ENABLE_BUSY_FROM_FPGA
8	GND	–
9	BUSY*	ENABLE_BUSY_FROM_FPGA
10	SPARE	ENABLE_SPARE_FROM_FPGA
11	GND	–
12	SPARE*	ENABLE_SPARE_FROM_FPGA
13	n.c.	
14	HDMI_POWER	–
15	TRIG	ENABLE_TRIG_FROM_FPGA
16	TRIG*	ENABLE_TRIG_FROM_FPGA
17	GND	
18	n.c.	
19	n.c.	

Table 2.1: HDMI pin connections.

Note

The input part of the transceiver is configured to be always on. This means that signals going *into* the TLU are always routed to the logic (FPGA). By contrast, the output transceivers have to be enabled and are off by default: signal sent from the logic to the DUTs cannot reach the devices unless the corresponding enable signal is active.

Table 2.1 shows the pin naming and the corresponding output enable signal. The clock pairs have two different enable signals to select the clock source (see section 3 for more details). In general only one of the clock sources should be active at any time.
The enable signals can be configured by programming two General Purpose Input/Output (GPIO) bus expanders via Inter-Integrated Circuit (I^2C) interface as described in section 2.4. Figure 2.1 illustrates the position of each pin within the HDMI connector.

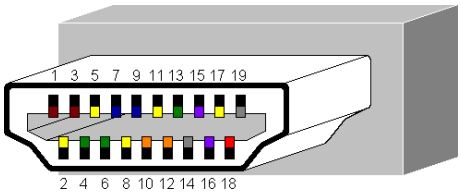


Figure 2.1: HDMI Pin Numbering (plug shown)

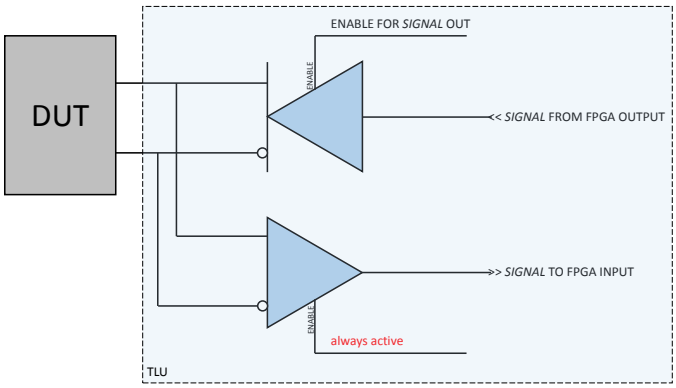


Figure 2.2: Internal configuration of the HDMI pins for the DUTs. The path from the DUT to the FPGA is always active. The path from the FPGA to the DUT can be enabled or disabled by the user.

In terms for functionalities, the four HDMI connectors are identical with one exception: the clock signal from `HDMI4` can be used as reference for the clock generator chip mounted on the hardware. For more details on this functionality refer to section 3.

SFP cage

FMC_TLU_v1F hosts a SFP cafe and a Clock and Data Recovery (CDR) chip that can be used to decode a data stream or to issue timing signals over optical/copper interface. The data from the stream is routed to the FPGA while the clock can be fed to the on-board clock chip to be used as a clock reference.

2.2 Clock LEMO

The board hosts a two-pin LEMO connector that can be used to provide a reference clock to the clock generator (see section 3) or to output the clock from the TLU to the external world, for instance to use it as a reference for another TLU. The signal level is 3.3 V LVDS.
As for the differential pairs of the DUTs, the pins of this connector are wired to a transceiver configured to always accept the incoming signals. The outgoing

Table 2.2: DAC outputs and corresponding threshold inputs.

	Output	
	DAC2(Ic2)	**DAC1 (Ic1)**
Threshold 0	1	
Threshold 1	0	
Threshold 2		3
Threshold 3		2
Threshold 4		1
Threshold 5		0

direction must be enabled by using the `ENABLE_CLK_TO_LEMO` signal, which can be configured using the bus expander described in in section 2.4.

2.3 Trigger inputs

Board FMC_TLU_v1F can accept up to six trigger inputs over the LEMO connectors labelled `IN_1`, `IN_2`, `IN_3`, `IN_4`, `IN_5` and `IN_6`. The FMC_TLU_v1F uses internal high-speed[2] discriminators to detect a valid trigger signal. The voltage thresholds can be adjusted independently for each input in a range from -1.3 V to +1.3 V with 40 μV resolution.
The adjustment is performed by writing to two 16-bit DACs via I^{2}C interface as described in section 2.4.
The DACs can either use an internal reference voltage of 2.5 V or an external one of 1.3 V provided by the TLU: it is recommended to choose the external one by configuring the appropriate register in the devices. This is the default option when operating within the AIDA2020 framework.
The correspondence between DAC slave and thresholds is shown in table 2.2.

2.4 I^{2}C slaves

The I^{2}C interface on the FMC_TLU_v1F can be used to configured several features of the board.
Table 2.3 lists all the valid addresses and the corresponding slave on the board. The Enclustra lines refer to slaves located on the PM3 board; these slaves can be ignored with the exception of the bus expander. The Enclustra expander is used to enable/disable the I^{2}C lines going to the FMC connector.

[2] 500$\pm$30 ps propagation delay.

Table 2.3: I²C addresses of the TLU.

CHIP	ID	FUNCTION	ADDRESS
IC1	AD5665RBRUZ	DAC1	0x1F
IC2	AD5665RBRUZ	DAC2	0x13
IC5	24AA025E48T	EEPROM	0x50
IC6	PCA9539PW	I2C Expander1	0x74
IC7	PCA9539PW	I2C Expander2	0x75
IC8	ADN2814ACPZ	CDR	0x60
IC8_9	Si5345A	Clock Generator	0x68
Enclustra slaves			
		Enclustra Bus Expander	0x21
		Enclustra System Monitor	0x21
		Enclustra EEPROM	0x54
		Enclustra slave	0x64

Note

After a power cycle the Enclustra expander is configured to disable the I²C interface pins. This means that it is impossible to communicate to any I²C slave on the TLU until the expander has been enabled.
The interface is enable by setting bit 7 to 0 on register 0x01 of the Enclustra expander.

Once the interface is enabled it is possible to read and write to the devices listed in the top part of table 2.3.
The user should reference the manual of each individual component to determine the register that must be addressed. The rest of this section is meant to provide an overview of the slave functionalities.

DAC

Each DAC has four outputs that can be configured independently. `DAC1` is used to configure the thresholds of the first four trigger inputs; `DAC2` configures the remaining two thresholds.
The DACs should be configured to use the TLU voltage reference of 1.3 V. In these conditions, writing a value of 0x00000 to a DAC output will set the corresponding threshold to -1.3 V while a value of 0xFFFF will set it to +1.3 V.

EEPROM

The EEPROM located on the board contains a factory-set unique number, used to identify each FMC_TLU_v1F unequivocally. The number is comprised of six bytes written in as many memory locations.

The identifier is always in the form: `0xD8 80 39 XX XX XX` with the top three bytes indicating the manufacturer and the bottom three unique to each device.

Bus expander

The expanders are used as electronic switched to enable and disable individual lines. Each expander has two 8-bit banks; the values of the bits, as well as their direction (input/output) can be configured via the I^2C interface. For the purpose of the TLU, all the expander pins should be configured as outputs since they must drive the enable signals on the DUT transceivers.

Clock and data recovery chip

The CDR is used in conjunction with the SFP cage to recover data and clock from the incoming bit stream. The functionality has not yet been implemented in the firmware so the I^2C slave can be ignored for now.

Clock generator

The clock for FMC_TLU_v1F can be generated using various external or internal references (see section 3 for further details). In order to reduce any jitter from the clock source and to provide a stable clock, the board hosts a Si5345 clock generator that needs to be configured via I^2C interface.
The configuration involves writing ∼380 register values. A configuration file, containing all the register addresses and the corresponding values, can be generated using the ClockBuilder tool available from Silicon Labs.
The registers addresses between 0x026B and 0x0272 contain user-defined values that can be used to identify the configuration version: it is advisable to check those registers and check that they contain the correct code to ensure that the chip is configured according to the TLU specifications. As an indication, files generated for the current version of the TLU should have a configuration identifier in the form `TLU1E_XX`, where `XX` is a sequential number.

TLU Producer

When using the TLU producer to configure hardware, the location of the configuration file can be specified by setting the `CLOCK_CFG_FILE` value in the *conf* file for the producer.
If no value is specified, the software will look for the configuration file `../conf/confClk.txt` i.e. if the `euRun` binary file is located in `./eudaq/bin`, then the default configuration file should reside in `./eudaq/conf`. The configuration will produce an error if the file is not found.

2.5 Power module and led

The LEDs and Photo Multiplier Tube (PMT) connectors on the front panel are part of an auxiliary board installed together with the FMC_TLU_v1F . All the functionalities on the board, such as the indicators and the DAC are controlled via I^2C bus.
Is the TLU is controlled using EUDAQ, the DAC can be steered by means of a parameter in the configuration file (see section 10 for details).
Three green LED on the front panel are used to indicate the presence of power (+12 V) and the correct functioning of the +5 V and -5 V voltage regulators. Further indicators are assigned to the HDMI and trigger inputs to provide information on their status. These indicators are RGB. At the moment there is not defined scheme to assign a meaning to each colour.
The LEMO connectors used to power the PMTs are wired according to the following scheme, inherited from what already in use in beam telescopes:

1. POWER: +12 V
2. not connected
3. CONTROL, voltage signal from 0 to +1 V
4. GND

TLU Control voltage on modified units

Some users requested the possibility to use different types of PMTs. To enable this, a few power modules have been modified to provide +5 V (instead of +12 V) and to have a maximum control voltage of 1.1 V (instead of 1 V).
The modified units are clearly labelled and use different style of PMT connectors, so that confusion should be minimized.

Chapter 3

Clock

The TLU can use various sources to produce a stable 40 MHz clock as required in the AIDA-2020 application[1].
The board hosts a high performance jitter attenuator/cleaner chip, the Si5345A.
A Low-voltage Positive Emitter-Coupled Logic (LVPECL) crystal provides a reference 50 MHz clock for the Si5345A. In conjunction with the reference clock, the Si5345A can accept up to four clock sources and use them to generate the required output clocks distributed to the various DUTs.
In FMC_TLU_v1F the possible sources are: differential LEMO connector LM1_9, one of the four HDMI connectors (`HDMI4`), a CDR chip connected to the SFP cage. The fourth input is used to provide a zero-delay feedback loop.
The low-jitter clock generated by the Si5345A can be distributed to up to ten recipients. In the TLU these are: the four DUTs via HDMI connectors, the differential LEMO cable, the FPGA, connector J1 as a differential pair (pins 4 and 6) and as a single ended signal (pin 8). The final output is connected to the zero-delay feedback loop. Note that it is possible to program the clock chip to generate a different frequency for each of its outputs.
The DUTs can receive the clock either from the Si5435A or directly from the FPGA: when provided by the clock generator, the signal name is `CLK\_TO\_DUT` and is enabled by signal `ENABLE_CLK_TO_DUT`; when the signal is provided directly from the FPGA the line used is `DUT_CLK_FROM_FPGA` and is enabled by `ENABLE_DUT_CLK_FROM_FPGA`.
The firmware uses the clock generated by the Si5345A except for the block `enclustra_ax3_pm3_infra` which relies on a crystal mounted on the Enclustra board to provide the IPBus functionalities (in this way, at power up the board can communicate via IPBus even if the Si5345A is not configured).

[1] For some applications a 50 MHz clock will be required instead

Table 3.1: Si5345 Input Selection Configuration.

Register Name	Hex Address [Bit Field]	Function
CLK_SWITCH_MODE	0x0536[1:0]	Selects manual or automatic switching modes. Automatic mode can be revertive or non-revertive. Selections are the following: 00 Manual 01 Automatic non-revertive 02 Automatic revertive 03 Reserved
IN_SEL_REGCTRL	0x052A [0]	0 for pin controlled clock selection 1 for register controlled clock selection
IN_SEL	0x052A [2:1]	0 for IN0 1 for IN1 2 for IN2 3 for IN3 (or FB_IN)

3.1 Input selection

The Si5345A has four inputs that can be selected to provide the clock alignment; the selection can be automatic or user-defined. For further details on this aspect the user should consult the chip documentation[2].

3.2 Logic clocks registers

LogicClocksCSR: in the new TLU the selection of the clock source is done by programming the Si5345A. As a consequence, there is no reason to write to this register. Reading it back returns the status of the PLL on bit 0, so this should read 0x1.

[2]https://www.silabs.com/documents/public/data-sheets/Si5345-44-42-D-DataSheet.pdf

Chapter 4

DUT Signals

In the older, EUDET, version of the TLU the direction of the signals on the `HDMI*` connectors were pre-defined. The new hardware has the ability to switch each LVDS pair between input and output.
The function and direction of each LVDS pair depends on the interface mode chosen.
Section 4.1 describes the different interface modes in more detail. See chapter 2.1 for details of how LVDS pairs are mapped onto physical HDMI pins.

4.1 Interface Modes

When operating within the AIDA2020 scope, the TLU can be operated in one of four different handshake modes, described in the remaining of this chapter.

Trigger/Busy (EUDET) Mode

This mode is designed to allow the TLU and DUT clocks to be asynchronous and to have any frequency relationship.
After the TLU detects an input trigger, the TRIGGER signal to the DUT is asserted and the TLU vetoes further triggers.
The DUT responds by asserting the BUSY line to the TLU. The TLU detects that the BUSY line has been asserted and responds by de-asserting the trigger line. Finally the DUT responds by de-asserting the BUSY line.
When the TLU detects that the BUSY has been de-asserted it re-enables triggers.
Figure 4.1 shows signal timing for this interface mode.

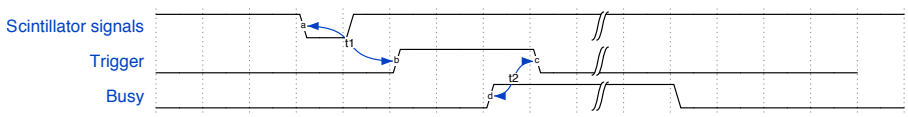


Figure 4.1: Trigger/Busy Interface Mode Timing

Trigger/Busy Handshake With Trigger Number

This interface mode is an extension of the Trigger/Busy handshake.
After the DUT detects that the TLU has de-asserted the TRIGGER line it can cause the TLU to clock out the current trigger number by toggling the DUT clock line. The number is clocked Least Significant Bit (LSB) first.
Figure 4.2 shows the signal timing for this interface mode.

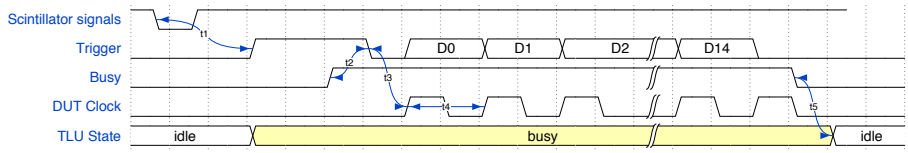


Figure 4.2: Trigger/Busy Interface Mode With Trigger Number

This mode of operations is enabled by setting the DUTMaskMode flag for the specific DUT to 0b00. See section 10.2 for details.

Synchronous (AIDA) Mode

In synchronous mode (also known as AIDA mode) the TLU sends a clock (by default 40MHz) to the DUT.
When the TLU produces a trigger, the trigger line from TLU to DUT is asserted for one cycle of the clock. In order to synchronize time-stamps between TLU to DUT a single cycle timestamp reset signal is issued at the start of each run.
The DUT can veto triggers at any point by asserting the BUSY line.
Figure 4.3 shows the signal timing for this interface mode.

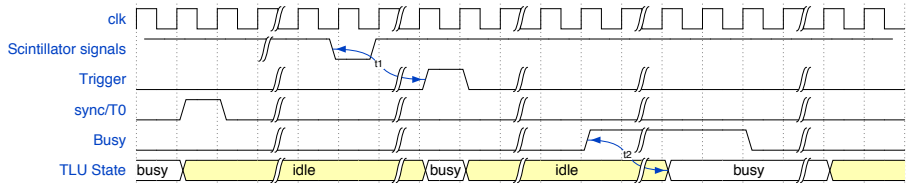


Figure 4.3: Synchronous (AIDA) Interface Mode

This mode of operations is enabled by setting the DUTMaskMode flag for the specific DUT to 0b11. See section 10.2 for details.

Synchronous Mode With Trigger Number

This is a modification of the synchronous/AIDA mode.
Immediately after the TLU issues a trigger, it clocks out the trigger number (LSB first) on the Sync/T0 line.
Figure 4.4 shows the signal timing for this interface mode.
This mode of operations is enabled by setting the DUTMaskMode flag for the specific DUT to 0b01. See section 10.2 for details.

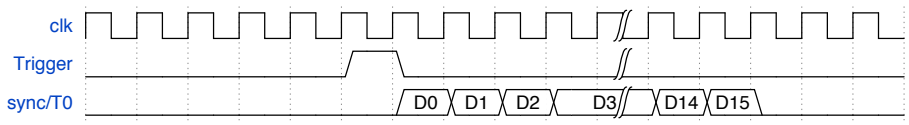


Figure 4.4: Synchronous (AIDA) Interface Mode With Trigger Number

Chapter 5

Trigger inputs

The six inputs on the TLU can be used to generate a global trigger that is then issued to all the DUTs.
Each input has a programmable voltage discriminator that can be configured in the range [-1.3 : +1.3] V.
All the inputs are protected by clamping diodes that limit the input voltage in the range [-5 : +5] V.
The discriminators are followed by edge-finding and Time to Digital Converter (TDC) logic. Currently only negative edges are registered. A future firmware version will implement user-selectable positive or negative edge detection.
The output of the edge finding logic is fed into logic to stretch and delay the pulses by a controllable amount. The stretched and delayed trigger pulses are fed into a look-up table that generates the triggers. Figure 5.1 illustrates the path of the trigger signals through the TLU.

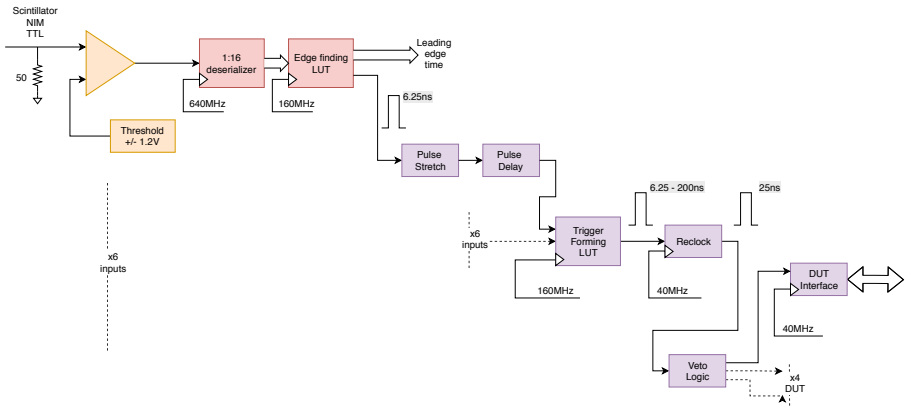


Figure 5.1: Trigger path in TLU

5.1 Trigger logic

The TLU has six trigger inputs than can be used to generate a valid trigger event. The number of possible different trigger combinations is $2^6 = 64$ so a 64-bit word can be used to decide the valid combinations. In the hardware the 64-bit word is split into two 32-bit words (indicated as Most Significant Bit (MSB) and LSB word) and the rules to generate the trigger can be specified by the user by writing in the two 32-bit IPBus registers `TriggerPattern_highW` and `TriggerPattern_lowW`: the first stores the 32 most significative bits of the trigger word, the latter stores the least significative bits.
The user can select any combination of the trigger inputs and declare it a valid trigger pattern by setting a 1 in the corresponding trigger configuration word. Multiple 1s indicate that the corresponding patterns are OR-ed.
Tables 5.1 and 5.2 show an example of how to determine the trigger configuration words: whenever a valid trigger combination is encountered, the user should put a 1 in the corresponding row under the PATTERN column. The pattern thus obtained is the required word to write in the configuration register.
It is important to note that this solution allows the user to set veto pattern as well: for instance if only word 31 from table 5.1 were picked, then the TLU would only register a trigger when the combination $\overline{I_5} * I_4 * I_3 * I_2 * I_1 * I_0$ was presented at its inputs. In other words, in this specific case I_5 would act as a veto signal and the TLU would **not** produce a global trigger if I_5=1.

The default configuration in the firmware is Hi= 0xFFFFFFFF, Low= 0xFFFEFFFE, which means that as long as any trigger input fires, a trigger will be generated. These words are loaded in the FPGA every time a new image is programmed.

Trigger logic definition

The user should pay attention to what trigger logic they want to define in order to avoid confusion in the data.
A "1" in the logic table means that the corresponding input must be active to produce a valid trigger. Similarly, a "0" indicates that the corresponding input must be inactive (i.e. is a veto, not an ignore). Any change in input configuration will cause the logic to re-assess the trigger status.
Section **??** provides a few examples.

DEC	I5	I4	I3	I2	I1	I0	PATTERN	CONFIG. WORD		2^n
0	0	0	0	0	0	0	0 0	0	LOWEST 32-bits	1
1	0	0	0	0	0	1	0 0			2
2	0	0	0	0	1	0	0 0			4
3	0	0	0	0	1	1	0 0			8
4	0	0	0	1	0	0	0 0	0		16
5	0	0	0	1	0	1	0 0			32
6	0	0	0	1	1	0	0 0			64
7	0	0	0	1	1	1	0 0			128
8	0	0	1	0	0	0	0 0	0		256
9	0	0	1	0	0	1	0 0			512
10	0	0	1	0	1	0	0 0			1024
11	0	0	1	0	1	1	0 0			2048
12	0	0	1	1	0	0	0 0	0		4096
13	0	0	1	1	0	1	0 0			8192
14	0	0	1	1	1	0	0 0			16384
15	0	0	1	1	1	1	0 0			32768
16	0	1	0	0	0	0	0 0	0		65536
17	0	1	0	0	0	1	0 0			131072
18	0	1	0	0	1	0	0 0			262144
19	0	1	0	0	1	1	0 0			524288
20	0	1	0	1	0	0	0 0	0		1048576
21	0	1	0	1	0	1	0 0			2097152
22	0	1	0	1	1	0	0 0			4194304
23	0	1	0	1	1	1	0 0			8388608
24	0	1	1	0	0	0	0 0	0		16777216
25	0	1	1	0	0	1	0 0			33554432
26	0	1	1	0	1	0	0 0			67108864
27	0	1	1	0	1	1	0 0			134217728
28	0	1	1	1	0	0	0 0	8		268435456
29	0	1	1	1	0	1	0 0			536870912
30	0	1	1	1	1	0	1 0			1073741824
31	0	1	1	1	1	1	1			2147483648

Table 5.1: Example of configuration word for the least significative bits of the trigger registers: the only valid configuration is represented by $\overline{I_5} + I_4 + I_3 + I_2 + I_1 + I_0$, i.e. a trigger is accepted if all the inputs, except I_5, present a logic 1 at the same time. The user would then write the resulting word 0x80000000 in the TriggerPattern_lowW register.

DEC	I5	I4	I3	I2	I1	I0	PATTERN	CONFIG. WORD		2^n
32	1	0	0	0	0	0	0 0 0 0 0 0	0	HIGHEST 32-bits	1
33	1	0	0	0	0	1				2
34	1	0	0	0	1	0				4
35	1	0	0	0	1	1				8
36	1	0	0	1	0	0	1 1 1 1 0 0	F		16
37	1	0	0	1	0	1				32
38	1	0	0	1	1	0				64
39	1	0	0	1	1	1				128
40	1	0	1	0	0	0	0 1 0 1 0 0	A		256
41	1	0	1	0	0	1				512
42	1	0	1	0	1	0				1024
43	1	0	1	0	1	1				2048
44	1	0	1	1	0	0	0 0 0 0 0 0	0		4096
45	1	0	1	1	0	1				8192
46	1	0	1	1	1	0				16384
47	1	0	1	1	1	1				32768
48	1	1	0	0	0	0	0 0 0 0 0 0	0		65536
49	1	1	0	0	0	1				131072
50	1	1	0	0	1	0				262144
51	1	1	0	0	1	1				524288
52	1	1	0	1	0	0	0 0 0 0 0 0	0		1048576
53	1	1	0	1	0	1				2097152
54	1	1	0	1	1	0				4194304
55	1	1	0	1	1	1				8388608
56	1	1	1	0	0	0	0 0 0 0 0 0	0		16777216
57	1	1	1	0	0	1				33554432
58	1	1	1	0	1	0				67108864
59	1	1	1	0	1	1				134217728
60	1	1	1	1	0	0	1 0 0 0 0 0	8		268435456
61	1	1	1	1	0	1				536870912
62	1	1	1	1	1	0				1073741824
63	1	1	1	1	1	1				2147483648

Table 5.2: Example of the most significative word of the register: a valid trigger is obtained when the inputs show the same configuration as row DEC 36, 37, 38, 39, 41, 43 and 63. These configuration are in logic OR with that presented in table 5.1. The resulting configuration word is 0x80000AF0.

Bit 0 meaning

A 1 in the lowest bit of the LSB word indicates that $\overline{I_5} * \overline{I_4} * \overline{I_3} * \overline{I_2} * \overline{I_1} * \overline{I_0}$ is a valid trigger combination, so the TLU will produce a trigger when all the inputs are inactive (i.e. even if all the inputs are unplugged).
Except for a few very specific cases, this is generally not a desirable behaviour.

Trigger configuration helper script

A lightweight script is available to help configuring the TLU trigger.
The file can be found in the:
`./Documentation/Misc`
folder of the OHWR documentation repository (AIDA-2020 TLU).
The script is written in Python 3.x and it should be possible to run it in standalone mode on any machine by simply using the command
`Python trigger_configuration_helper`
This will create an interactive shell; when started, the shell will ask a series of questions to the user and then generates the two 32-bit words that need to be written in the trigger registers.
The script is only meant to be a quick and simple way to generate the configuration words without having to dwell too much in the details provided in section 5.1. This means that it can only offer a limited set of configurations that should, nonetheless, be enough for most of the user cases.
To take advantage of the full flexibility of the TLU trigger and generate more advanced configurations (such as mutually excluding trigger inputs) the user should refer to section 5.1.
To use the script:

- In the script folder, type `Python trigger_configuration_helper`. This will open an interactive shell. The shell supports tab-autocompletion.
- In the shell, type `start`
- For each of the LEMO trigger inputs, specify if the signal is to be considered ACTIVE or VETO. Active signals must be asserted to create a valid trigger. VETO signals must be de-asserted to create a valid signal. There is also the option to set an input as DO-NOT-CARE (DNC): these inputs are not taken into account for the purpose of trigger generation but they are still time-stamped if asserted.
  The DNC option can be useful if the user want to connect signals that are not part of the trigger generation but for which it is required to register the status and the time-stamp whenever a valid trigger is produced.
  The DNC option can be used for any unconnected input.
  The VETO option should be used, for instance, for any inputs that is used as a shutter signal (see section 6).

- If more than one active input is present, it is possible to configure the TLU to generate a trigger if at least N are asserted (as opposed to all of them). The shell will ask for the minimum number of ACTIVE signals that should be asserted, at the same time, to generate a valid trigger.
- The shell will produce a list of all the configurations that will produce a valid trigger, followed by the two values to be written in the registers.
- If the user is happy with those, they can just copy those values and use them to configure the TLU for instance by including them in the EUDAQ configuration file. It is always possible to restart the procedure by typing `start` again.
- Please note that a VETO signal is always prioritized: if a VETO signal is asserted, the TLU will not produce any trigger.
- Also note that a DNC signal, even if asserted, does not contribute to the count of the minimum number of active inputs N.

Warning

The script only tells the user what values to write in the trigger configuration registers, but does not write them itself.
It is up to the user to program the TLU with those values, in whichever method is preferred (EUDAQ, Python scripts, etc).

Example of trigger configurations

In this example we have connected a pulse generator to two inputs of the TLU, namely `IN_1` and `IN_5`. The inputs fire with a small, random delay with respect to each other.
In order to ensure that the signals overlap adequately, we use the *stretch* register (see chapter 5.1) to increase the length of the pulses: we extend *in0* to 10 clock cycles and *in4* to 8 clock cycles, where the clock has a frequency of 160 MHz. The resulting signals are shown in figure 5.2.
We can now define the trigger logic to be used to assert a valid trigger: we only consider the lower 32-bits of the trigger word and see how different values can produce very different results.

- Trigger LSB word= 0x00020000. This indicates that the only valid trigger combination occurs when both `IN_1` and `IN_5` are high. The valid trigger goes high 1 clock cycle after this condition is met and remains high up to 1 clock cycle after the condition is no longer valid. This is illustrated in figure 5.3.

- Trigger LSB word= 0x00020002. This indicates that a valid trigger is achieved in two separated configurations (in logic OR): when both

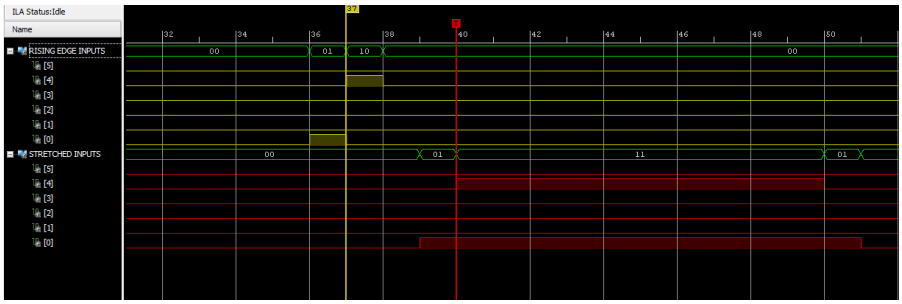


Figure 5.2: Input pulses (yellow) and corresponding stretched signals (red). Input 0 is stretched by 10 cycles, input 4 by 8, hence the difference in pulse widths.

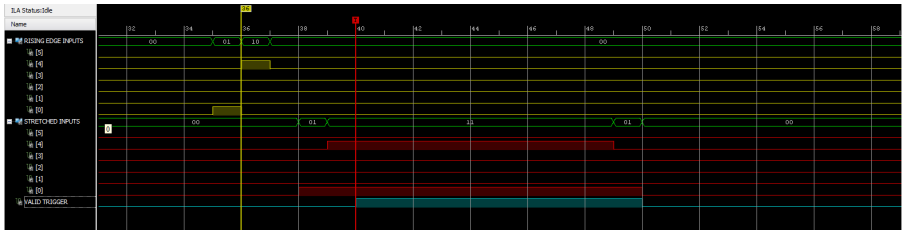


Figure 5.3: Trigger configuration 0x00020000. The valid trigger (blue) is asserted only when both signals are high. This condition occurs at frame 39. The trigger is asserted on the following frame.

inputs are high at the same time (as in the previous case) or if `IN_1` is active on its own. This is illustrated in figure 5.4. It can be seen that the valid trigger is asserted immediately one clock cycle after `IN_1` is high and remains high as long as this condition is met. One might assume that specifying the combination with `IN_5` is redundant, but the following example should show that this is not the case.

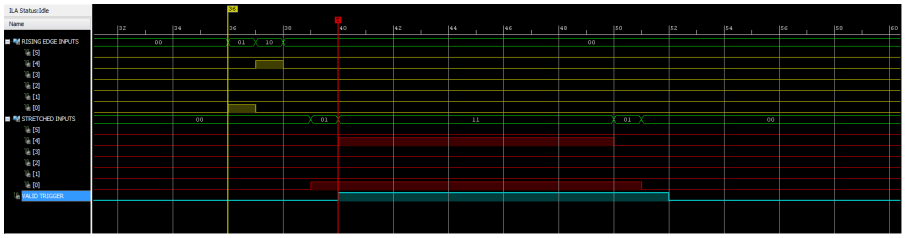


Figure 5.4: Trigger configuration 0x00020002. The valid trigger (blue) is asserted if `IN_1` is high OR when `IN_1` and `IN_5` are both high at the same time.

- Trigger LSB word= 0x00000002. This indicates that the only valid configuration is the one where only `IN_1` is high. It is important to understand that in this configuration all other inputs act as veto. This

might produce unexpected results if the user is not careful[1].
In figure 5.5 it is possible to see that the logic produces two separated trigger valid pulses, both shorter than the ones in previous examples: the first one is due to `IN_1` going high while `IN_5` is low. As soon as `IN_5` goes high, the trigger condition is no longer met. When `IN_5` returns low, a trigger condition is met again because `IN_1` is still high. In this specific case, the double pulse is caused by the different width of the pulses.

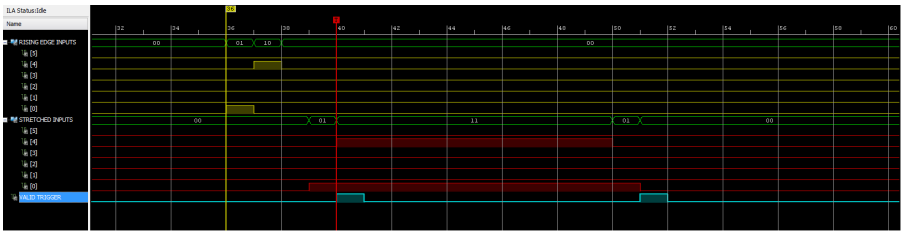


Figure 5.5: Trigger configuration 0x00000002. The valid trigger (blue) is asserted only when `IN_1` is active on its own. As such, two separated trigger pulses are produced because `IN_5` goes high and returns low before `IN_1`.

5.2 Stretch and delay

The trigger logic is designed to detect edge transitions[2] at the trigger inputs and produce a pulse for each transition detected.
The pulse has an initial duration of one clock cycle (f= 160 MHz, one cycle 6.25 ns) and occurs on the next rising edge of the 160 MHz internal clock.
Each pulse can be stretched and delayed in integer numbers of clock cycles (25 ns by default) to compensate for differences in cable length. Two separate 5-bit registers are used for the task: the value written in the registers will stretch/delay the pulse by a corresponding number of clock cycles.
Diagram 5.6 shows the effect of the delay and stretch words on the trigger logic.
Further details on how to configure the stretch and delay values are provided in section 10.

[1] Specifically, pulse stretch, pulse delay and trigger logic must be configured correctly to avoid unwanted results.

[2] By default transitions from low voltage to high voltage are detected (e.g. the leading edge of TTL pulses). The bottom 6 bits of IPBus (IPBus) register InvertEdgeW can be used to select triggering on high voltage to low voltage transitions (e.g. NIM pulses, PMT pulses)

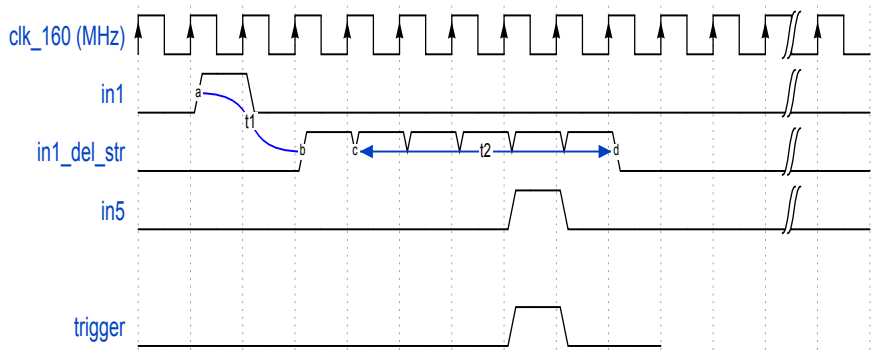


Figure 5.6: Effect of the stretch and delay values. In1 is delayed by 2 clock cycles (t1= 12.5 ns) and stretched by 5 clock cycles (t2= 31.25 ns) to create a coincidence window with in5 and produce the resulting trigger signal.

Chapter 6

Shutter

An optional "shutter" can be enabled to synchronize the acquisition window to a signal, such as the spill signal from a beam line.
When the shutter is "closed" triggers are vetoed and no triggers are issued from the TLU. When the shutter is "open" triggers can be generated and sent to active DUTs.
The shutter cycle can either be started by an external signal or synchronized by a counter clocked by the system clock (i.e. internally-generated shutter, which can be used to debug hardware).
The external signal, if used, must be connected to one of the six LEMO trigger inputs.

Warning

If the external signal is used, an appropriate threshold should be set to the corresponding input. The input used for synchronizing the shutter should not be used in the trigger mask.

Figure 6.1 illustrates the timing of the shutter sequence.
When the shutter is open, the TLU will assert the `CONT` line (see table 2.1), indicating to the DUT that the sequence is active.
Behaviour of the shutter is controlled by the IPBus registers described in table 6.1. If using EUDAQ, the registers can be written by including the corresponding steering parameters. In this case, the easiest way to avoid potential conflict between the shutter signal and the trigger input is to connect the shutter input to LEMO 6 and then setting `trigMaskHi= 0x0`. This means that the corresponding input is never involved in a valid active word. See section 5.1 for details.
The parameters should be included in the config file described in section 10.2.

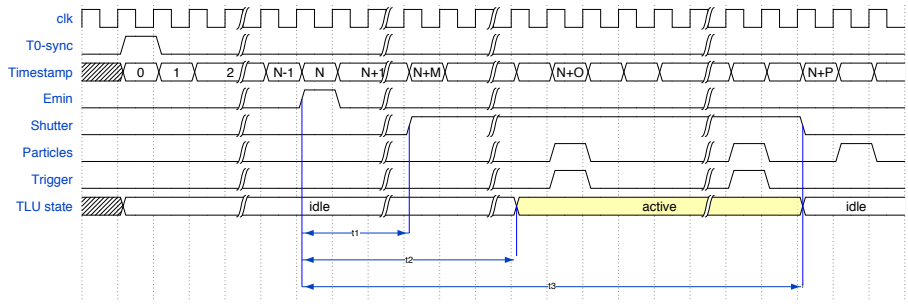


Figure 6.1: Shutter Timing: the E_{min} signal is fed to one of the trigger inputs and initiates the shutter sequence; after a programmable delay t_1 the TLU asserts the *shutter* signal. The unit will start to issue trigger signals to the DUT once a programmable time t_2 has elapsed. The window between t_1 and t_2 can be used to ensure the DUT is configured and ready to accept triggers. The unit will issue triggers until the end of the shutter window, determined by t_3.

CONFIGURATION PARAMETER	FUNCTION	NOTE	REGISTER NAME
EnableShutterMode	If 1, shutter mode is enabled. If 0, shutter mode is disabled.		ControlRW
ShutterSource	Selects which input is used to trigger shutter sequence.	Range 0:5	ShutterSelectRW
InternalShutterInterval	Internal shutter period when using internal sequence. Set to 0 to not use internal shutter generator.	32-bit vale. Units of 25 ns clock cycles.	InternalShutterPeriodRW
ShutterOnTime	Time between start of sequence and shutter asserted (t_1).	32-bit vale. Units of 25 ns clock cycles.	ShutterOnTimeRW
ShutterVetoOffTime	Time between start of sequence and veto being de-asserted (t_2).	32-bit vale. Units of 25 ns clock cycles.	ShutterVetoOffTimeRW
ShutterOffTime	Time between start of sequence and time at which shutter de-asserted and veto reasserted (t_3).	32-bit vale. Units of 25 ns clock cycles.	ShutterOffTimeRW

Table 6.1: Configuration parameters and corresponding IPBus registers controlling behaviour of shutter.

Chapter 7

Event buffer

The event buffer IPBus slave has four registers. Writing to `EventFifoCSR` will reset the First In First Out (FIFO). Reading from either of the register will put their data on the IPBus data line.
Reading from `EventFifoCSR` returns the following:

- bit 0: FIFO empty flag
- bit 1: FIFO almost empty flag
- bit 2: FIFO almost full flag
- bit 3: FIFO full flag
- bit 4: FIFO programmable full flag
- other bits: 0

The status register (SerdesRst) is as follows:

- bit 0: reset the ISERDES
- bit 1: reset the trigger counters
- bit 2: calibrate IDELAY: This seems to be disconnected at the moment.
- bit 3: fixed to 0
- bit 4, 5: status of `thresholdDeserializer(Input0)`. When the IDELAY modules (prompt, delayed) have reached the correct delay, these two bits should read 00.
- bit 6, 7: status of `thresholdDeserializer(Input1)`
- bit 8, 9: status of `thresholdDeserializer(Input2)`
- bit 10, 11: status of `thresholdDeserializer(Input3)`

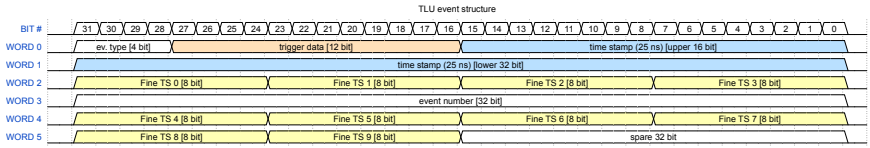


Figure 7.1: Event structure

- bit 12, 13: status of `thresholdDeserializer(Input4)`
- bit 14, 15: status of `thresholdDeserializer(Input5)`
- bit 16, 19: fixed to 0
- bit 20: `s_deserialized_threshold_data(Input0)(7)`
- bit 21: `s_deserialized_threshold_data(Input1)(7)`
- bit 22: `s_deserialized_threshold_data(Input2)(7)`
- bit 23: `s_deserialized_threshold_data(Input3)(7)`
- bit 24: `s_deserialized_threshold_data(Input4)(7)`
- bit 25: `s_deserialized_threshold_data(Input5)(7)`

9 bits are used to determine trigger edges. 8 are from the deserializers, 1 is added as the LSB and is the MSB from the previous word.

Chapter 8

Functions

The following is a list of files containing the code for the TLU:

- `./eudaq2/user/eudet/misc/aida_tlu_test.ini`:
  initialization file for the hardware. The location of the file can be passed to the EUDAQ code in the Graphic User Interface (GUI).

- `./eudaq2/user/eudet/misc/aida_tlu_test.conf`:
  configuration file. It contains all the parameters to be loaded in the TLU at the beginning of the run. If this file is not found, EUDAQ will use a list of default settings. The location of the file (and its name) can be passed to the EUDAQ code in the GUI.

- `./eudaq2/user/eudet/misc/aida_tlu_test_connection.xml`:
  define the IP address and address map of the TLU. The one listed is the default location for the file. A different location can be specified with the `ConnectionFile` option in the *conf* file for the TLU.

- `./eudaq2/user/eudet/misc/aida_tlu_test_address.xml`:
  address map for the TLU. The location of the file is specified in the `fmctlu_connection.xml` file.

- `./eudaq2/user/eudet/misc/aida_tlu_test_clock_config.txt`:
  configuration for the Si5345 clock chip. In order for the hardware to work a configuration file must be present. Those listed are the default name and location for the file; a different file can be specified with the `CLOCK_CFG_FILE` option in the *conf* file for the TLU.

- `./eudaq2/user/eudet/module/src/FMCTLU_Producer.cc`:
  eudaq producer for the TLU. Contains the methods to initialize, configure, start, stop the TLU producer.

- `./eudaq2/user/eudet/hardware/src/AidaTluController.cc`:
  Contains the definition of the hardware class for the TLU and the methods to set and read from its hardware, such as clock chip, DAC, etc. This

lever is abstract with respect to the actual hardware, so that if a future version of the board uses different components it should be possible to re-use this code.

- `./eudaq2/user/eudet/hardware/include/AidaTluController.hh`: Headers for the controller.
- `./eudaq2/user/eudet/hardware/src/AidaTluController.cxx`: Executable for the controller.
- `./eudaq2/user/eudet/hardware/src/AidaTluHardware.cc`: This is the code that deals with the actual hardware on the TLU, and contains specific instructions for the chips mounted in the current version. It contains several classes for the ADC, the clock chip, the I/O expanders etc.
- `./eudaq2/user/eudet/hardware/include/AidaTluHardware.hh`: Header for the hardware.
- `./eudaq2/user/eudet/hardware/src/AidaTluI2c.cc`: core functions used to read and write from I^2C compatible slaves.
- `./eudaq2/user/eudet/hardware/include/AidaTluI2c.hh`: Headers for the I^2C core.

8.1 Functions

enableClkLEMO Enable or disable the output clock to the differential LEMO connector.

enableHDMI Set the status of the transceivers for a specific HDMI connector. When enable= False the transceivers are disabled and the connector cannot send signals from FPGA to the outside world. When enable= True then signals from the FPGA will be sent out to the HDMI.
In the configuration file use `HDMIx_on = 0` to disable a channel and `HDMI1_on = 1` to enable it (x can be 1, 2, 3, 4).
NOTE: the other direction is always enabled, i.e. signals from the DUTs are always sent to the FPGA.
NOTE: Clock source must be defined separately using SetDutClkSrc (DUTClkSrc in python script).
NOTE: this is called `DUTOutputs` on the python scripts.

GetFW dsds

getSN dsd

I2C_enable dsd

InitializeClkChip

InitializeDAC

InitializeIOexp

InitializeI2C

PopFrontEvent

ReadRRegister

ReceiveEvents

ResetEventsBuffer

SetDutClkSrc Set the clock source for a specific HDMI connector. The source can be set to 0 (no clock), 1 (Si5345) or 2 (FPGA). In the configuration file use `HDMIx_on = N` to select the source (x can be 1, 2, 3, 4, N is the clock source).
NOTE: this is called `DUTClkSrc` on python scripts.

SetPulseStretchPk Takes a vector of six numbers, packs them (5-bits each) and sends them to the PulseStretch register.

SetThresholdValue

setTrgPattern Writes two 32-bit words to define the trigger pattern for the inputs. See section 5 for details.

SetWRegister

SetUhalLogLevel

Chapter 9

IPBus Registers

version Returns the current version of firmware used to program the TLU

DUTINTERFACES

DUTMaskW Writing to this register allows to define which DUTs are active when in AIDA mode. The lower 4 bits of the register can be used to define the status of the DUTs: 1 for active, 0 for masked. `hdmi1` is defined by bit 0, `hdmi2` is defined by bit 1, `hdmi3` is defined by bit 2, `hdmi4` is defined by bit 3.

IgnoreDUTBusyW Writing to this register allows to ignore the busy signal from a particular DUT while in AIDA mode. The lower 4 bits are used to define the status for each device. A 1 indicates that the logic should ignore busy signals from the specific DUT.

IgnoreShutterVetoW The LSB of this register can be written to define whether the DUT should ignore the shutter veto signal. Normally, when the shutter signal is asserted the DUT reports busy. If this bit is flag the DUT will ignore the shutter signal.

DUTInterfaceModeW Write register to define the mode of operation for a DUT. Two bits per device can be used to define the mode; currently only two modes are available (AIDA, EUDET) but the second but is reserved for additional modes introduced in the future.
The bit pairs are packed from the LSB starting with `hdmi1` (bits 0, 1), `hdmi2` (bits 2, 3), `hdmi3` (bits 4, 5), `hdmi4` (bits 6, 7).

- bit pair `X0`: EUDET
- bit pair `X1`: AIDA

DUTInterfaceModeModifierW Write register. This register only affects the EUDET mode of operation. For each DUT two bits can be configured although cyrrently only the lower of the pair is considere. The bit packing

Table 9.1: IPBus register

NODE	SUBNODE	ADDRESS	MASK	PERMISSION
version		0x1		r
DUTInterfaces		**0x1000**		
	DUTMaskW	0x0		w
	IgnoreDUTBusyW	0x1		w
	IgnoreShutterVetoW	0x2		w
	DUTInterfaceModeW	0x3		w
	DUTInterfaceModeModifierW	0x4		w
	DUTInterfaceModeR	0xB		r
	DUTInterfaceModeModifierR	0xC		r
	DUTMaskR	0x8		r
	IgnoreDUTBusyR	0x9		r
	IgnoreShutterVetoR	0xA		r
Shutter		**0x2000**		
	ControlRW	0x0		rw
	ShutterSelectRW	0x1		rw
	InternalShutterPeriodRW	0x2		rw
	ShutterOnTimeRW	0x3		rw
	ShutterVetoOffTimeRW	0x4		rw
	ShutterOffTimeRW	0x5		rw
	RunActiveRW	0x6		rw
i2c_master		**0x3000**		
	i2c_pre_lo	0x0	0xFF	r/w
	i2c_pre_hi	0x1	0xFF	r/w
	i2c_ctrl	0x2	0xFF	r/w
	i2c_rxtx	0x3	0xFF	r/w
	i2c_cmdstatus	0x4	0xFF	r/w
eventBuffer		**0x4000**		
	EventFifoData	0x0		r
	EventFifoFillLevel	0x1		r
	EventFifoCSR	0x2		r/w
	EventFifoFillLevelFlags	0x3		r
Event_Formatter		**0x5000**		
	Enable_Record_Data	0x0		r/w
	ResetTimestampW	0x1		w
	CurrentTimestampLR	0x2		r
	CurrentTimestampHR	0x3		r
triggerInputs		**0x6000**		
	SerdesRstW	0x0		w
	InvertEdgeW	0x1		w
	SerdesRstR	0x8		r
	ThrCount0R	0x9		r
	ThrCount1R	0xA		r
	ThrCount2R	0xB		r
	ThrCount3R	0xC		r
	ThrCount4R	0xD		r
	ThrCount5R	0xE		r
triggerLogic		**0x7000**		
	PostVetoTriggersR	0x10		r
	PreVetoTriggersR	0x11		r
	InternalTriggerIntervalW	0x02		w
	InternalTriggerIntervalR	0x12		r
	TriggerVetoW	0x04		w
	TriggerVetoR	0x14		r
	ExternalTriggerVetoR	0x15		r
	PulseStretchW	0x06		w
	PulseStretchR	0x16		r
	PulseDelayW	0x07		w
	PulseDelayR	0x17		r
	TriggerHoldOffW	0x08		w
	TriggerHoldOffR	0x18		r
	AuxTriggerCountR	0x19		r
	TriggerPattern_lowW	0x0A		w
	TriggerPattern_lowR	0x1A		r
	TriggerPattern_highW	0x0B		w
	TriggerPattern_highR	0x1B		r
logic_clocks		**0x8000**		
	LogicClocksCSR	0x0		r/w
	LogicRst	0x1		w

is done in a manner similar to the DUTInterfaceMode. Set bit high to allow asynchronous veto using DUT_CLK when in EUDET mode.

DUTInterfaceModeR Read the content of the DUTInterfaceMode register.

DUTInterfaceModeModifierR Read status of the DUTInterfaceMode register.

DUTMaskR Read the status of the DUTMask register.

IgnoreDUTBusyR Read the status of the IgnoreDUTBusy register.

IgnoreShutterVetoR Read the status of the IgnoreShutterVeto word (only the last bit is meanigful).

SHUTTER These registers control the signal that the DUTs receive on the cont line. A shutter on/off (active/inactive) signal can either be produced from an internal timer or triggered from one of the trigger inputs (N.B. Any trigger input used to control the shutter will still be connected to the trigger logic. Set the trigger mask accordingly)

ControlRW The LSB of this register controls if shutter pulses are active. 1 = active.

ControlRW Bit-0 controls if shutter pulses are active. 1 = active

ShutterSelectRW Selects which input is used to trigger shutter

InternalShutterPeriodRW Internal trig generator period (units = number of strobe pulses)

ShutterOnTimeRW Time between input trigger being received and shutter asserted(T1) (units = number of strobe pulses)

ShutterVetoOffTimeRW time between input trigger and veto being de-asserted(T2) (units = number of strobe pulses)

ShutterOffTimeRW time between input trigger and time at which shutter de-asserted and veto reasserted(T3) (units = number of strobe pulses)

RunActiveRW Writing '1' to Bit-0 of this register raises the internal run_active signal and and causes sync line to pulse for one clock cycle (i.e. issues a start of run T0 signal.

I2C_MASTER This section includes registers used to talk to the I^2C bus.

i2c_pre_lo Lower part of the clock pre-scaler value. The pre-scaler is used to reduce the clock frequency of the bus and make it compatible with the I^2C slaves on the board.

i2c_pre_hi Higher part of the clock pre-scaler value.

i2c_ctrl

i2c_rxtx

i2c_cmdstatus

EVENTBUFFER

EventFifoData Returns the content of the FIFO. In the current firmware implementation the memory can hold 8192 words (32-bit).

EventFifoFillLevel Read register. Returns the number of words written in the FIFO. The lowest 14-bits are the actual data.

EventFifoCSR Read or write register. When read it returns the status of the FIFO. Five flags are returned:

- bit 0: empty. Asserted when the FIFO is empty.
- bit 1: almost empty. Asserted when one word remains in the FIFO.
- bit 2: almost full. Asserted when the FIFO can only accept one more word before becoming full.
- bit 3: full. In the current firmware the FIFO can hold 8192 words before filling up.
- bit 4: programmable full. This signal is asserted when the number of words in the FIFO is greater than or equal to the assert threshold (8181). It is de-asserted when the number of words in the FIFO is less than the negate threshold (8180).

When any value is written to this register the FIFO is reset.

EventFifoFillLevelFlags Does not do anything? REMOVE CHECK

EVENT_FORMATTER

Enable_Record_Data Read and write register. When written, CHECK When read returns the content of the enable record word.

ResetTimestampW Write register. Writing any value to this register will cause the firmware to produce a retest timestamp signal (high for one clock cycle of clk_4x_logic). At the moment it does not seems to be connected to anything. CHECK

CurrentTimestampLR CHECK

CurrentTimestampHR CHECK

TRIGGERINPUTS

SerdesRstW Write register for the SerDes control.

- bit 0: set this bit to reset the ISERDES
- bit 1: set this bit to reset the input trigger counters
- bit 2: `s_calibrate_delay`

InvertEdgeW Bottom 6 bits control what counts as leading edge of pulse. Set bit to 0 to trigger on low voltage to high voltage (e.g. TTL pulses). Set bit to 1 to trigger on high voltage to low voltage (e.g. NIM pulses, PMT pulses)

SerdesRstR Read register for the SerDes control.

ThrCount0R Read register. Returns the number of pulses above threshold for the trigger input.

ThrCount1R Read register. Returns the number of pulses above threshold for the trigger input.

ThrCount2R Read register. Returns the number of pulses above threshold for the trigger input.

ThrCount3R Read register. Returns the number of pulses above threshold for the trigger input.

ThrCount4R Read register. Returns the number of pulses above threshold for the trigger input.

ThrCount5R Read register. Returns the number of pulses above threshold for the trigger input.

TRIGGERLOGIC

PostVetoTriggersR Read register. Returns the number of triggers recorded in the TLU after the veto is applied. These are the triggers actually sent to the DUTs.

PreVetoTriggersR Read register. Returns the number of triggers recorded in the TLU before the veto is applied. This is used for debugging purposes.

InternalTriggerIntervalW Write the number of clock cycles to be used as period for the internal trigger generator. If this number is smaller than 5 then the triggers are disabled. Otherwise the period is number -2.

InternalTriggerIntervalR Read the value written in InternalTriggerIntervalW.

TriggerVetoW Write register. The value written to the LSB of this register is used to generate a veto signal. This can be used to put switch the TLU status: if the bit is asserted the logic will not send new triggers to the DUTs. If the bit is reset the board will process new triggers.

TriggerVetoR Read the content of the TriggerVeto register.

ExternalTriggerVetoR Read register. Bit 0 of this register reports the `veto` status (1 for veto active, 0 for no veto). The veto is active if the TLU buffer is full or if one of the DUTs is sending a veto signal.

PulseStretchW Write the stretch word for the trigger pulses. The original trigger pulses collected at a trigger input can be stretched by N cycles of the 4x clock (160 MHz, 6.25 ns). N is a number between 0 and 31. The stretched pulse is always at least as long as the original input.
The stretch values can be written in the `conf` file using the parameters `inX_STR` (X= [0 ... 5]).
The six words for the inputs are packed in a single 32-bit word written to this register according to the format shown in table 9.2.

PulseStretchR Returns the content of the PulseStretch word.

PulseDelayW Write the delay word for the trigger pulses. The original pulse is delayed by N clycles of the 4x clock (160 MHz, 6.25 ns). N is a number between 0 and 31. The six words for the inputs are packed in a single 32-bit word written to this register according to the format shown in table 9.2.
The delay values can be written in the `conf` file using the parameters `inX_DEL` (X= [0 ... 5]).

PulseDelayR Returns the content of the PulseDelay word.

TriggerHoldOffW Does not do anything? CHECK

TriggerHoldOffR Read the previous register... CHECK

AuxTriggerCountR Auxiliary trigger counter. Used for debug.

TriggerPattern_lowW Write register for the lower 32-bits of the trigger pattern. This pattern is used to select the combinations of trigger signals that produce a valid trigger in the TLU. See section 5.1 for details.

TriggerPattern_lowR Read register for the lower 32-bits of the trigger pattern. This pattern is used to select the combinations of trigger signals that produce a valid trigger in the TLU. See section 5.1 for details.

TriggerPattern_highW Write register for the higher 32-bits of the trigger pattern. This pattern is used to select the combinations of trigger signals that produce a valid trigger in the TLU. See section 5.1 for details.

TriggerPattern_highR Read register for the higher 32-bits of the trigger pattern. This pattern is used to select the combinations of trigger signals that produce a valid trigger in the TLU. See section 5.1 for details.

LOGIC_CLOCKS

LogicClocksCSR This is a read/write register. The write function is now obsolete and should be removed. Reading from this register returns the status of the PLL lock: bit 0 is the locked value of the pll (1= locked).

LogicRst Writing a 1 in the LSB of this register will reset the PLL and the clocks used by the TLU firmware. It needs to be checked for bugs.

Table 9.2: Packing scheme for values in registers used to define the pulse stretch and delay.

Register value																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	Input 5					Input 4					Input 3					Input 2					Input 1					Input 0				
x	x	b4	b3	b2	b1	b0	b4	b3	b2	b1	b0	b4	b3	b2	b1	b0	b4	b3	b2	b1	b0	b4	b3	b2	b1	b0	b4	b3	b2	b1	b0

Chapter 10

EUDAQ Parameters

List of parameters that are parsed by the EUDAQ run control GUI to configure the TLU.
The parameters must be included in the INI or CONF file passed to the main window (see fig.10.1).
Not all parameters are needed; if one of the parameters is not present in the files, the code will generally assume a default value, indicated in brackets in the following document `[type, default]`.

Case sensitiveness

All parameters names are case sensitive!
Please ensure to use the correct capitalization.
A misspelled parameter will be ignored and its default value will be used instead. EUDAQ does not provide any warning or feedback about this, so extra care should be used to avoid unexpected results.

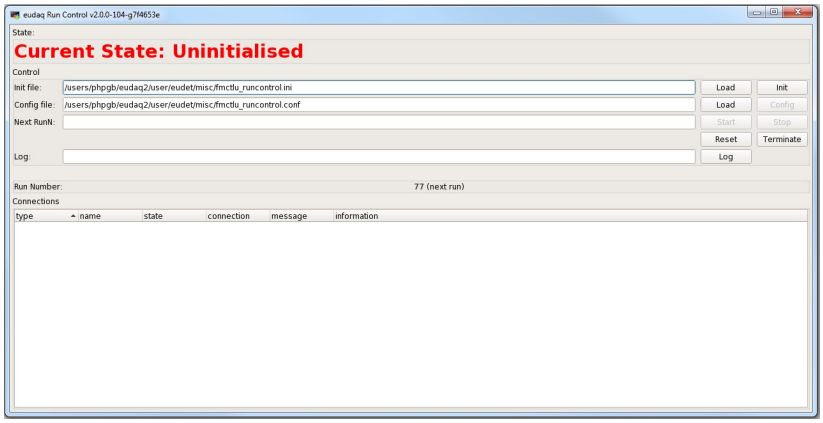


Figure 10.1: Main user iterface of the EUDAQ framework.

10.1 INI file

initid `[string, "0"]` Does not serve any purpose in the code but can be useful to identify configuration settings used in a specific run. As an example, the user can write a mnemonic such as 'Testbeam_April' or '2017_10_init' to help identifying a specific configuration. EUDAQ will store this information in the run data.

ConnectionFile `[string, "file://./FMCTLU_connections.xml"]` Name of the xml file used to store the information required to communicate with the hardware, such as its IP address and the location of the address map. The default location indicates a file that must be located in the `bin` folder.

skipini `[int, 0]` When this flas is set, the producer will skip the whole initialization phase for the TLU. This can be useful to avoid disturbing any other piece of hardware connected to the unit, as it avoid re-initializing the DACs, HDMI connectors, clock chip, etc.

DeviceName `[string, "fmctlu.udp"]` The name of the type of hardware to be contacted by the IPBus.

TLUmod `[string, "1e"]` Version of the TLU hardware. Reserved for future use.

nDUTs `[positive int, 4]` Number of DUT in the current TLU. This is for future upgrades and should not require editing by the user.

nTrgIn `[positive int, 6]` Number of trigger inputs in the current TLU. This is for future upgrades and should not require editing by the user.

I2C_COREEXP_Addr `[positive int, 0x21]` I^2C address of the core expander mounted on the Enclustra board. This is not required if a different FPGA is used. See section 2.4 for further details.

I2C_CLK_Addr `[positive int, 0x68]` I^2C address of Si5345 clock generator installed on the TLU.

I2C_DAC1_Addr `[positive int, 0x13]` I^2C address of DAC installed on the TLU. The DAC is used to configure the threshold of the trigger inputs.

I2C_DAC2_Addr `[positive int, 0x1F]` I^2C address of DAC installed on the TLU. The DAC is used to configure the threshold of the trigger inputs.

I2C_ID_Addr `[positive int, 0x50]` I^2C address of the unique ID EEPROM installed on the TLU. The chip is used to provide a unique identifier to each kit.

I2C_EXP1_Addr `[positive int, 0x74]` I^2C address of the bus expander used to select the direction of the HDMI pins on the board.

I2C_EXP2_Addr `[positive int, 0x75]` I^{2}C address of the bus expander used to select the direction of the HDMI pins on the board.

I2C_DACModule_Addr `[positive int, 0x1C]` I^{2}C address of the DAC installed on the power module and used to control the PMT outputs.

PMT_vCtrlMax `[float, 1]` value, in volts, of the maximum control voltage for the PMTs. For EUDET telescopes this should normally be left to 1 V. If the TLU is going to be used with different PMTs, then a new value can be used but the hardware must be tweaked accordingly by changing the voltagi divider on the power module.

I2C_EXP1Module_Addr `[positive int, 0x76]` I^{2}C address of the first expander used to control the indicators on the power module.

I2C_EXP2Module_Addr `[positive int, 0x77]` I^{2}C address of the second expander used to control the indicators on the power module.

intRefOn `[boolean, false]` If true, the DACs installed on the TLU will use their internal voltage reference rather than the one provide externally.

VRefInt `[float, 2.5]` Value in volts for the internal reference voltage of the DACs. The voltage is chosen by the chip manufacturer. This is only used if `intRefOn= true`.

VRefExt `[float, 1.3]` Value in volts for the external reference voltage of the DACs. The voltage is determined by a circuit on the TLU and the value of this parameter must reflect such voltage. This is only used if `intRefOn= false`.

CONFCLOCK `[boolean, true]` If true, the clock chip Si5345 will be reconfigured when the INIT button is pressed (see figure fig.10.1). The chip is configured via I^{2}C interface using a specific text file (see next parameter). After a power cycle, the chip is its default state and must be reconfigured to operate the TLU correctly[1].

CLOCK_CFG_FILE `[string, "./../user/eudet/misc/fmctlu_clock_config.txt"]` Name of the text file used to store the configuration values of the Si5345. The file can be generate using the Clockbuilder Pro software provided by SiLabs.

10.2 CONF file

confid `[string, "0"]` Does not serve any purpose in the code but can be useful to identify configuration settings used in a specific run. EUDAQ will store this information in the run data.

[1] As long as the unit is powered, the clock chip will maintain its setup, so the user can set this flag to 0 after the first initialization, in order to save time.

verbose `[int, 0]` Defines the level of output messages from the TLU. 0= only errors (minimum), 1= warning (default), 2= info, 3= all.

skipconf `[int, 0]` When this flag is set, EUDAQ will skip the whole configuration phase for the TLU. When the user configures the hardware in EUDAQ, the board will remain in its current state and no configuration parameter will be written. This can be useful to avoid disturbing other pieces of electronics.

HDMI1_set `[unsigned int, 0b0001]` Defines the source of the signal on the pins for the `HDMI1` connector. A 1 indicates that each pin pair is an driven by the TLU, a 0 that they are left floating (with respect to the TLU). This can be used to define the signal direction on each pin pair. The order of the pairs is as follow:
bit 0= CONT, bit 1= SPARE, bit 2= TRIG, bit 3= BUSY.
Note that the direction of the DUTClk pair is defined in a separate parameter (see HDMI_clk).
Example to configure the connector to work with an EUDET device:
- in this configuration the BUSY line is driven by the device under test, so it is an input for the TLU and should not be driven by it (bit 3= 0)
- TRIGGER line is an output for the TLU so is driven by it (bit 2= 1)
- SPARE line is used to provide control signals, such as the reset signal to initialize the devices at the start of a run (T_0). It should be configured as driven by the TLU (bit 1= 1)
- CONT is used by the TLU to issue control commands and should be configured as a signal driven by the TLU (bit 0= 1).
Therefore the value of this parameter would be 0x7 (b0111).

HDMI2_set `[unsigned int, 0b0001]` Defines the direction of the pins for the `HDMI2` connector.

HDMI3_set `[unsigned int, 0b0001]` Defines the direction of the pins for the `HDMI3` connector.

HDMI4_set `[unsigned int, 0b0001]` Defines the direction of the pins for the `HDMI4` connector.

HDMI1_clk `[unsigned int, 1]` Defines if the DUTClk pair on the HDMI connector must be driven by the TLU and, if so, what clock source to use. A 0 indicates that the pins are not driven by the TLU. 1 indicates that pins will by driven with the clock produced from the on-board clock chip Si5345. 2 indicates that the driving clock is obtained from the FPGA. Example to configure the connector to work with an EUDET device: in this scenario the clock is driven by the DUT so the parameter should be set to 0. Example to configure the connector to work with an AIDA device: in this scenario the clock is driven by the TLU so the parameter should be set to either 1 or 2 (by default 1).

HDMI2_clk `[unsigned int, 1]` Defines the driving signal on the corresponding HDMI connector.

HDMI3_clk `[unsigned int, 1]` Defines the driving signal on the corresponding HDMI connector.

HDMI4_clk `[unsigned int, 1]` Defines the driving signal on the corresponding HDMI connector.

LEMOclk `[boolean, true]` Defines whether a driving clock is to be provided on the differential LEMO connector of the TLU. By default (value= 1), the clock is driven from the clock chip. If the value is set to 0 no clock will be driven.

PMT1_V `[float, 0.0]` Defines the control voltage for PMT 1, in volts. The value can range from 0 to 1 V.

PMT2_V `[float, 0.0]` Defines the control voltage for PMT 2, in volts. The value can range from 0 to 1 V.

PMT3_V `[float, 0.0]` Defines the control voltage for PMT 3, in volts. The value can range from 0 to 1 V.

PMT4_V `[float, 0.0]` Defines the control voltage for PMT 4, in volts. The value can range from 0 to 1 V.

in0_STR `[unsigned int, 0]` Defines the number of clock cycles used to stretch a pulse once a trigger is detected by the discriminator on input 0. This feature allows the user to modify the pulses that are then fed into the trigger logic within the TLU. A minimum lenght of 6.25 ns is provided if the value is 0. Any extra clock cycle extend the pulse by 6.25 ns (160 MHz clock). An example of the effect on the stretch setting is shown in figure 5.2.

in0_DEL `[unsigned int, 0]` Defines the delay, in 160 MHz clock cycles, to be assigned to the discriminated pulse from input 0, in order to process the logic for the trigger. This can be used to compensate for differences in cable lengths for the signals used to create a trigger.

in1_STR `[unsigned int, 0]` Same as `in1_STR` but for input 1.

in1_DEL `[unsigned int, 0]` Same as `in1_DEL` but for input 1.

in2_STR `[unsigned int, 0]` Same as `in1_STR` but for input 2.

in2_DEL `[unsigned int, 0]` Same as `in1_DEL` but for input 2.

in3_STR `[unsigned int, 0]` Same as `in1_STR` but for input 3.

in3_DEL `[unsigned int, 0]` Same as `in1_DEL` but for input 3.

in4_STR `[unsigned int, 0]` Same as `in1_STR` but for input 4.

in4_DEL `[unsigned int, 0]` Same as `in1_DEL` but for input 4.

in5_STR `[unsigned int, 0]` Same as `in1_STR` but for input 5.

in5_DEL `[unsigned int, 0]` Same as `in1_DEL` but for input 5.

trigMaskHi `[unsigned int32, 0]` This word represents the most significative bits of the 64-bits used to determine the trigger mask.
A detailed explanation of how to determine the correct word is provided in section 5.1.

trigMaskLo `[unsigned int32, 0]` This word represents the least significative bits of the 64-bits used to determine the trigger mask.
A detailed explanation of how to determine the correct word is provided in section 5.1.

DUTMask `[unsigned int, 0x1]` This mask indicates which HDMI inputs have an AIDA device connected. Each of the lowest four bits correspond to a connector (bit 0= DUT1, bit 1= DUT2, bit 2= DUT3, bit 3= DUT4). If the bit is set to 1 the TLU expects a device connected and exchanging signals according to the mode selected (see DUTMaskMode).

DUTMaskMode `[unsigned int, 0xFF]` Defines the mode of operation of the device connected to a specific HDMI port.
Two bits are needed for each device, so bits 0,1 refer to HDMI1, bits 2, 3 refer to HDMI2, etc. The bits define whether the device is in AIDA or EUDET mode and if the trigger output is required, as described in section 4.1. The available options are:

0x00 EUDET mode.

0x01 AIDA mode with trigger output.

0x11 AIDA mode.

0x10 reserved for future mode. Do not use.

Example: to configure device 0 and 1 as EUDET, 2 as AIDA and 3 as AIDA with trigger the parameters should be set to 01-11-00-00, i.e. 0x70. See also section 9.

DUTMaskModeModifier `[unsigned int, 0xF]` This mask only affects EUDET mode. Each of the lower 4 bits correspond to a device. If the device is in EUDET mode, it can assert DUTClk to produce a global veto in the triggers. This behaviour occurs if the corresponding bit is set to 1. If the bit is set to 0, asserting the DUTClk from the device will not produce a global veto.

DUTIgnoreBusy `[unsigned int, 0xF]` This mask tells the TLU to ignore the BUSY signal from a specific device, either in AIDA or EUDET mode. If the device is in AIDA mode, this means that further triggers will be issued while the device is busy. If the device is in EUDET mode, this means that the TLU will not pause while they are in the handshake phase. In turn, this means that the device will likely receive events where the trigger number does not increase sequentially by one.

DUTIgnoreShutterVeto `[unsigned int, 0x1]` Set bit to 1 to tell the DUT to ignore the shutter signal.

EnableRecordData `[boolean, true]` if set to 1, enable the data recording in the TLU.

InternalTriggerFreq `[unsigned int, 0]` Defines the rate of the trigger generated internally by the TLU, in Hz: if 0, the internal triggers are disabled. Any other value activates the internal trigger generator with frequency equal to the parameter. Values above 160 MHz are coerced to 160 MHz.

EnableShutterMode `[unsigned int, 0]` If set to 1, enables the use of the shutter mode described in section 6. Set to 0 to disable the shutter mode.

ShutterSource `[unsigned int, 0]` Defines which of the six LEMO inputs is to be used to trigger the shutter sequence. The input should not be also used as part of the trigger validation.

InternalShutterInterval `[unsigned int, 0]` Determines the period, in 25 ns clock cycles, of the internal shutter trigger. This can be used for debugging purposes. Set to 0 to disable this feature.

ShutterOnTime `[unsigned int, 0]` Time between start of sequence and shutter asserted (t_1 in figure 6.1). The value is defined in 25 ns clock units, i.e. a value of 3 corresponds to 75 ns.

ShutterVetoOffTime `[unsigned int, 0]` Time between start of sequence and veto being de-asserted (t_2 in figure 6.1). The value is defined in 25 ns clock units.

ShutterOffTime `[unsigned int, 0]` Time between start of sequence and time at which shutter de-asserted and veto reasserted (t_3 in figure 6.1). The value is defined in 25 ns clock units.

Chapter 11

Control software

The preferred method to run the TLU is by using the EUDAQ[1] data acquisition framework.
A TLU producer, based on C++, has been written to integrate the hardware in EUDAQ and is regularly pushed to the master repository. Checking out the latest EUDAQ software ensures to also have a stable version of the producer.
In addition to the EUDAQ producer, a set of Python scripts has been developed to enable users to configure and run the TLU using a minimal environment without having to setup the whole data acquisition framework. The scripts are meant to reflect all the functionalities in the EUDAQ producers, i.e. using the scripts it should be possible to perform any operation available on the EUDAQ producer. However, they should only be used for local debugging and testing.

Warning

When fixing bus or developing new software for the TLU, priority will be given to ensure that the EUDAQ producer is patched first. As a consequence, there is a higher chance to find bugs in the Python scripts.

11.1 EUDAQ Producer

Current structure of a fmctlu producer event:

```
<Event>
  <Type>2149999981</Type>
  <Extendword>171577627</Extendword>
  <Description>Ex0Tg</Description>
  <Flag>0x00000018</Flag>
  <RunN>0</RunN>
  <StreamN>0</StreamN>
  <EventN>0</EventN>
  <TriggerN>88</TriggerN>
  <Timestamp>0x0000000000000000  ->  0x0000000000000000</Timestamp>
```

[1] https://github.com/eudaq/eudaq

```
  <Timestamp>0   ->   0</Timestamp>
  <Block_Size>0</Block_Size>
  <SubEvents>
    <Size>1</Size>
    <Event>
      <Type>2149999981</Type>
      <Extendword>3634980144</Extendword>
      <Description>TluRawDataEvent</Description>
      <Flag>0x00000010</Flag>
      <RunN>96</RunN>
      <StreamN>4008428646</StreamN>
      <EventN>88</EventN>
      <TriggerN>88</TriggerN>
      <Timestamp>0x0000000105b44f91   ->   0x0000000105b44faa</Timestamp>
      <Timestamp>4390670225   ->   4390670250</Timestamp>
      <Tags>
        <Tag>PARTICLES=89</Tag>
        <Tag>SCALER0=93</Tag>
        <Tag>SCALER1=93</Tag>
        <Tag>SCALER2=0</Tag>
        <Tag>SCALER3=0</Tag>
        <Tag>SCALER4=0</Tag>
        <Tag>SCALER5=0</Tag>
        <Tag>TEST=110011</Tag>
        <Tag>trigger=</Tag>
      </Tags>
      <Block_Size>0</Block_Size>
    </Event>
  </SubEvents>
</Event>
```

Type ??

ExtendWord ??

Description

Flag Independent from producer. See the EUDAQ documentation for details.

RunN

StreamN

EventN

TriggerN Both in the event and subevent this is written byt the producer with `ev->SetTriggerN(trigger_n);`

Timestamp The event timestamp is currently always 0. The subevent timestamps is written by the producer `ev->SetTimestamp(ts_ns, ts_ns+25, false);`. The top line (0x0000000105b44f91, in the example) is coarse time stamp multiplied by 25, so it represents the time in nanoseconds. The bottom one (4390670225) is the same number but written in decimal format instead of hexadecimal.

PARTICLES Number of pre-veto triggers recorded by the TLU: the trigger logic can detect a valid trigger condition even when the unit

is vetoed. In this case no trigger is issued to the DUTs but the number of such triggers is stored as number of particles. `ev->SetTag("PARTICLES", std::to_string(pt));`

SCALER# Number of triggers edges seen by the specific discriminator. `ev->SetTag("SCALER", std::to_string(sl));`

??? Event type from TLU is missing?

??? Input trig, i.e. the actual firing inputs should be in TRIGGER but there seems to be nothing there

11.2 Python scripts

The scripts used to debug work locally with the TLU are located in the OHWR fmc-mtlu-sw firmware repository[2]. It is also necessary to have a local installation of IPBUS and uHAL[3].Set the PYTHONPATH environment variable to include the packages sub-directory and the UHAL package.
Once all the necessary packages have been installed and the environment is set to point to the right folders, it is possible to run the `startTLU_v1e.py` script to start an interface that allows to operate the TLU.

[2]https://ohwr.org/project/fmc-mtlu-sw.git
[3]https://ipbus.web.cern.ch/ipbus/doc/user/html/index.html

Chapter 12

Appendix

12.1 Layout of Enclustra FPGA.

2.4 Top view

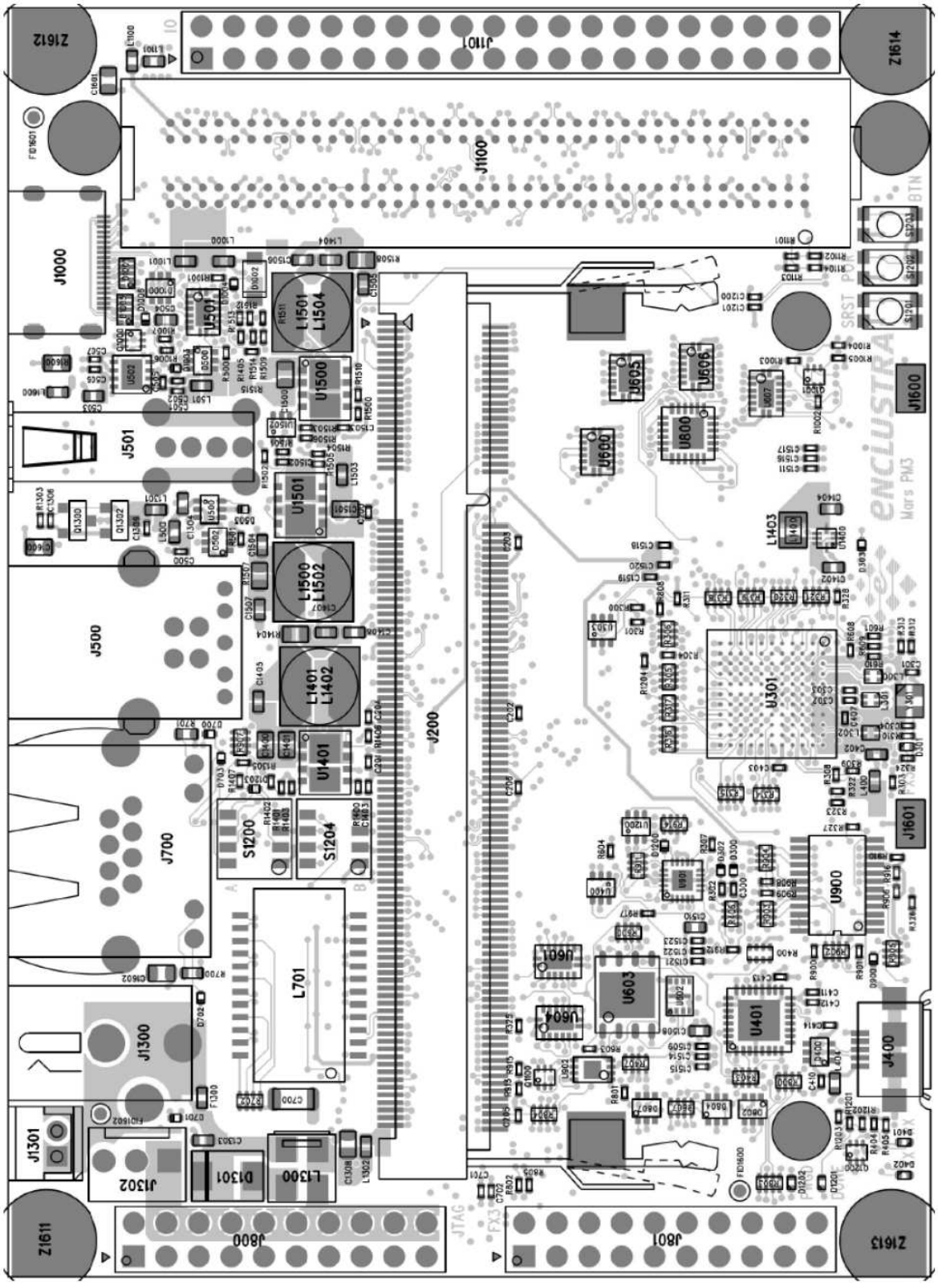


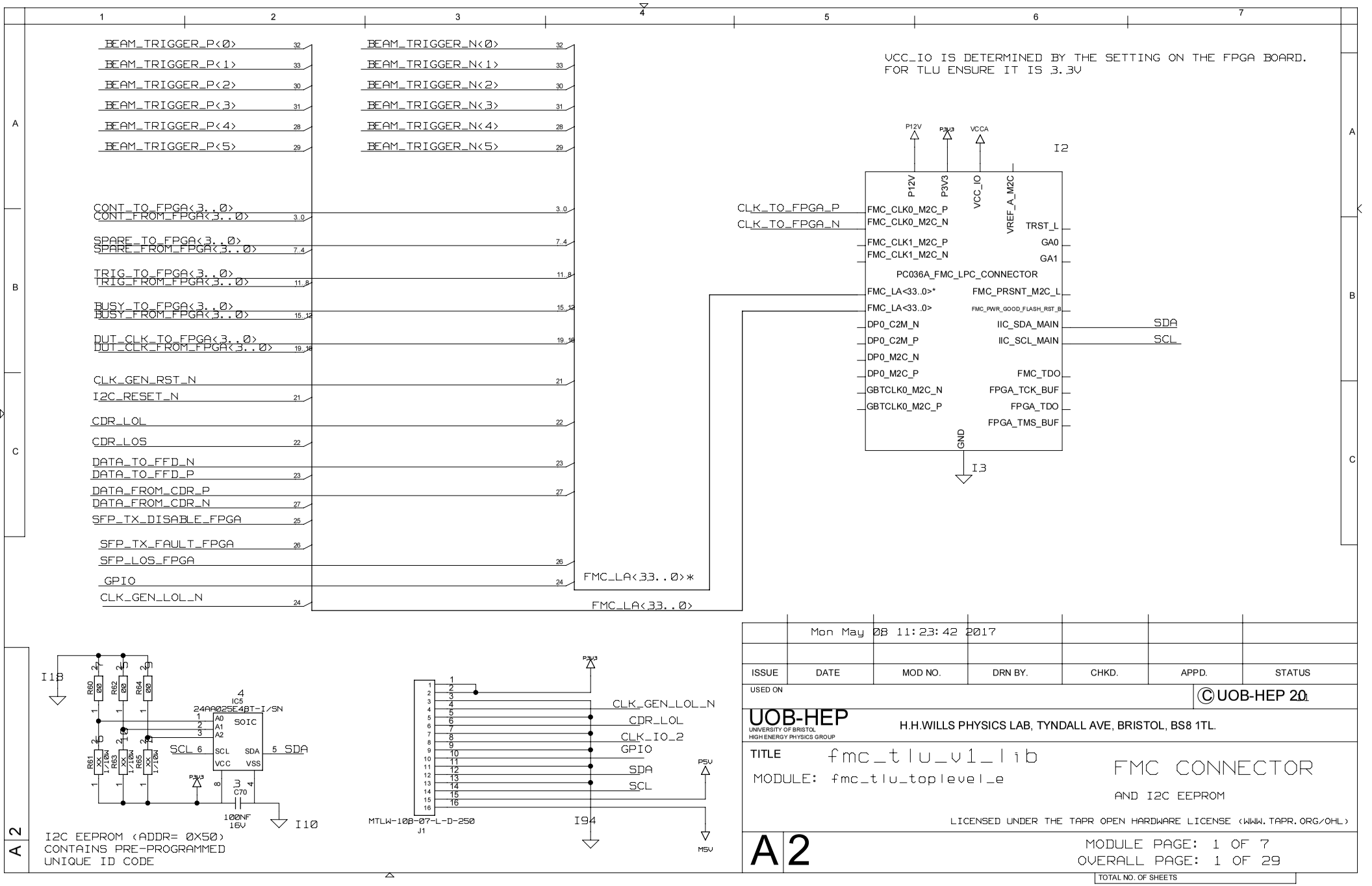
Figure 3: Top view

12.2 Connections between TLU and FPGA package.

Schematic side			FPGA Side				
NET NAME	**FMC_LA**	**J4**	**FMC NAME**	**PACKAGE_PIN**	**VDHL NAME**	**FPGA IN/OUT**	**CONSTRAINT INSTRUCTION**
BEAM_TRIGGER_P<0>	FMC_LA<32>	H37	LA32_P	B1	threshold_discr_p_i[0]	In	set_property PACKAGE_PIN B1 [get_ports {threshold_discr_p_i[0]}]
BEAM_TRIGGER_P<1>	FMC_LA<33>	G36	LA33_P	C4	threshold_discr_p_i[1]	In	set_property PACKAGE_PIN C4 [get_ports {threshold_discr_p_i[1]}]
BEAM_TRIGGER_P<2>	FMC_LA<30>	H34	LA30_P	K2	threshold_discr_p_i[2]	In	set_property PACKAGE_PIN K2 [get_ports {threshold_discr_p_i[2]}]
BEAM_TRIGGER_P<3>	FMC_LA<31>	G33	LA31_P	C6	threshold_discr_p_i[3]	In	set_property PACKAGE_PIN C6 [get_ports {threshold_discr_p_i[3]}]
BEAM_TRIGGER_P<4>	FMC_LA<28>	H31	LA28_P	J4	threshold_discr_p_i[4]	In	set_property PACKAGE_PIN J4 [get_ports {threshold_discr_p_i[4]}]
BEAM_TRIGGER_P<5>	FMC_LA<29>	G30	LA29_P	H1	threshold_discr_p_i[5]	In	set_property PACKAGE_PIN H1 [get_ports {threshold_discr_p_i[5]}]
BEAM_TRIGGER_N<0>	FMC_LA*<32>	H38	LA32_N	A1	threshold_discr_n_i[0]	In	set_property PACKAGE_PIN A1 [get_ports {threshold_discr_n_i[0]}]
BEAM_TRIGGER_N<1>	FMC_LA*<33>	G37	LA33_N	B4	threshold_discr_n_i[1]	In	set_property PACKAGE_PIN B4 [get_ports {threshold_discr_n_i[1]}]
BEAM_TRIGGER_N<2>	FMC_LA*<30>	H35	LA30_N	K1	threshold_discr_n_i[2]	In	set_property PACKAGE_PIN K1 [get_ports {threshold_discr_n_i[2]}]
BEAM_TRIGGER_N<3>	FMC_LA*<31>	G34	LA31_N	C5	threshold_discr_n_i[3]	In	set_property PACKAGE_PIN C5 [get_ports {threshold_discr_n_i[3]}]
BEAM_TRIGGER_N<4>	FMC_LA*<28>	H32	LA28_N	H4	threshold_discr_n_i[4]	In	set_property PACKAGE_PIN H4 [get_ports {threshold_discr_n_i[4]}]
BEAM_TRIGGER_N<5>	FMC_LA*<29>	G31	LA29_N	G1	threshold_discr_n_i[5]	In	set_property PACKAGE_PIN G1 [get_ports {threshold_discr_n_i[5]}]
				P17	enclustra_clk	In	
CLK_TO_FPGA_P	FMC_CLK0_M2C_P	H4	CLK0_M2C_P	T5	sysclk_40_i_p	In	set_property PACKAGE_PIN T5 [get_ports {sysclk_40_i_p}]
CLK_TO_FPGA_N	FMC_CLK0_M2C_N	H5	CLK0_M2C_N	T4	sysclk_40_i_n	In	set_property PACKAGE_PIN T4 [get_ports {sysclk_40_i_n}]
CLK_FROM_FPGA_P	FMC_CLK1_M2C_P	G2	CLK1_M2C_P	E3	sysclk_50_o_p	Out	set_property PACKAGE_PIN E3 [get_ports {sysclk_50_o_p}]
CLK_FROM_FPGA_N	FMC_CLK1_M2C_N	G3	CLK1_M2C_N	D3	sysclk_50_o_n	Out	set_property PACKAGE_PIN D3 [get_ports {sysclk_50_o_n}]
SDA				P18			
SCL				N17			
I2C_RESET_N	FMC_LA<21>	H25	LA21_P	C2	i2c_reset	Out	set_property PACKAGE_PIN C2 [get_ports {i2c_reset}]
GPIO	FMC_LA*<24>	H29	LA24_N	F6	gpio	In/Out	set_property PACKAGE_PIN F6 [get_ports {gpio}]
CLK_GEN_RST_N	FMC_LA*<21>	H26	LA21_N	C1	clk_gen_rst	Out	set_property PACKAGE_PIN C1 [get_ports {clk_gen_rst}]
CLK_GEN_LOL_N	FMC_LA<24>	H28		G6		In	
SFP_LOS_FPGA	FMC_LA*<26>	D27		G2		In	
SFP_TX_FAULT_FPGA	FMC_LA<26>	D26		H2		In	
SFP_TX_DISABLE_FPGA	FMC_LA<25>	G27		H6		Out	
CDR_LOL	FMC_LA*<22>	G25		D7		In	
CDR_LOS	FMC_LA<22>	G24		E7		In	
DATA_FROM_CDR_P	FMC_LA<27>	C26		J3		In	
DATA_FROM_CDR_N	FMC_LA*<27>	C27		J2		In	
DATA_TO_FFD_P	FMC_LA<23>	D23		F1			
DATA_TO_FFD_N	FMC_LA*<23>	D24		E1		Out	
CONT_TO_FPGA<0>	FMC_LA*<0>	G7	LA00_N_CC	P5	cont_i[0]	In	set_property PACKAGE_PIN P5 [get_ports {cont_i[0]}]
CONT_TO_FPGA<1>	FMC_LA*<1>	D9	LA01_N_CC	P3	cont_i[1]	In	set_property PACKAGE_PIN P3 [get_ports {cont_i[1]}]
CONT_TO_FPGA<2>	FMC_LA*<2>	H8	LA02_N	N6	cont_i[2]	In	set_property PACKAGE_PIN N6 [get_ports {cont_i[2]}]
CONT_TO_FPGA<3>	FMC_LA*<3>	G10	LA03_N	L5	cont_i[3]	In	set_property PACKAGE_PIN L5 [get_ports {cont_i[3]}]
SPARE_TO_FPGA<0>	FMC_LA*<4>	H11	LA04_N	M1	spare_i[0]	In	set_property PACKAGE_PIN M1 [get_ports {spare_i[0]}]

SPARE_TO_FPGA<1>	FMC_LA*<5>	D12	LA05_N	N4	spare_i[1]	In	set_property PACKAGE_PIN N4 [get_ports {spare_i[1]}]
SPARE_TO_FPGA<2>	FMC_LA*<6>	C11	LA06_N	N1	spare_i[2]	In	set_property PACKAGE_PIN N1 [get_ports {spare_i[2]}]
SPARE_TO_FPGA<3>	FMC_LA*<7>	H14	LA07_N	M2	spare_i[3]	In	set_property PACKAGE_PIN M2 [get_ports {spare_i[3]}]
TRIG_TO_FPGA<0>	FMC_LA*<8>	G13	LA08_N	R5	triggers_i[0]	In	set_property PACKAGE_PIN R5 [get_ports {triggers_i[0]}]
TRIG_TO_FPGA<1>	FMC_LA*<9>	D15	LA09_N	R2	triggers_i[1]	In	set_property PACKAGE_PIN R2 [get_ports {triggers_i[1]}]
TRIG_TO_FPGA<2>	FMC_LA*<10>	C15	LA10_N	T1	triggers_i[2]	In	set_property PACKAGE_PIN T1 [get_ports {triggers_i[2]}]
TRIG_TO_FPGA<3>	FMC_LA*<11>	H17	LA11_N	V1	triggers_i[3]	In	set_property PACKAGE_PIN V1 [get_ports {triggers_i[3]}]
BUSY_TO_FPGA<0>	FMC_LA*<12>	G16	LA12_N	T6	busy_i[0]	In	set_property PACKAGE_PIN T6 [get_ports {busy_i[0]}]
BUSY_TO_FPGA<1>	FMC_LA*<13>	D18	LA13_N	U3	busy_i[1]	In	set_property PACKAGE_PIN U3 [get_ports {busy_i[1]}]
BUSY_TO_FPGA<3>	FMC_LA*<14>	C19	LA14_N	T8	busy_i[2]	In	set_property PACKAGE_PIN T8 [get_ports {busy_i[2]}]
BUSY_TO_FPGA<2>	FMC_LA*<15>	H20	LA15_N	L4	busy_i[3]	In	set_property PACKAGE_PIN L4 [get_ports {busy_i[3]}]
DUT_CLK_TO_FPGA<0>	FMC_LA*<16>	G19	LA16_N	L3	dut_clk_i[0]	In	set_property PACKAGE_PIN L3 [get_ports {dut_clk_i[0]}]
DUT_CLK_TO_FPGA<1>	FMC_LA*<17>	D21	LA17_N_CC	F3	dut_clk_i[1]	In	set_property PACKAGE_PIN F3 [get_ports {dut_clk_i[1]}]
DUT_CLK_TO_FPGA<2>	FMC_LA*<18>	C23	LA18_N_CC	D2	dut_clk_i[2]	In	set_property PACKAGE_PIN D2 [get_ports {dut_clk_i[2]}]
DUT_CLK_TO_FPGA<3>	FMC_LA*<19>	H23	LA19_N	G3	dut_clk_i[3]	In	set_property PACKAGE_PIN G3 [get_ports {dut_clk_i[3]}]
CONT_FROM_FPGA<0>	FMC_LA<0>	G6	LA00_P_CC	N5	cont_o[0]	Out	set_property PACKAGE_PIN N5 [get_ports {cont_o[0]}]
CONT_FROM_FPGA<1>	FMC_LA<1>	D8	LA01_P_CC	P4	cont_o[1]	Out	set_property PACKAGE_PIN P4 [get_ports {cont_o[1]}]
CONT_FROM_FPGA<2>	FMC_LA<2>	H7	LA02_P	M6	cont_o[2]	Out	set_property PACKAGE_PIN M6 [get_ports {cont_o[2]}]
CONT_FROM_FPGA<3>	FMC_LA<3>	G9	LA03_P	L6	cont_o[3]	Out	set_property PACKAGE_PIN L6 [get_ports {cont_o[3]}]
SPARE_FROM_FPGA<0>	FMC_LA<4>	H10	LA04_P	L1	spare_o[0]	Out	set_property PACKAGE_PIN L1 [get_ports {spare_o[0]}]
SPARE_FROM_FPGA<1>	FMC_LA<5>	D11	LA05_P	M4	spare_o[1]	Out	set_property PACKAGE_PIN M4 [get_ports {spare_o[1]}]
SPARE_FROM_FPGA<2>	FMC_LA<6>	C10	LA06_P	N2	spare_o[2]	Out	set_property PACKAGE_PIN N2 [get_ports {spare_o[2]}]
SPARE_FROM_FPGA<3>	FMC_LA<7>	H13	LA07_P	M3	spare_o[3]	Out	set_property PACKAGE_PIN M3 [get_ports {spare_o[3]}]
TRIG_FROM_FPGA<0>	FMC_LA<8>	G12	LA08_P	R6	triggers_o[0]	Out	set_property PACKAGE_PIN R6 [get_ports {triggers_o[0]}]
TRIG_FROM_FPGA<1>	FMC_LA<9>	D14	LA09_P	P2	triggers_o[1]	Out	set_property PACKAGE_PIN P2 [get_ports {triggers_o[1]}]
TRIG_FROM_FPGA<2>	FMC_LA<10>	C14	LA10_P	R1	triggers_o[2]	Out	set_property PACKAGE_PIN R1 [get_ports {triggers_o[2]}]
TRIG_FROM_FPGA<3>	FMC_LA<11>	H16	LA11_P	U1	triggers_o[3]	Out	set_property PACKAGE_PIN U1 [get_ports {triggers_o[3]}]
BUSY_FROM_FPGA<0>	FMC_LA<12>	G15	LA12_P	R7	busy_o[0]	Out	set_property PACKAGE_PIN R7 [get_ports {busy_o[0]}]
BUSY_FROM_FPGA<1>	FMC_LA<13>	D17	LA13_P	U4	busy_o[1]	Out	set_property PACKAGE_PIN U4 [get_ports {busy_o[1]}]
BUSY_FROM_FPGA<2>	FMC_LA<14>	C18	LA14_P	R8	busy_o[2]	Out	set_property PACKAGE_PIN R8 [get_ports {busy_o[2]}]
BUSY_FROM_FPGA<3>	FMC_LA<15>	H19	LA15_P	K5	busy_o[3]	Out	set_property PACKAGE_PIN K5 [get_ports {busy_o[3]}]
DUT_CLK_FROM_FPGA<0>	FMC_LA<16>	G18	LA16_P	K3	dut_clk_o[0]	Out	set_property PACKAGE_PIN K3 [get_ports {dut_clk_o[0]}]
DUT_CLK_FROM_FPGA<1>	FMC_LA<17>	D20	LA17_P_CC	F4	dut_clk_o[1]	Out	set_property PACKAGE_PIN F4 [get_ports {dut_clk_o[1]}]
DUT_CLK_FROM_FPGA<2>	FMC_LA<18>	C22	LA18_P_CC	E2	dut_clk_o[2]	Out	set_property PACKAGE_PIN E2 [get_ports {dut_clk_o[2]}]
DUT_CLK_FROM_FPGA<3>	FMC_LA<19>	H22	LA19_P	G4	dut_clk_o[3]	Out	set_property PACKAGE_PIN G4 [get_ports {dut_clk_o[3]}]

12.3 Schematics for main TLU electronics.



	Mon May 08 11:23:42 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS
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H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

TITLE fmc_tlu_v1_lib

MODULE: fmc_tlu_toplevel_e

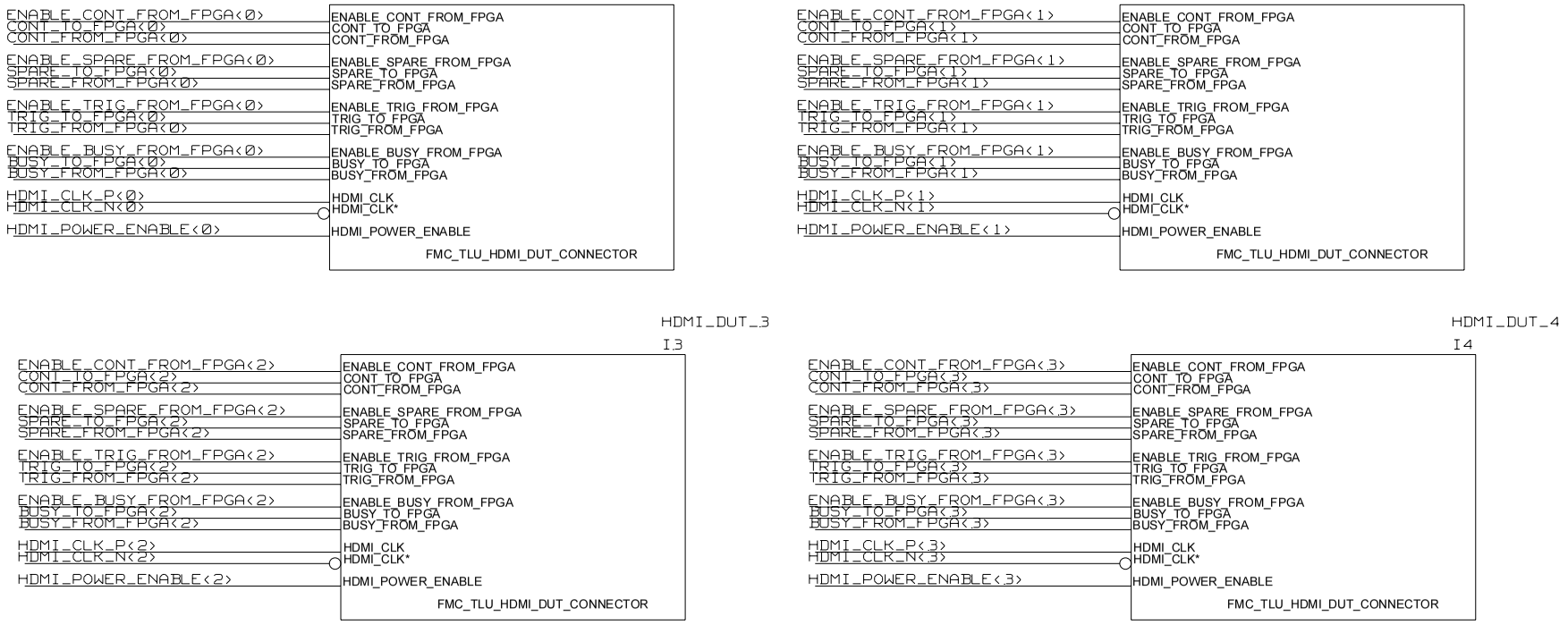
FMC CONNECTOR

AND I2C EEPROM

A2

MODULE PAGE: 1 OF 7
OVERALL PAGE: 1 OF 29

TOTAL NO. OF SHEETS



	Thu May 04 13:37:48 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

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HIGH ENERGY PHYSICS GROUP
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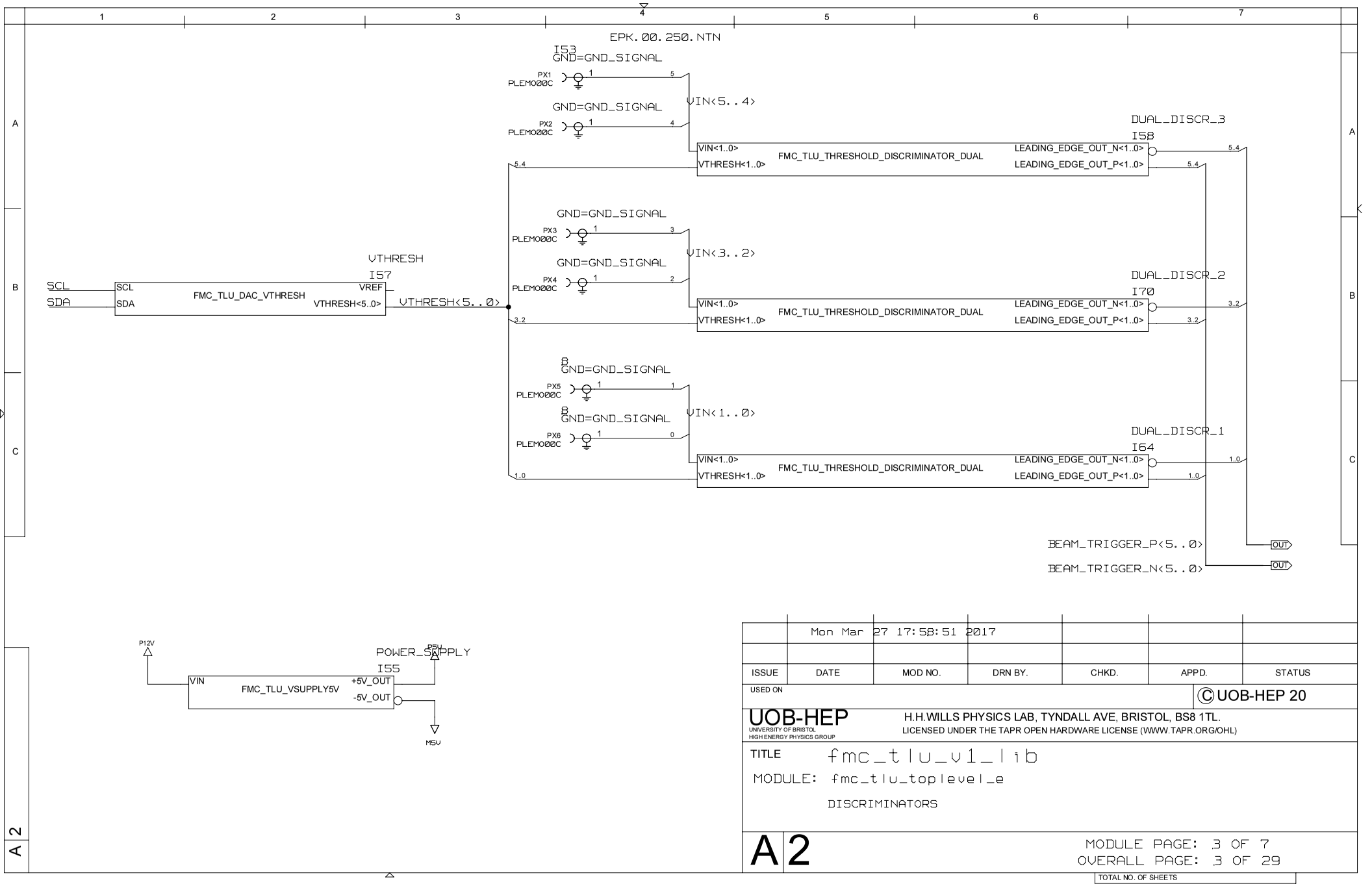
TITLE fmc_tlu_v1_lib

MODULE: fmc_tlu_toplevel_e

FRONT PANEL DUT CONNECTORS
3 X HDMI (DUT ONLY)
1 X HDMI (DUT OR UPLINK)

A2



	Mon Mar 27 17:58:51 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS
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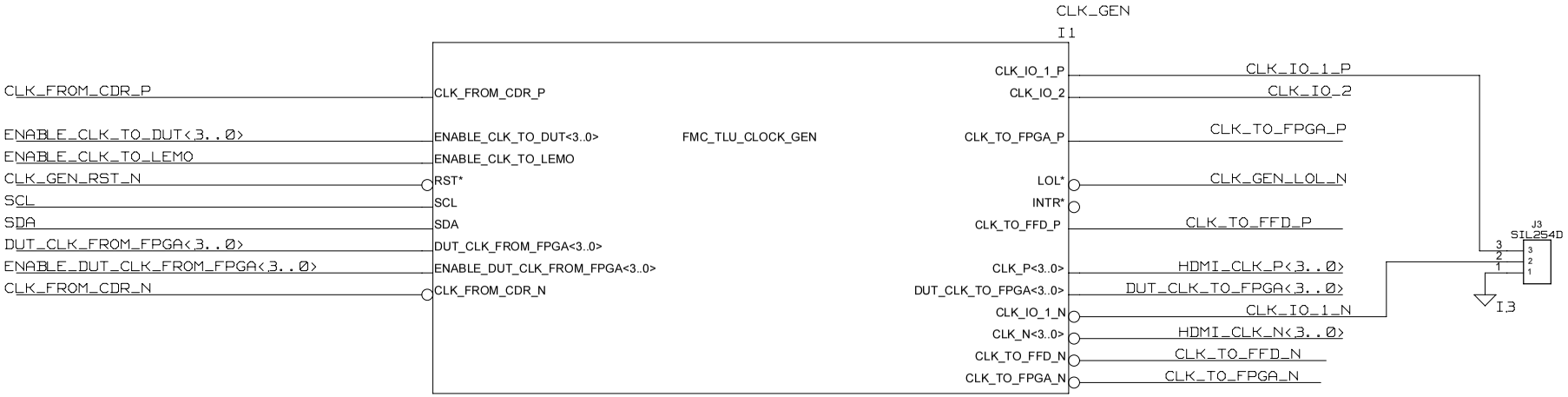
TITLE fmc_tlu_v1_lib

MODULE: fmc_tlu_toplevel_e

DISCRIMINATORS

A2



	Thu Mar 30 17:10:57 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

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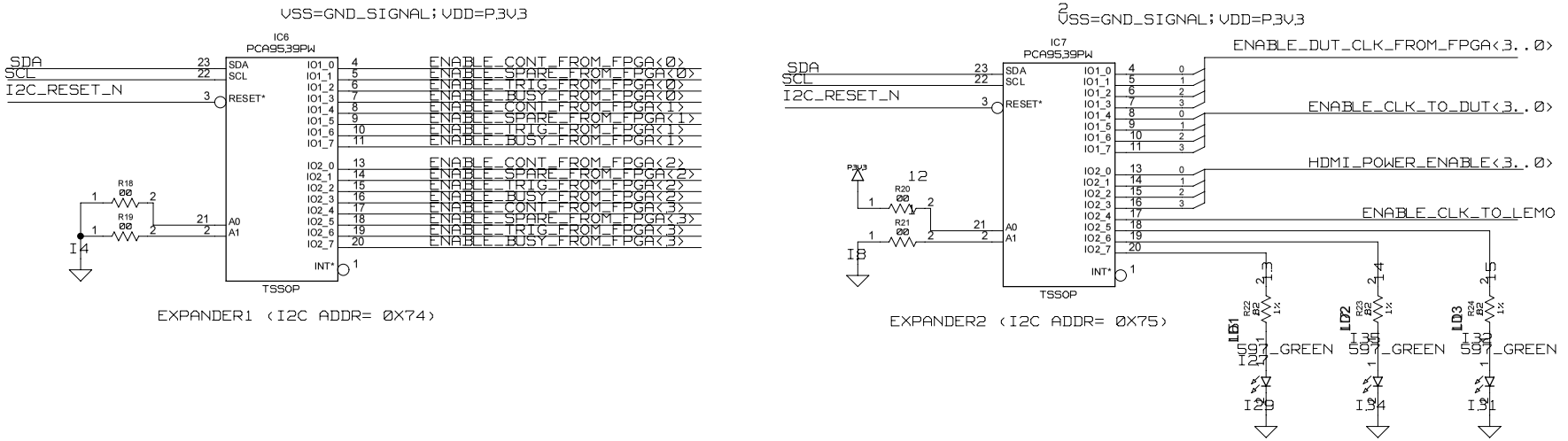
TITLE fmc_tlu_v1_lib CLOCK GENERATION

MODULE: fmc_tlu_toplevel_e

A2



	Mon Mar 27 17:58:54 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

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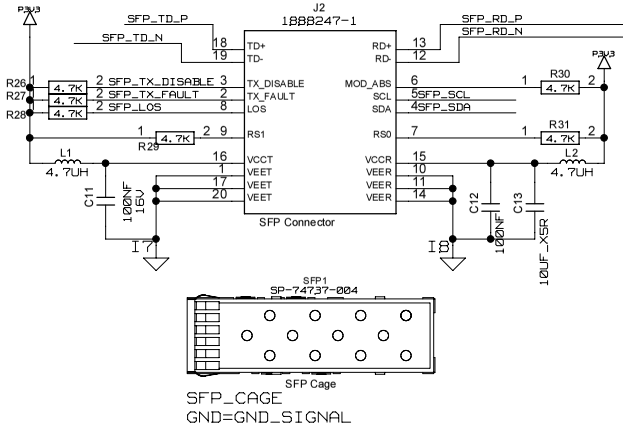
TITLE fmc_tlu_v1_lib I2C I/O EXTENDERS

MODULE: fmc_tlu_toplevel_e

A2

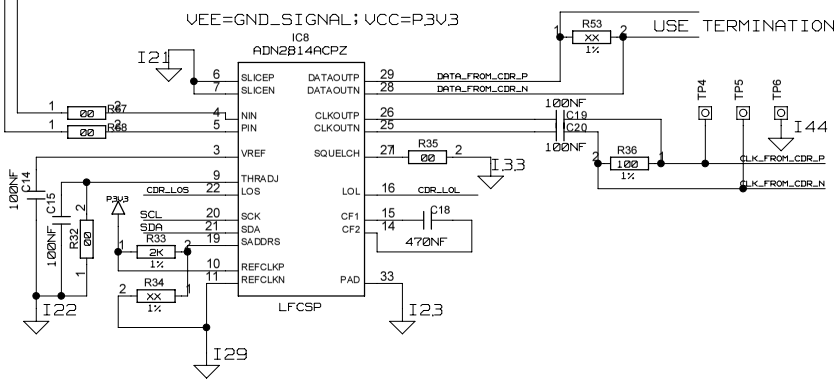
SN65LVDS2 OR SN65LVDT2
SN65LVDT2 HAS TERMINATION.
SN65LVDS2 REQUIRES EXTERNAL TERMINATION.

SFP_CAGE



SFP_CAGE
GND=GND_SIGNAL

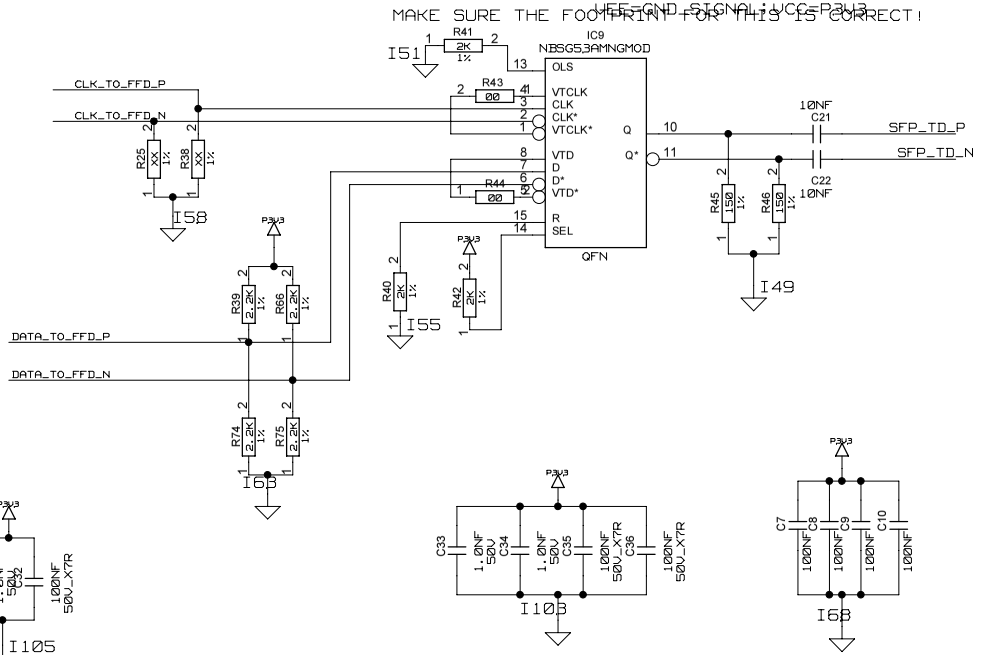
CDR (I2C ADDR= 0X60)
VEE=GND_SIGNAL; VCC=P3V3

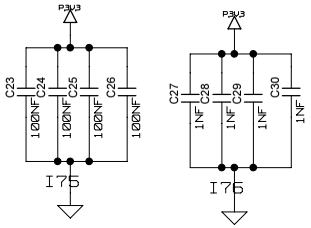


USE TERMINATION IN FPGA IF POSSIBLE

( )
(GND_SIGNAL: 17; VEE: 12; VCC: 9, 16)
VEE=GND_SIGNAL; VCC=P3V3

MAKE SURE THE FOOTPRINT FOR THIS IS CORRECT!





	Fri May 05 14:40:28 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

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TITLE fmc_tlu_v1_lib

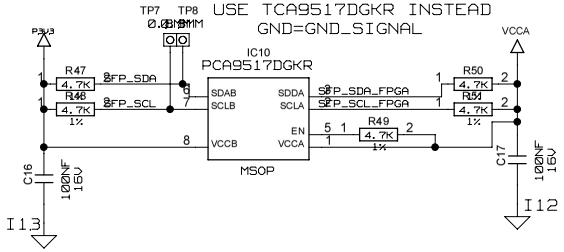
MODULE: fmc_tlu_toplevel_e

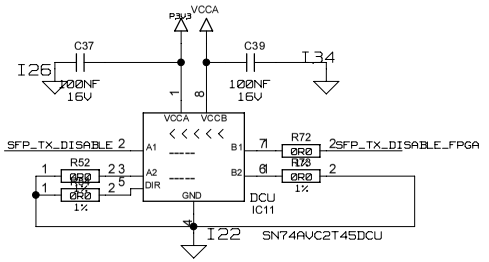
SFP INTERFACE

A2

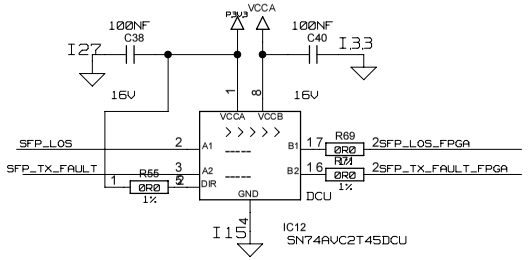
MODULE PAGE: 6 OF 7
OVERALL PAGE: 6 OF 29

TOTAL NO. OF SHEETS





DIR LOW : B -> A
DIR HIGH: A -> B



	Thu Mar 30 17:11:07 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

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TITLE fmc_tlu_v1_lib

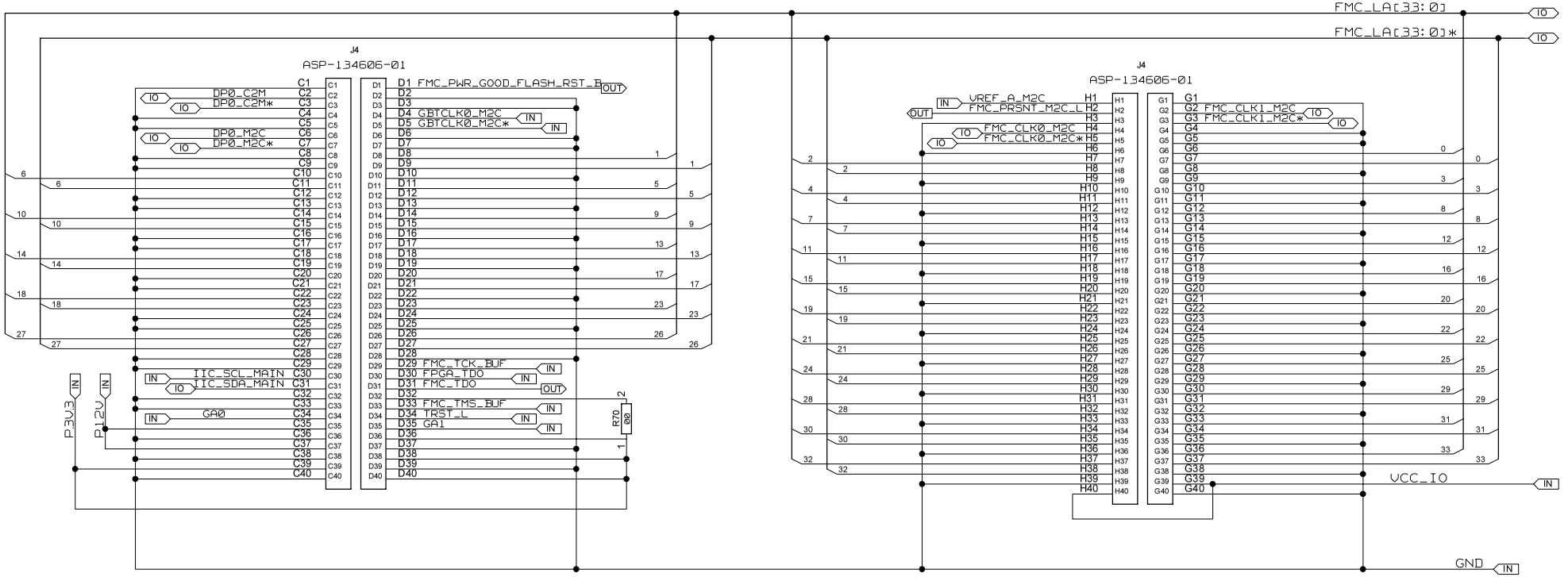
MODULE: fmc_tlu_toplevel_e

LEVEL TRANSLATORS

A2

MODULE PAGE: 7 OF 7
OVERALL PAGE: 7 OF 29

TOTAL NO. OF SHEETS



	Thu Mar 30 11:19:40 2017					
			D. CUSSANS	C. JESKE	D. CUSSANS	
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

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TITLE fmc_tlu_v1_lib

MODULE: pc036a_fmc_lpc_connector

FMC LPC

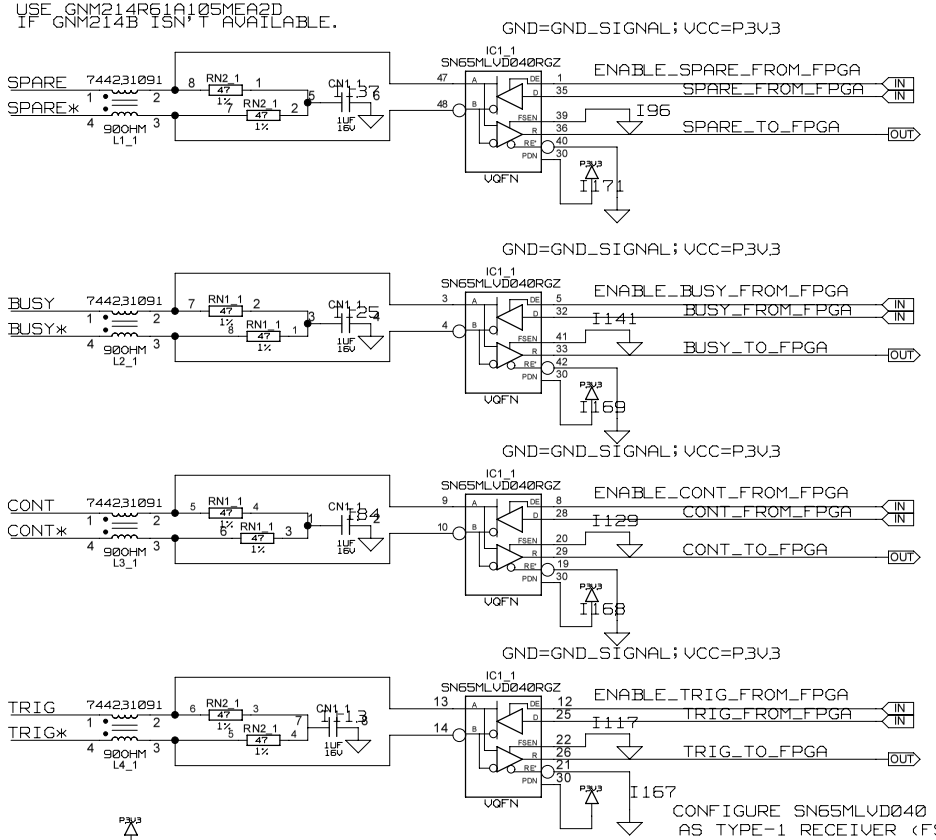
A2

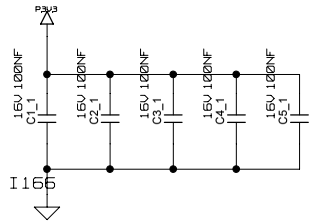
MODULE PAGE: 1 OF 1

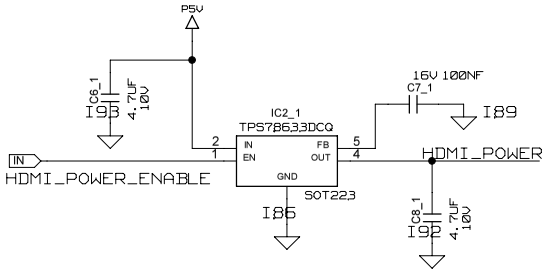
OVERALL PAGE: 8 OF 29

TOTAL NO. OF SHEETS

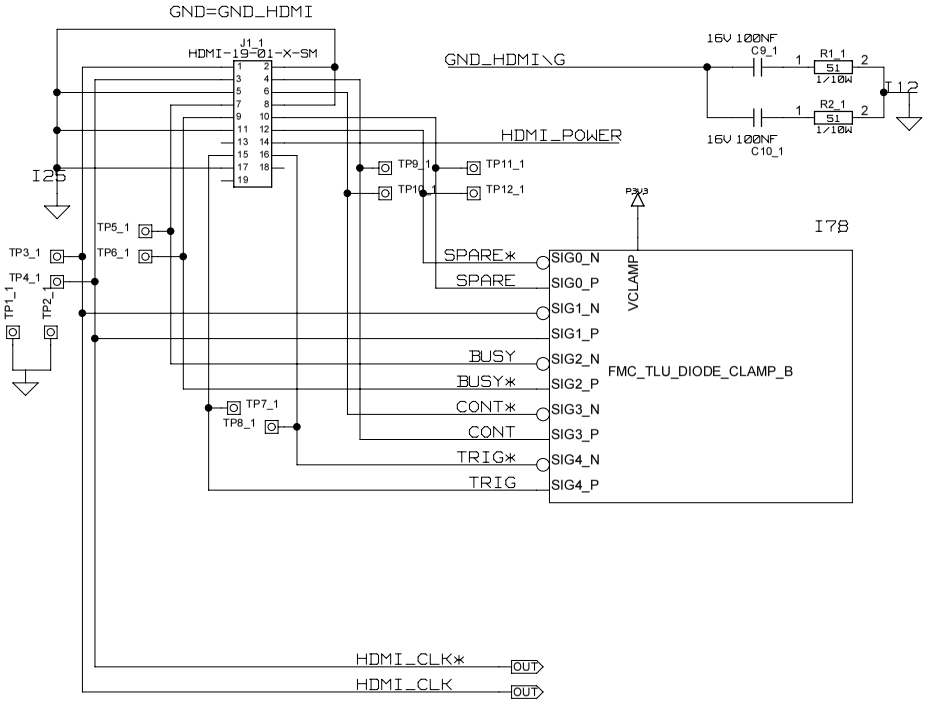
USE GNM214R61A105MEA2D
IF GNM214B ISN'T AVAILABLE.







REPLACE SAMTEC CONNECTOR WITH MOLEX 47151-0002



	Thu Apr 13 16:21:16 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

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TITLE fmc_tlu_v1_lib

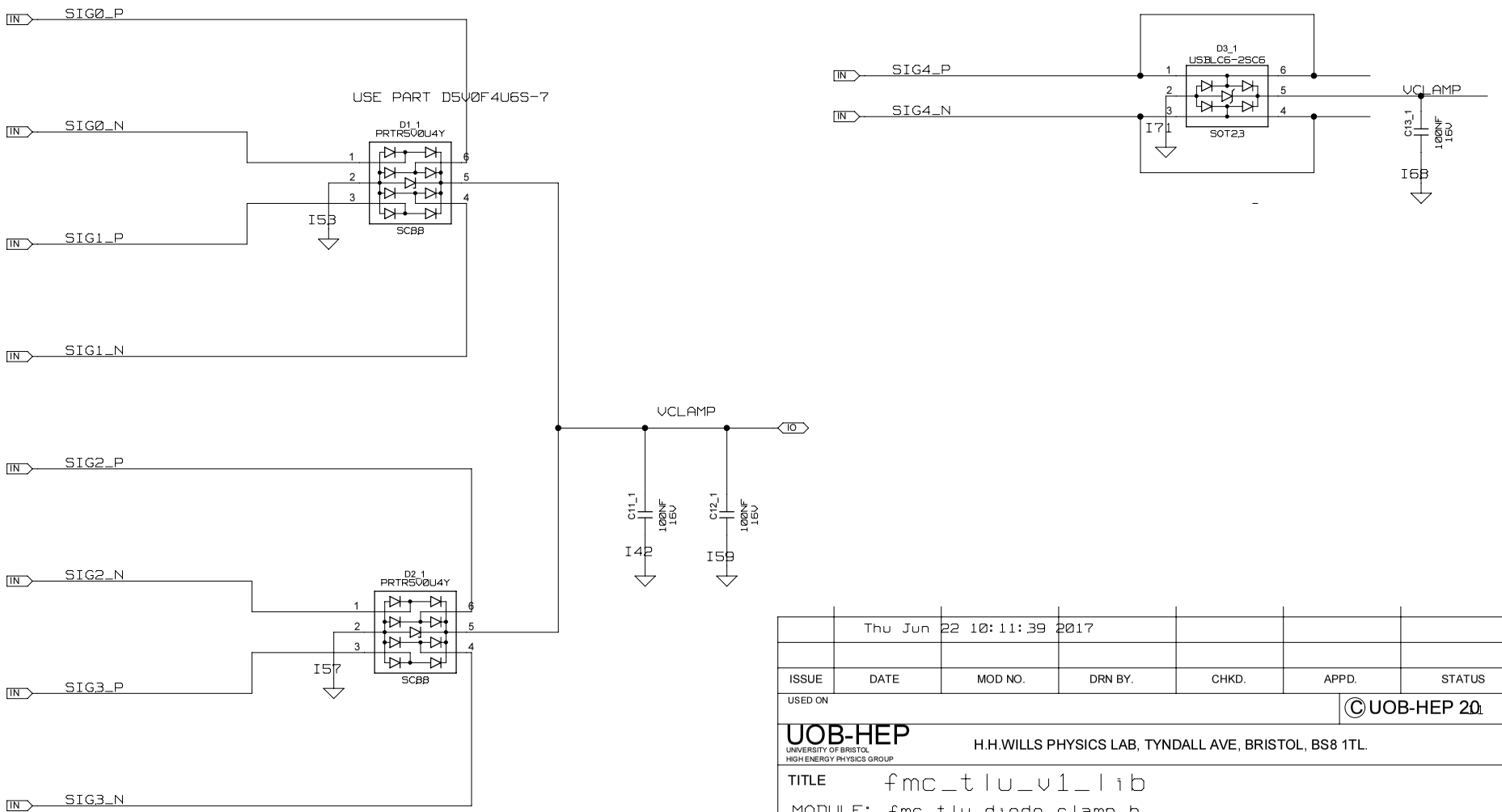
HDMI FRONT PANEL CONNECTOR

MODULE: fmc_tlu_hdmi_dut_connector

A2

MODULE PAGE: 1 OF 1
OVERALL PAGE: 9 OF 29

TOTAL NO. OF SHEETS



	Thu Jun 22 10:11:39 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

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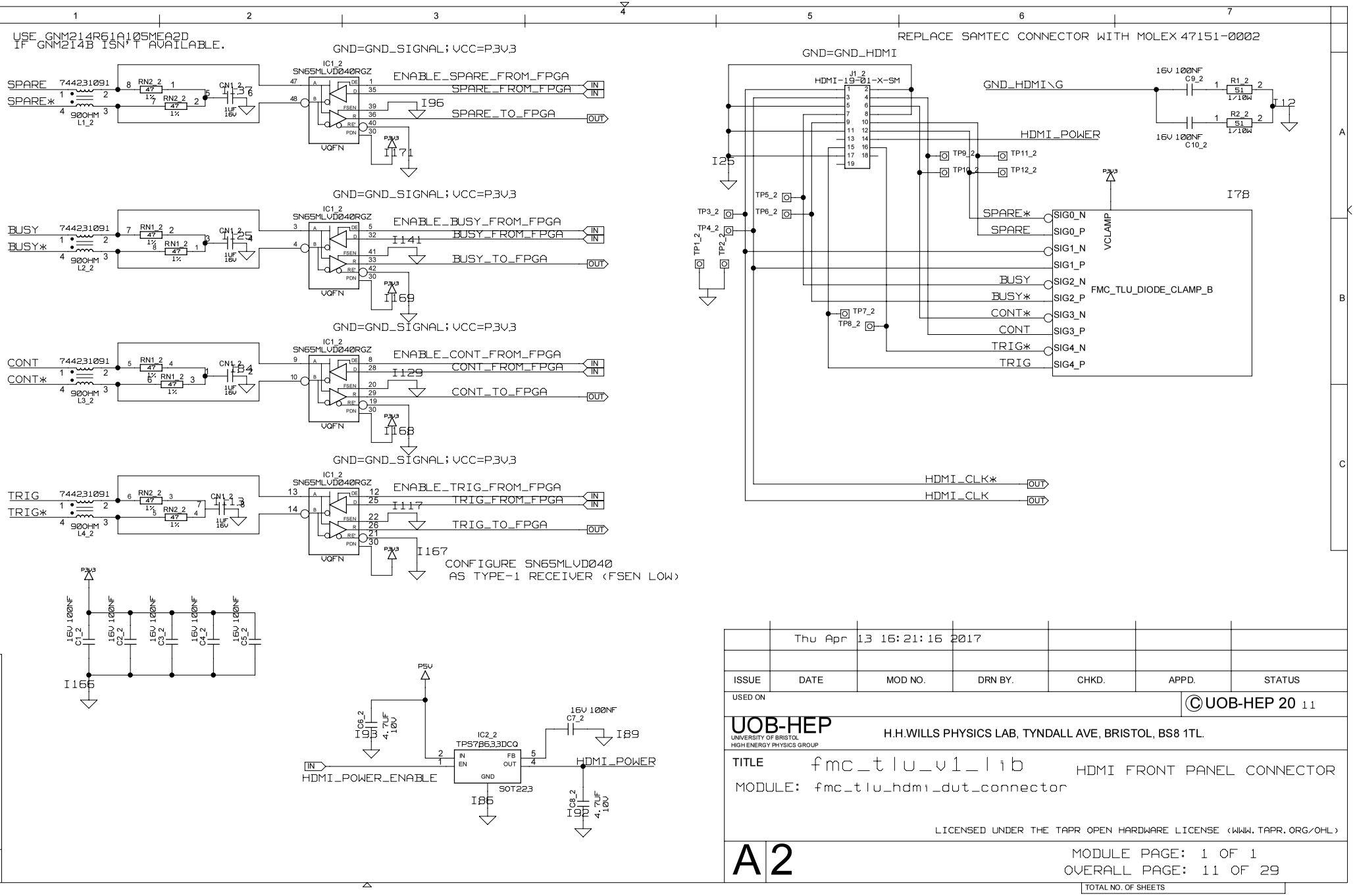
TITLE fmc_tlu_v1_lib

MODULE: fmc_tlu_diode_clamp_b

A2

MODULE PAGE: 1 OF 1
OVERALL PAGE: 10 OF 29

TOTAL NO. OF SHEETS



	Thu Apr 13 16:21:16 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS
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HIGH ENERGY PHYSICS GROUP

H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

TITLE fmc_tlu_v1_lib

HDMI FRONT PANEL CONNECTOR

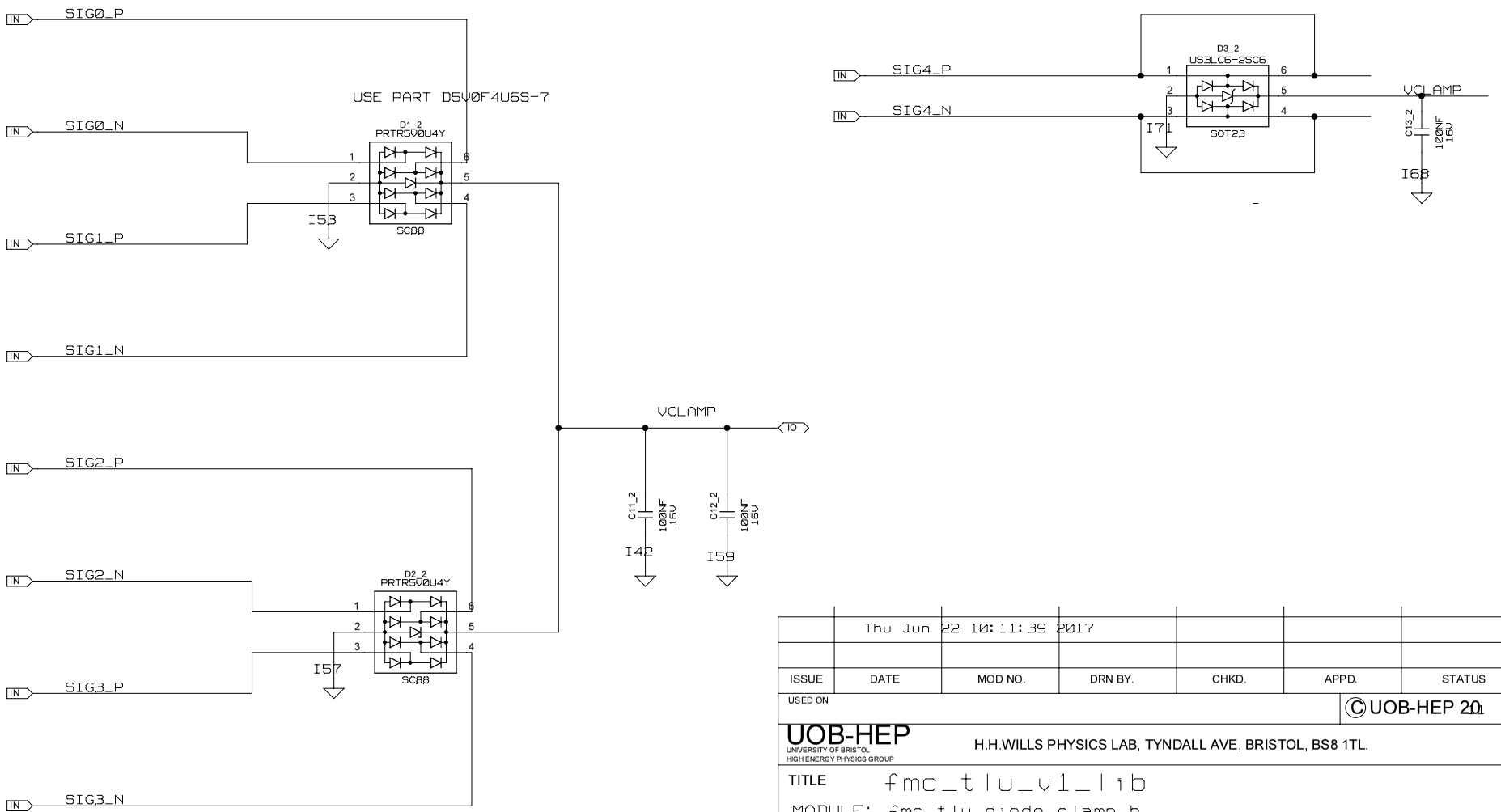
MODULE: fmc_tlu_hdmi_dut_connector

A2

MODULE PAGE: 1 OF 1

OVERALL PAGE: 11 OF 29

TOTAL NO. OF SHEETS



	Thu Jun 22 10:11:39 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

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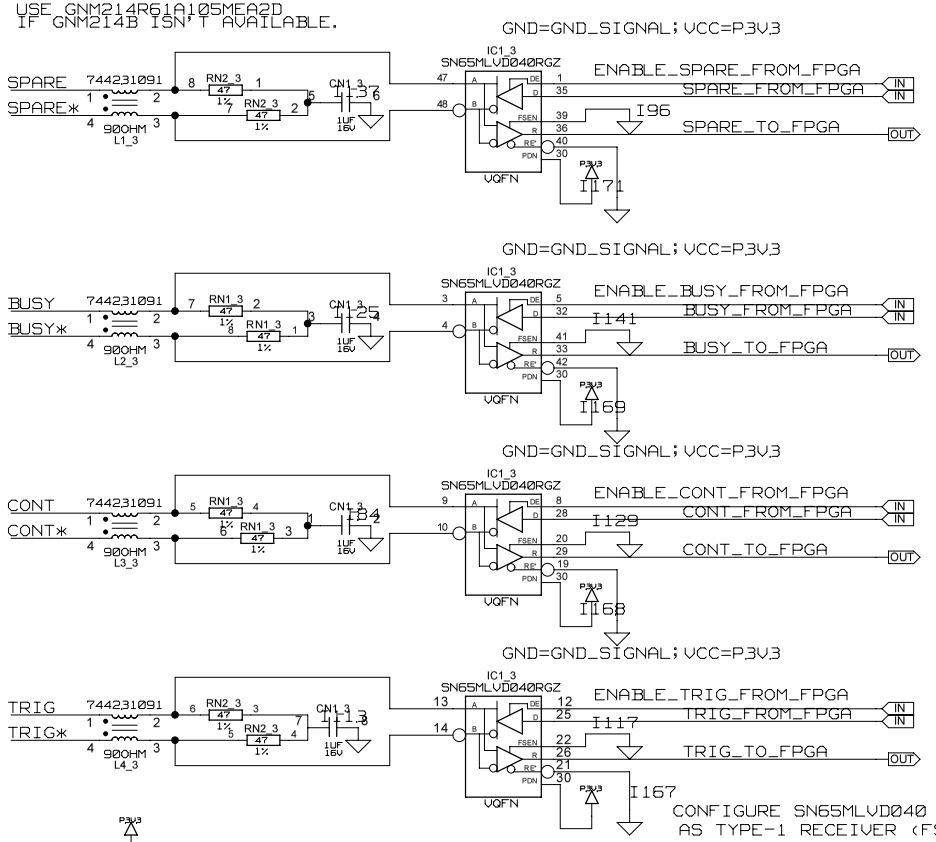
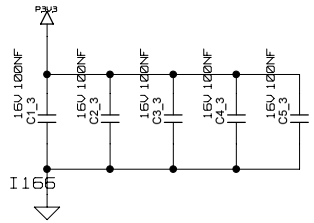
TITLE fmc_tlu_v1_lib

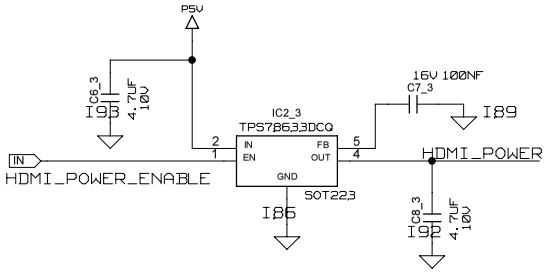
MODULE: fmc_tlu_diode_clamp_b

A2

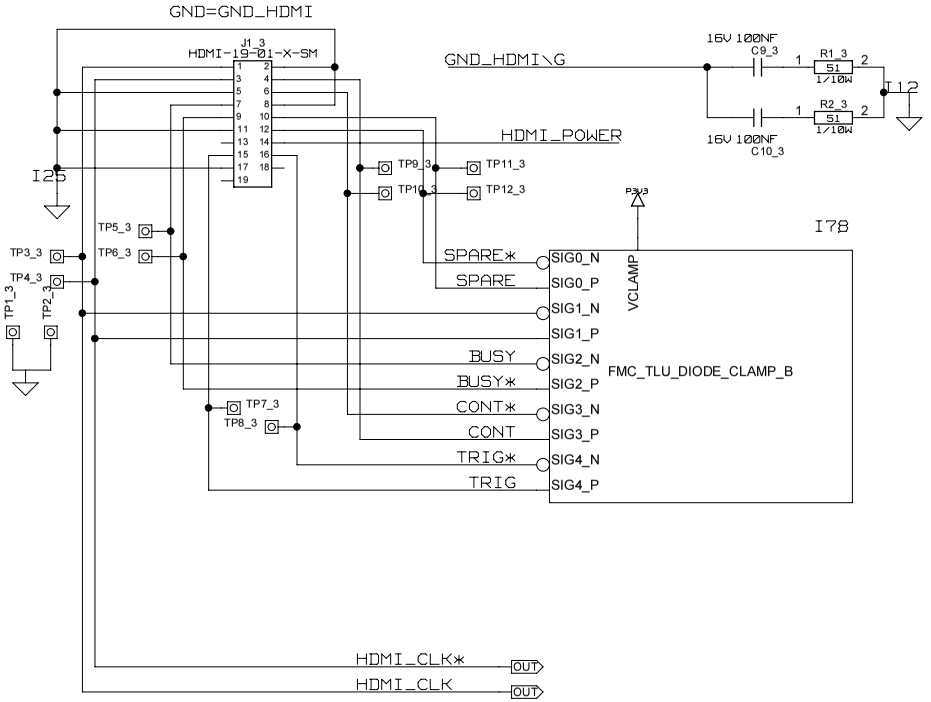
USE GNM214R61A105MEA2D
IF GNM214B ISN'T AVAILABLE.







REPLACE SAMTEC CONNECTOR WITH MOLEX 47151-0002



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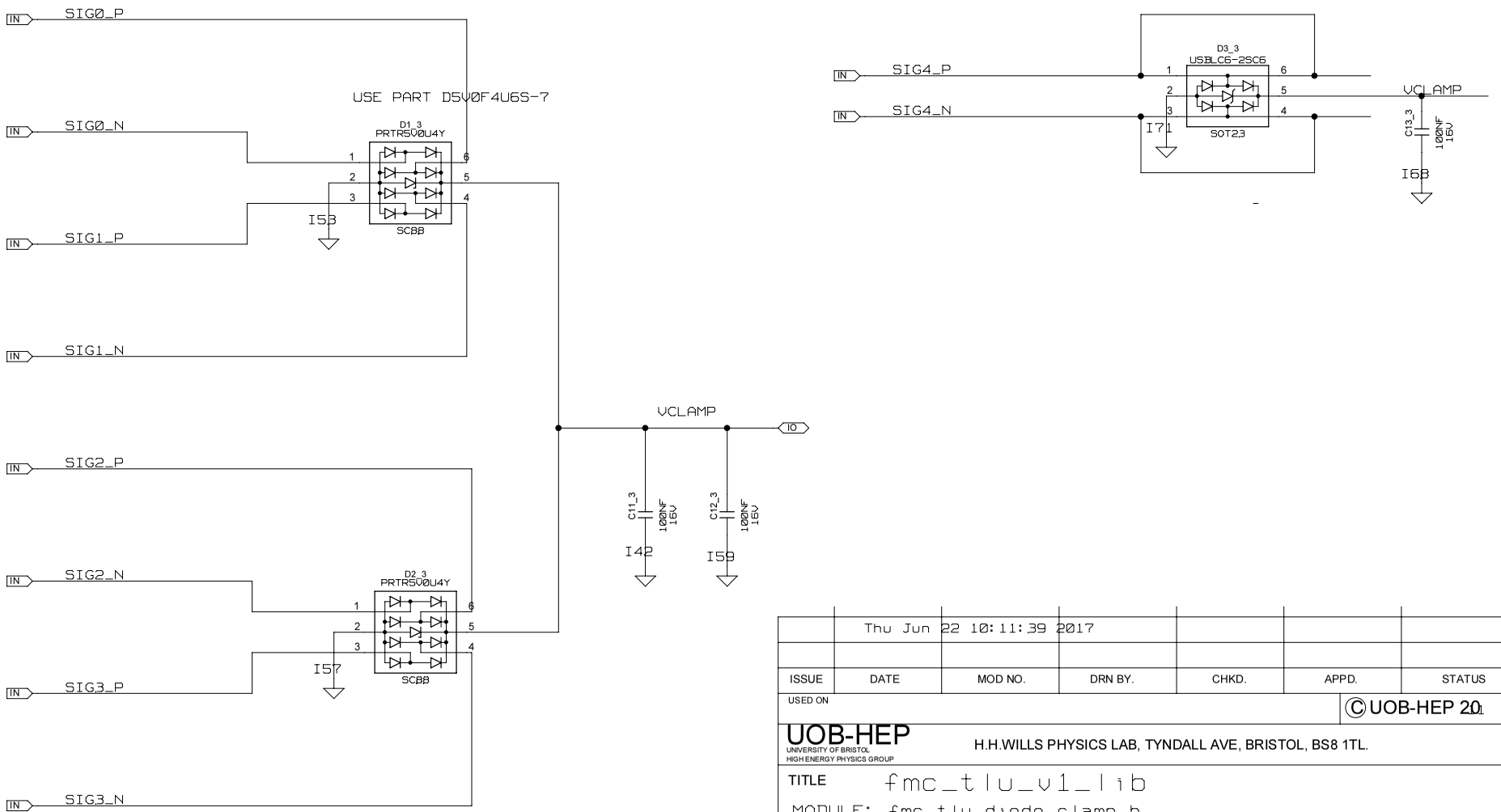
TITLE fmc_tlu_v1_lib
HDMI FRONT PANEL CONNECTOR
MODULE: fmc_tlu_hdmi_dut_connector

A2

MODULE PAGE: 1 OF 1
OVERALL PAGE: 13 OF 29
TOTAL NO. OF SHEETS



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TITLE fmc_tlu_v1_lib

MODULE: fmc_tlu_diode_clamp_b

A2

USE GNM214R61A105MEA2D
IF GNM214B ISN'T AVAILABLE.

REPLACE SAMTEC CONNECTOR WITH MOLEX 47151-0002

GND=GND_SIGNAL; VCC=P3V3

SPARE
SPARE*
744231091
L1_4
RN2_4 47 1% 7
RN1_4 47 1% 8
CN1_4 I137 1UF 16V
IC1_4 SN65MLVD040RGZ
ENABLE_SPARE_FROM_FPGA
SPARE_FROM_FPGA
I96
SPARE_TO_FPGA
I171

GND=GND_SIGNAL; VCC=P3V3

BUSY
BUSY*
744231091
L2_4
RN1_4 47 1% 7
RN1_4 47 1% 8
CN1_4 I125 1UF 16V
IC1_4 SN65MLVD040RGZ
ENABLE_BUSY_FROM_FPGA
BUSY_FROM_FPGA
I141
BUSY_TO_FPGA
I169

GND=GND_SIGNAL; VCC=P3V3

CONT
CONT*
744231091
L3_4
RN1_4 47 1% 5
RN1_4 47 1% 6
CN1_4 I134 1UF 16V
IC1_4 SN65MLVD040RGZ
ENABLE_CONT_FROM_FPGA
CONT_FROM_FPGA
I129
CONT_TO_FPGA
I168

GND=GND_SIGNAL; VCC=P3V3

TRIG
TRIG*
744231091
L4_4
RN2_4 47 1% 6
RN2_4 47 1% 5
CN1_4 I133 1UF 16V
IC1_4 SN65MLVD040RGZ
ENABLE_TRIG_FROM_FPGA
TRIG_FROM_FPGA
I117
TRIG_TO_FPGA
I167

CONFIGURE SN65MLVD040
AS TYPE-1 RECEIVER (FSEN LOW)

P3V3
16V 100NF C1_4 I166
16V 100NF C2_4
16V 100NF C3_4
16V 100NF C4_4
16V 100NF C5_4

P5V
C6_4 4.7UF 10V I193
IC2_4 TPS78633DCQ SOT223
IN HDMI_POWER_ENABLE
EN
IN
FB
OUT
GND
I186
16V 100NF C7_4 I189
HDMI_POWER
C8_4 4.7UF 10V I192

GND=GND_HDMI

J1_4 HDMI-19-01-X-SM
GND_HDMI\G
16V 100NF C9_4
R1_4 51 1/10W
I112
16V 100NF C10_4
R2_4 51 1/10W
HDMI_POWER
I125
TP9_4 TP11_4
TP10_4 TP12_4
P3V3
I178
TP5_4 TP6_4
TP3_4 TP4_4
TP1_4 TP2_4
TP7_4 TP8_4
SPARE*
SPARE
BUSY
BUSY*
CONT*
CONT
TRIG*
TRIG
SIG0_N
SIG0_P
SIG1_N
SIG1_P
SIG2_N
SIG2_P
SIG3_N
SIG3_P
SIG4_N
SIG4_P
VCLAMP
FMC_TLU_DIODE_CLAMP_B
HDMI_CLK*
HDMI_CLK

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	Thu Apr 13 16:21:16 2017					

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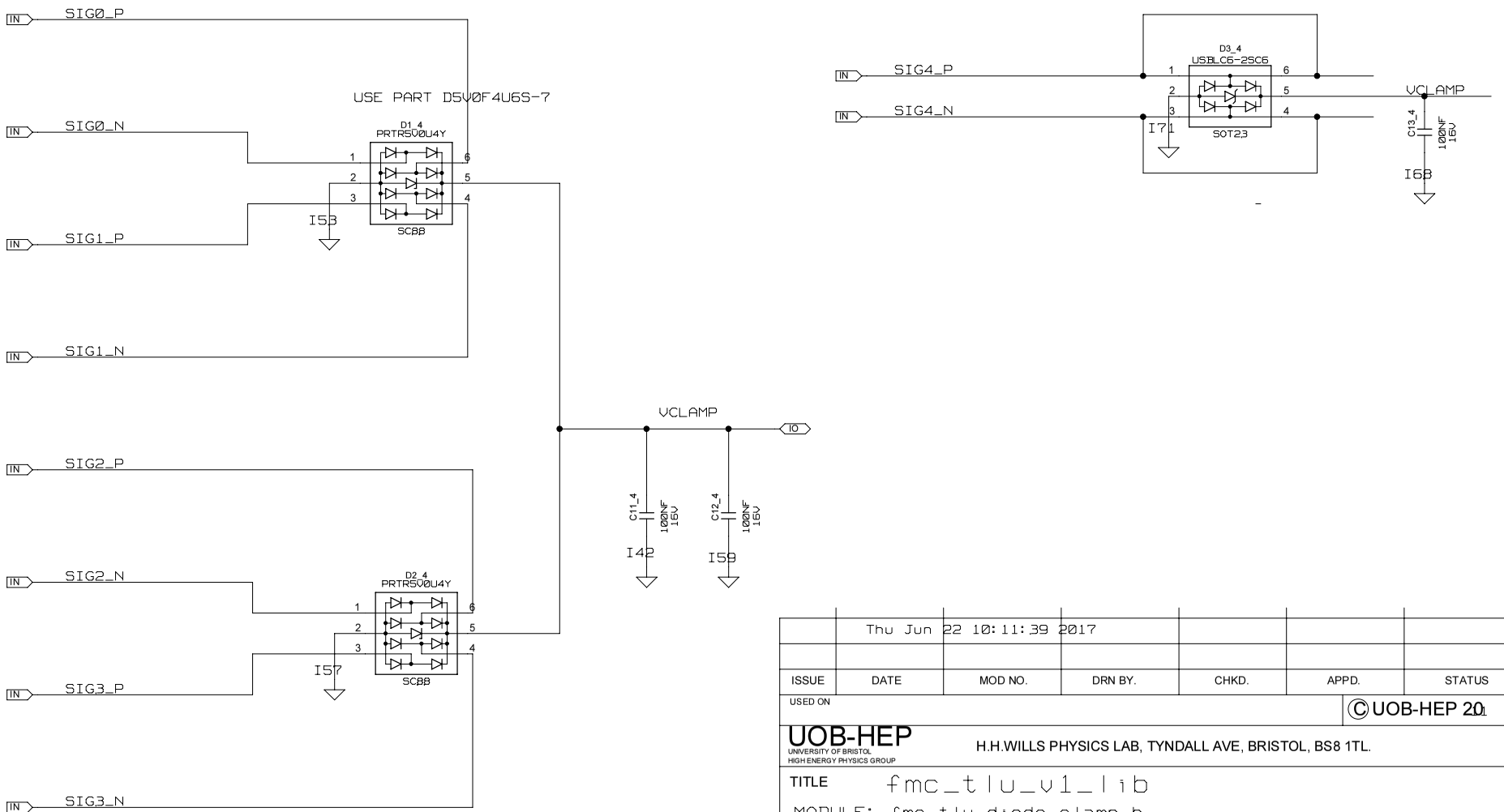
TITLE fmc_tlu_v1_lib
HDMI FRONT PANEL CONNECTOR
MODULE: fmc_tlu_hdmi_dut_connector

A2



	Thu Jun 22 10:11:39 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

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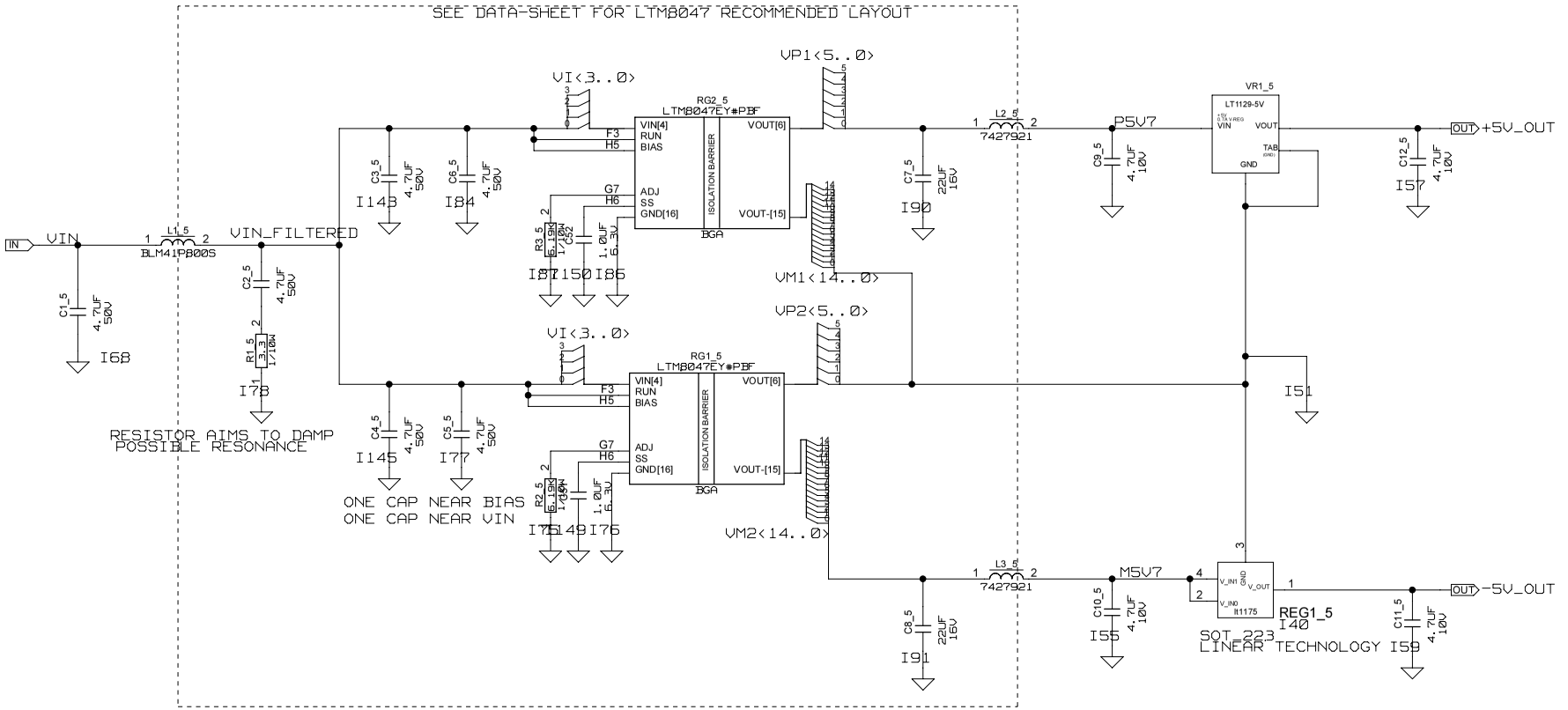
TITLE fmc_tlu_v1_lib

MODULE: fmc_tlu_diode_clamp_b

A2



	Fri May 05 14:39:22 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS
USED ON						©UOB-HEP 20

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TITLE fmc_tlu_v1_lib

MODULE: fmc_tlu_vsupply5v

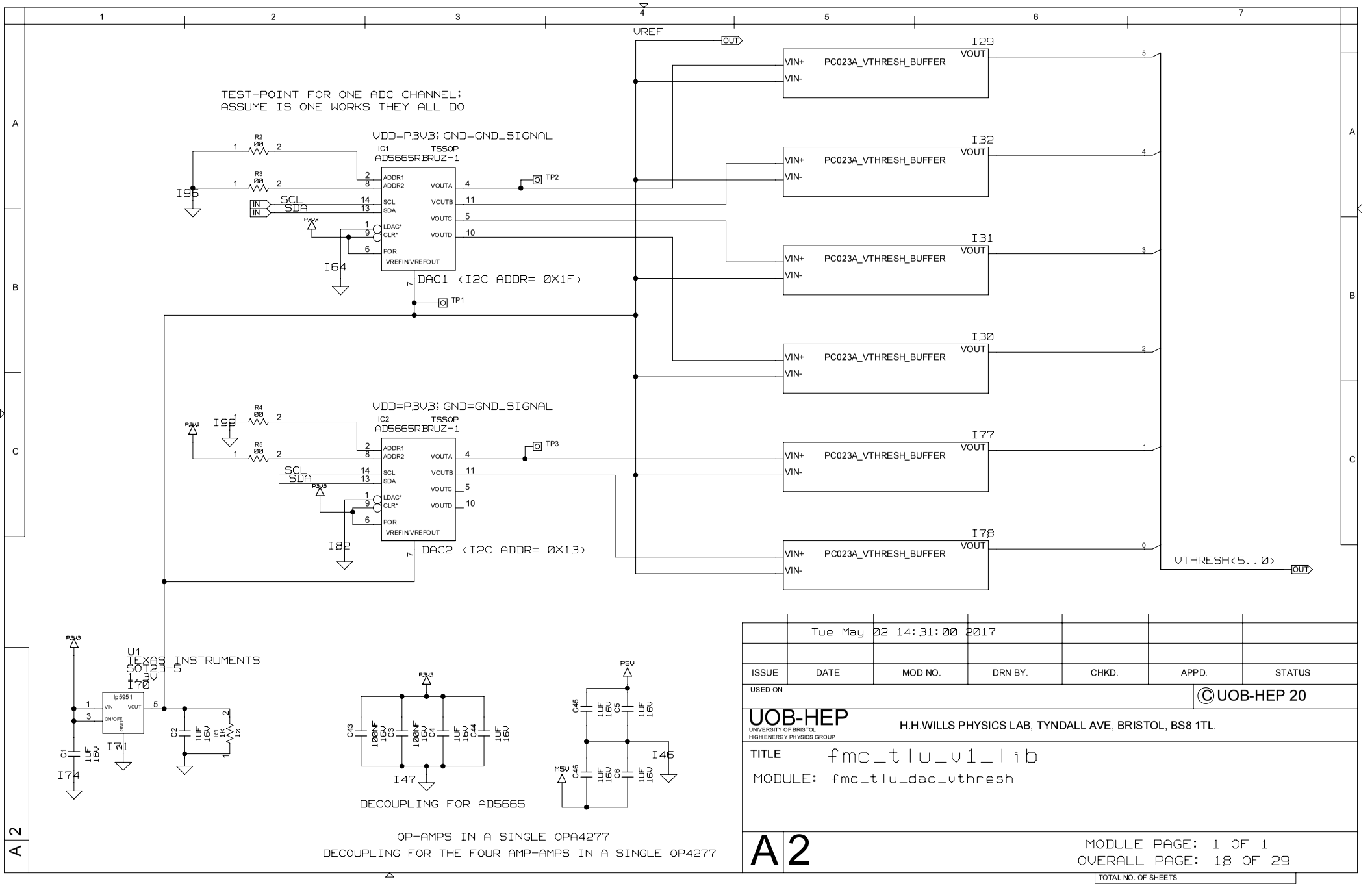
SUPPLY_DIGITAL

OVERALL PAGE: 17 OF 29

A2

MODULE PAGE: 1 OF 1

TOTAL NO. OF SHEETS



	Tue May 02 14:31:00 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

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TITLE fmc_tlu_v1_lib

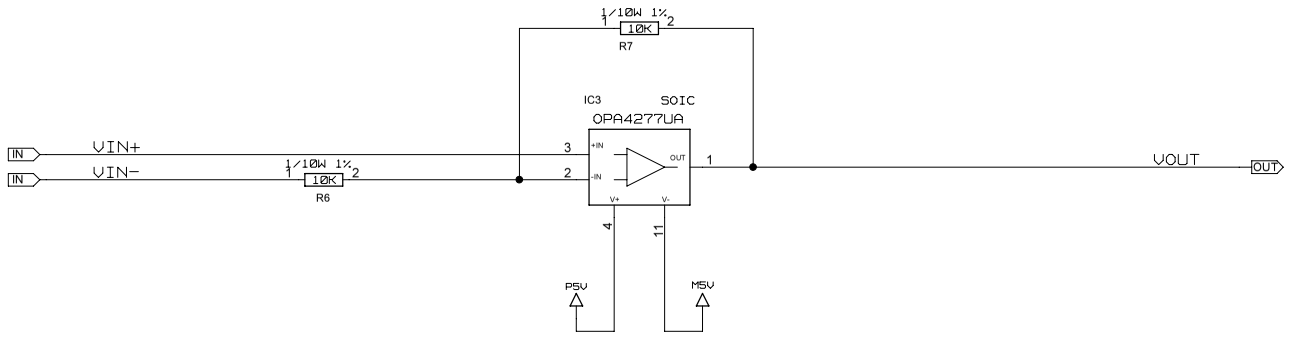
MODULE: fmc_tlu_dac_vthresh

A2

MODULE PAGE: 1 OF 1
OVERALL PAGE: 18 OF 29

TOTAL NO. OF SHEETS

INVERTING BUFFER WITH X-1 GAIN



	Mon Mar 27 17:58:27 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON

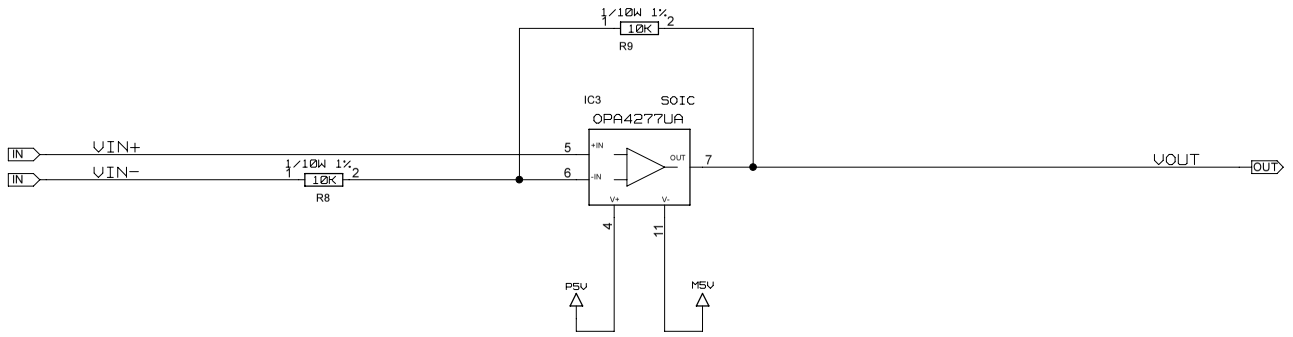
UOB-HEP
UNIVERSITY OF BRISTOL
HIGH ENERGY PHYSICS GROUP
H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

TITLE fmc_tlu_v1_lib

MODULE: pc023a_vthresh_buffer

A2

INVERTING BUFFER WITH X-1 GAIN



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TITLE fmc_tlu_v1_lib

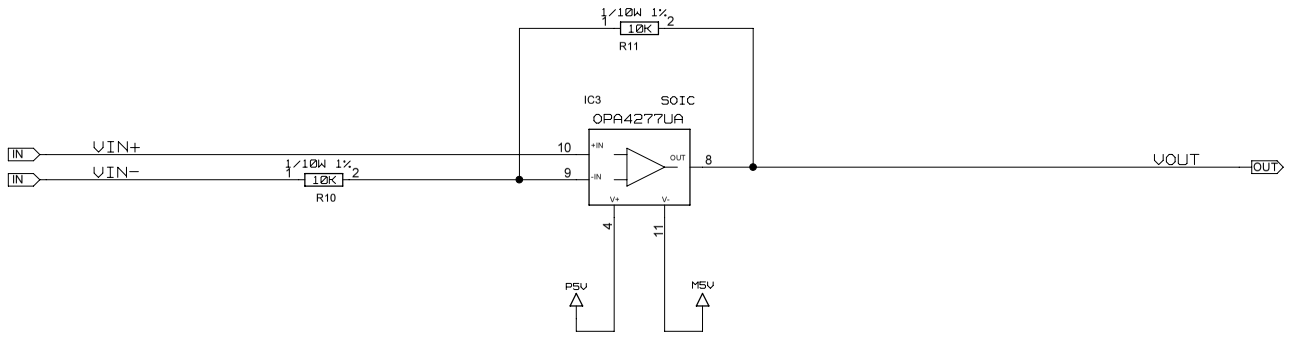
MODULE: pc023a_vthresh_buffer

A2

MODULE PAGE: 1 OF 1
OVERALL PAGE: 20 OF 29

TOTAL NO. OF SHEETS

INVERTING BUFFER WITH X-1 GAIN



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TITLE fmc_tlu_v1_lib

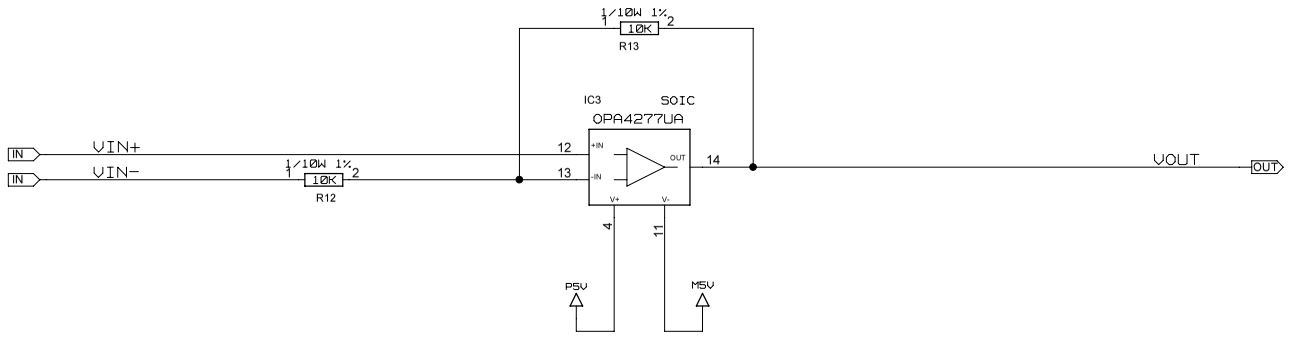
MODULE: pc023a_vthresh_buffer

A2

MODULE PAGE: 1 OF 1
OVERALL PAGE: 21 OF 29

TOTAL NO. OF SHEETS

INVERTING BUFFER WITH X-1 GAIN



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TITLE fmc_tlu_v1_lib

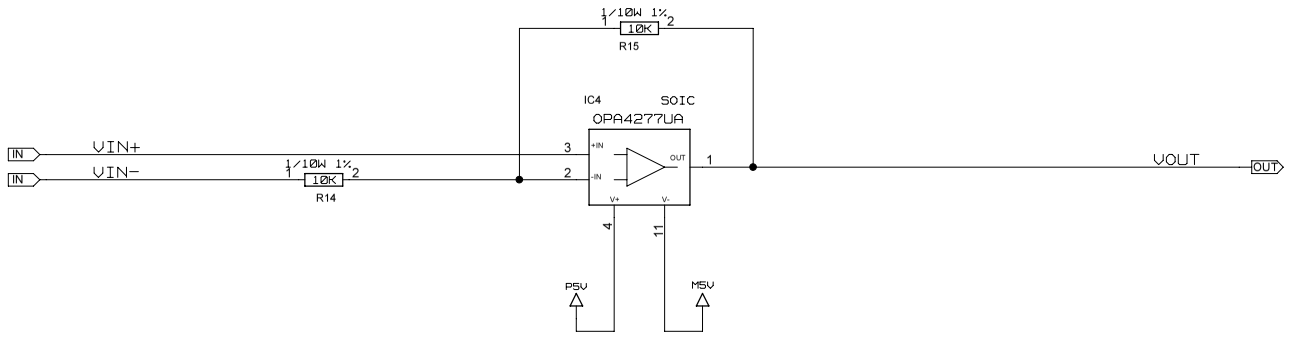
MODULE: pc023a_vthresh_buffer

A2

MODULE PAGE: 1 OF 1
OVERALL PAGE: 22 OF 29

TOTAL NO. OF SHEETS

INVERTING BUFFER WITH X-1 GAIN



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TITLE fmc_tlu_v1_lib

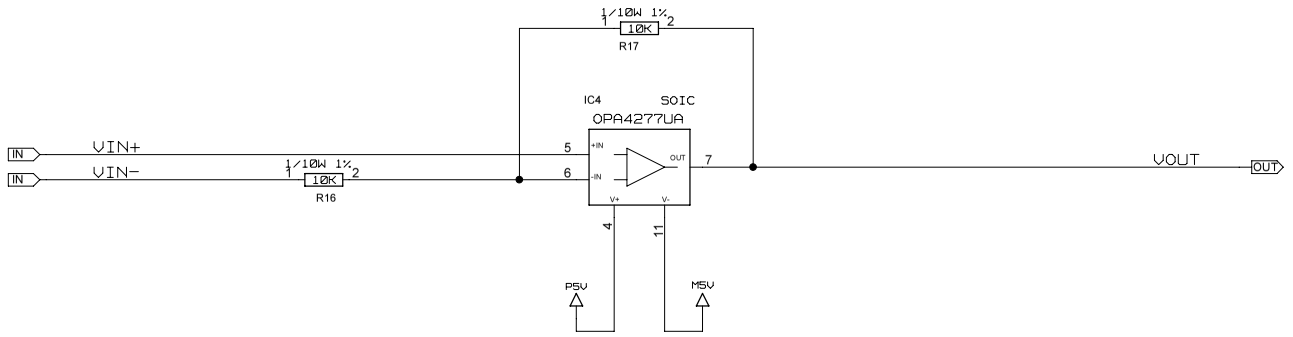
MODULE: pc023a_vthresh_buffer

A2

MODULE PAGE: 1 OF 1
OVERALL PAGE: 23 OF 29

TOTAL NO. OF SHEETS

INVERTING BUFFER WITH X-1 GAIN



	Mon Mar 27 17:58:27 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

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TITLE fmc_tlu_v1_lib

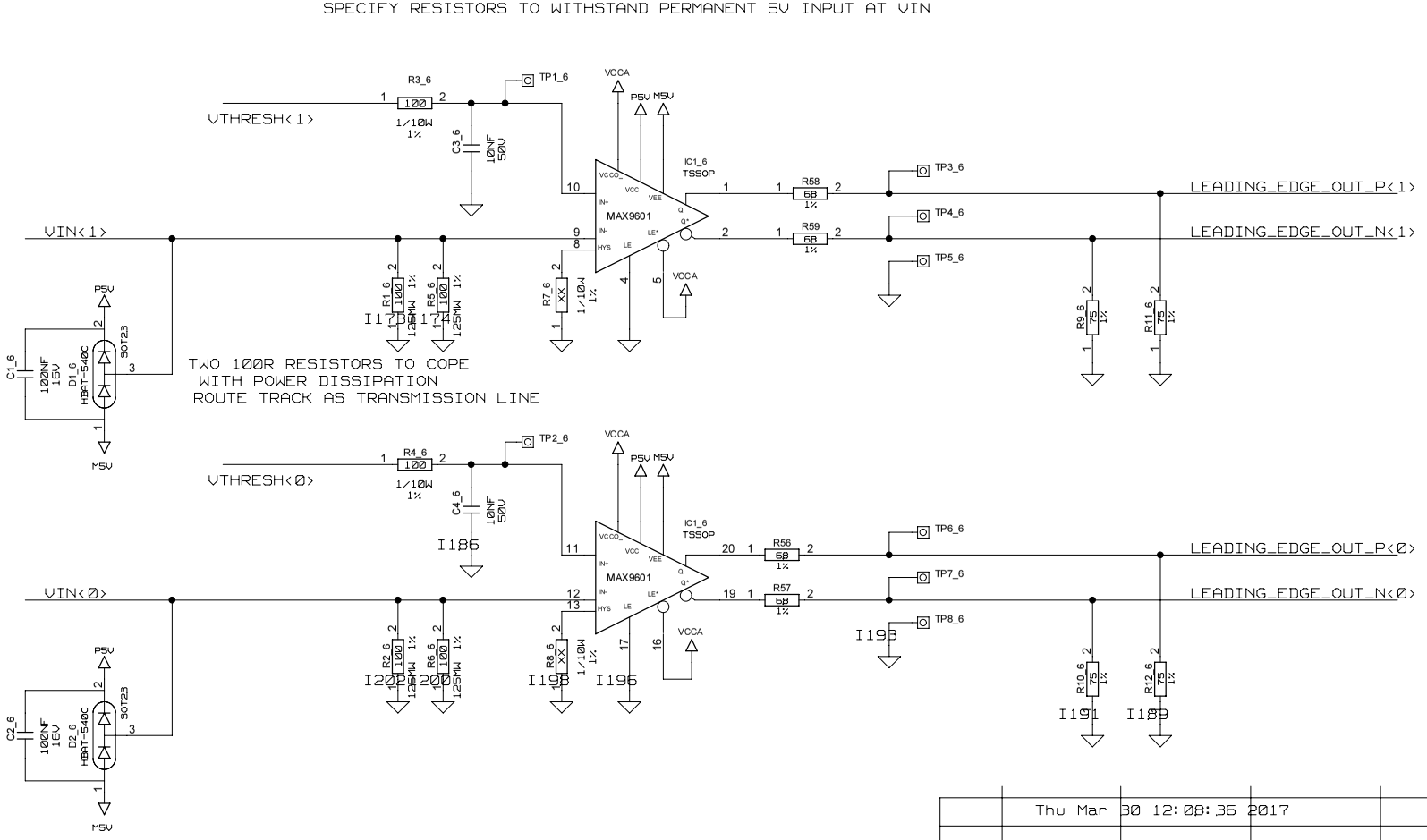
MODULE: pc023a_vthresh_buffer

A2

MODULE PAGE: 1 OF 1
OVERALL PAGE: 24 OF 29

TOTAL NO. OF SHEETS

SPECIFY RESISTORS TO WITHSTAND PERMANENT 5V INPUT AT VIN



IN VTHRESH<1..0>

IN VIN<1..0>

LEADING_EDGE_OUT_P<1..0> OUT

LEADING_EDGE_OUT_N<1..0> OUT

	Thu Mar 30 12:08:36 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

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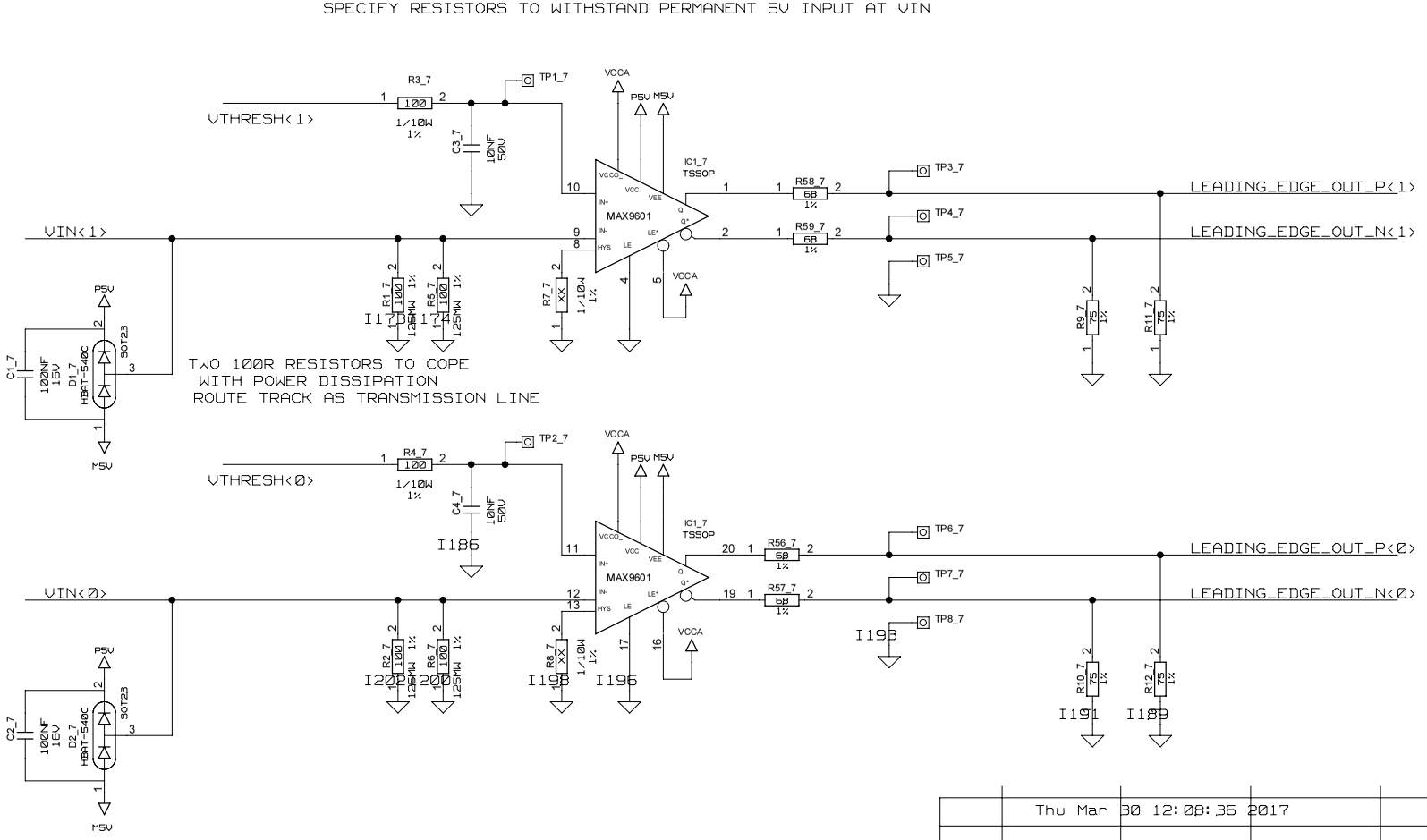
TITLE fmc_tlu_v1_lib

MODULE: fmc_tlu_threshold_discriminator_dual

A2 MODULE PAGE: 1 OF 1
OVERALL PAGE: 25 OF 29

TOTAL NO. OF SHEETS

SPECIFY RESISTORS TO WITHSTAND PERMANENT 5V INPUT AT VIN



IN VTHRESH<1..0>

IN VIN<1..0>

LEADING_EDGE_OUT_P<1..0> OUT

LEADING_EDGE_OUT_N<1..0> OUT

	Thu Mar 30 12:08:36 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON

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HIGH ENERGY PHYSICS GROUP
H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

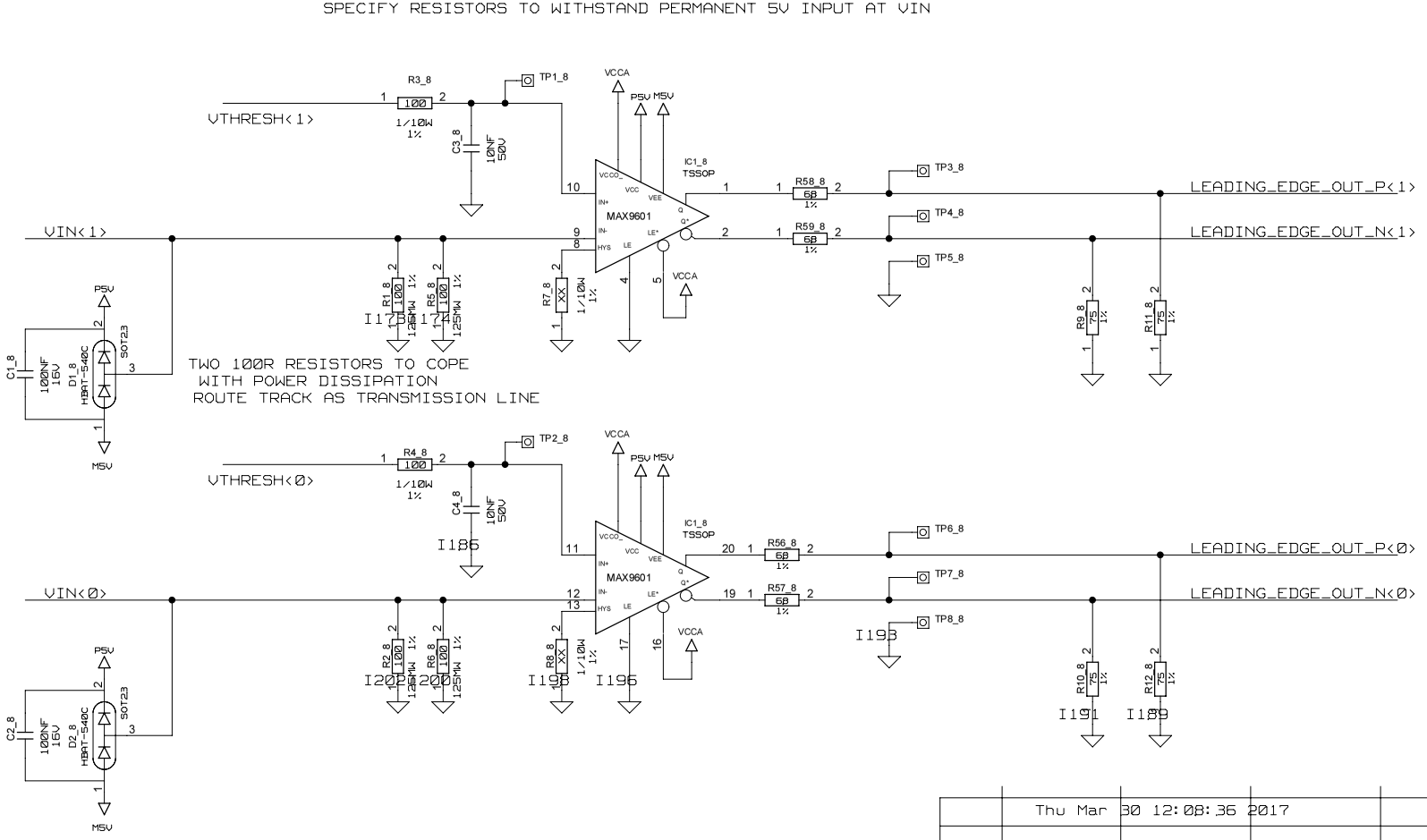
TITLE fmc_tlu_v1_lib

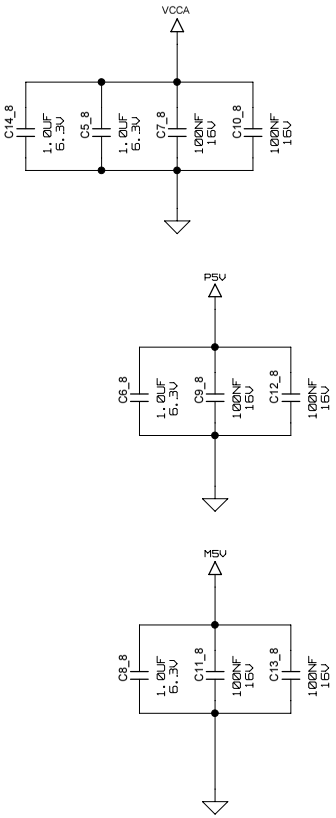
MODULE: fmc_tlu_threshold_discriminator_dual

A2 MODULE PAGE: 1 OF 1
OVERALL PAGE: 26 OF 29

TOTAL NO. OF SHEETS

SPECIFY RESISTORS TO WITHSTAND PERMANENT 5V INPUT AT VIN





VTHRESH<1..0> IN

VIN<1..0> IN

LEADING_EDGE_OUT_P<1..0> OUT

LEADING_EDGE_OUT_N<1..0> OUT

	Thu Mar 30 12:08:36 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

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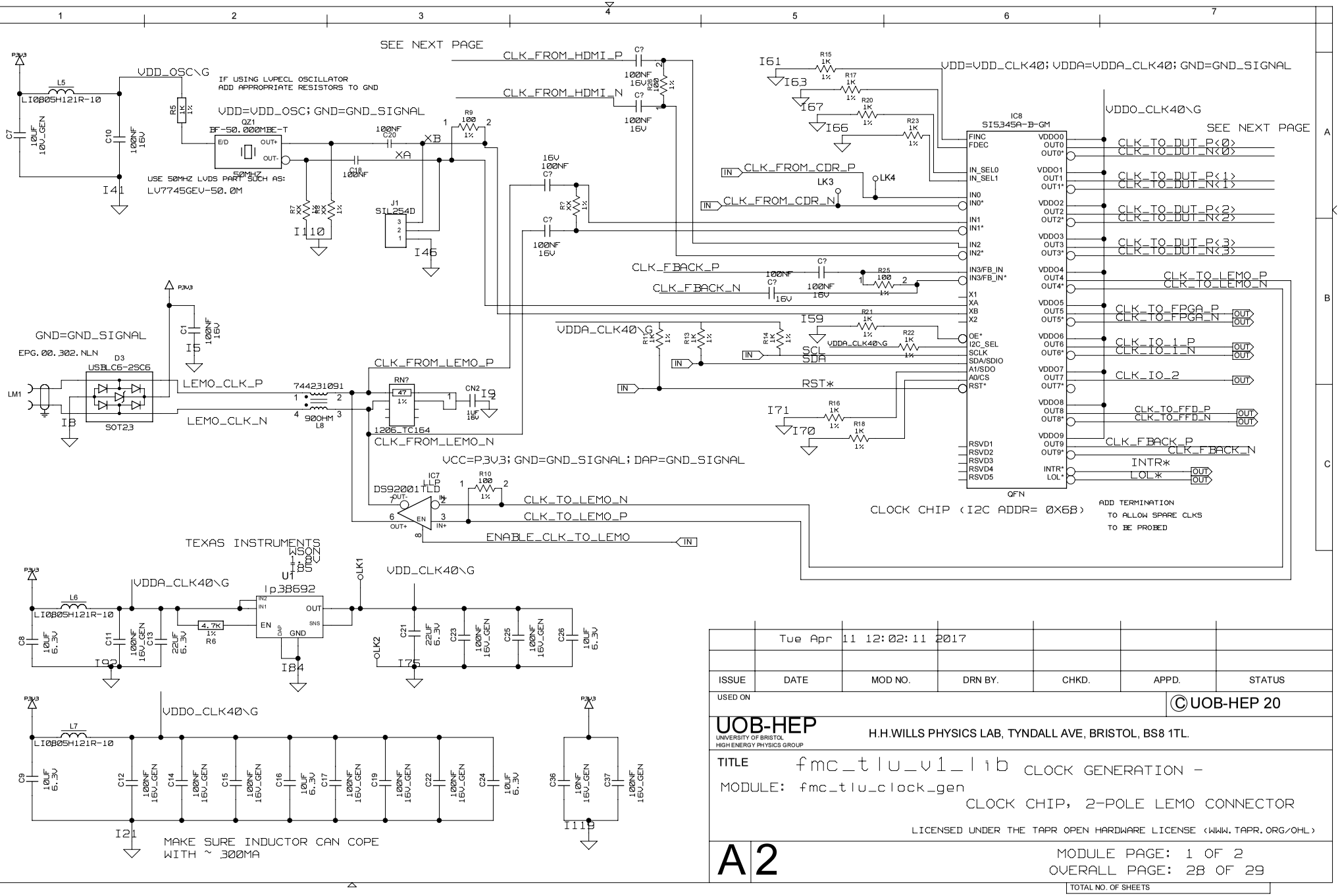
TITLE fmc_tlu_v1_lib

MODULE: fmc_tlu_threshold_discriminator_dual

A2 MODULE PAGE: 1 OF 1
OVERALL PAGE: 27 OF 29

TOTAL NO. OF SHEETS



	Tue Apr 11 12:02:11 2017					
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TITLE fmc_tlu_v1_lib CLOCK GENERATION -

MODULE: fmc_tlu_clock_gen

CLOCK CHIP, 2-POLE LEMO CONNECTOR

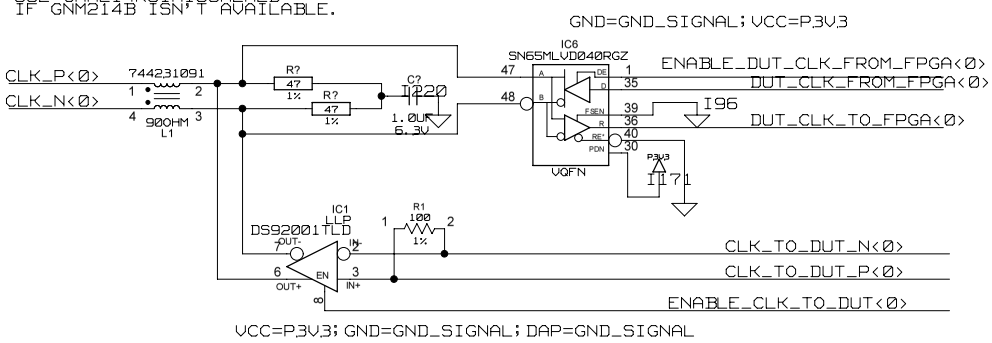
A2

MODULE PAGE: 1 OF 2

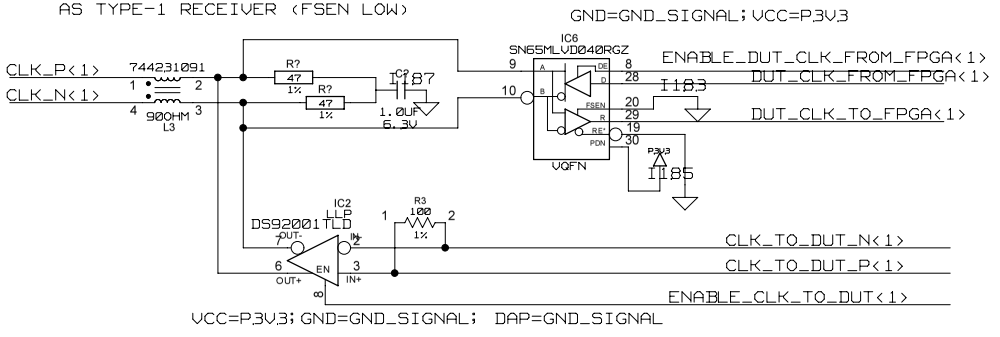
OVERALL PAGE: 28 OF 29

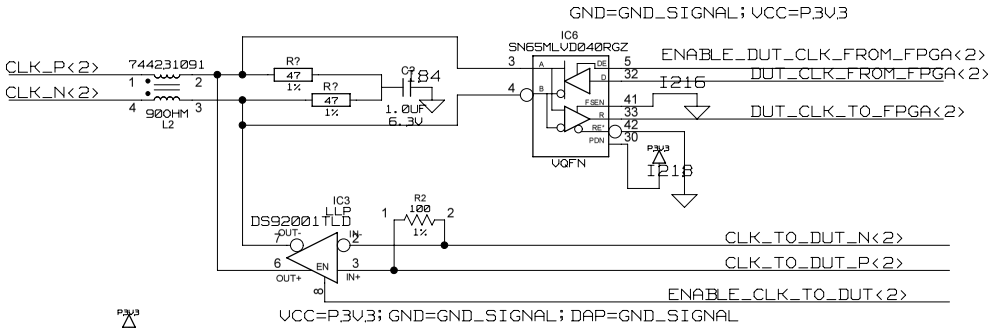
TOTAL NO. OF SHEETS

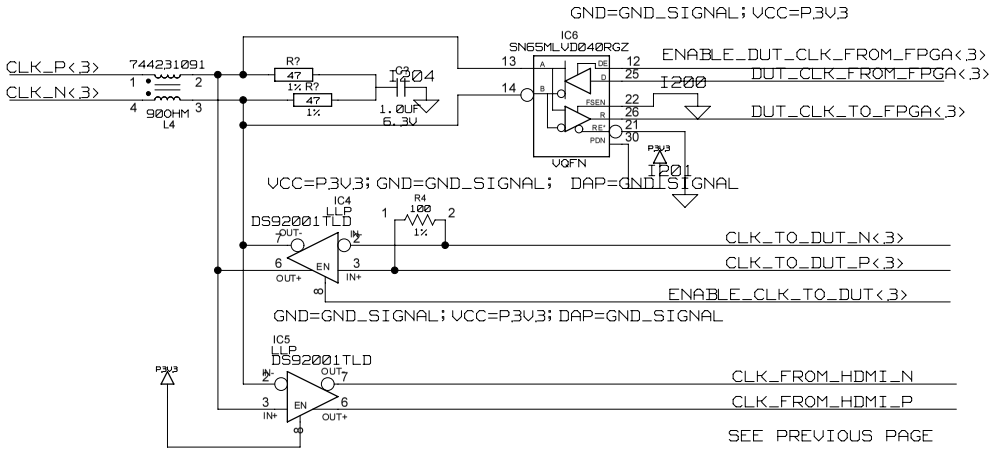
USE GNM214R61A105MEA2D
IF GNM214B ISN'T AVAILABLE.



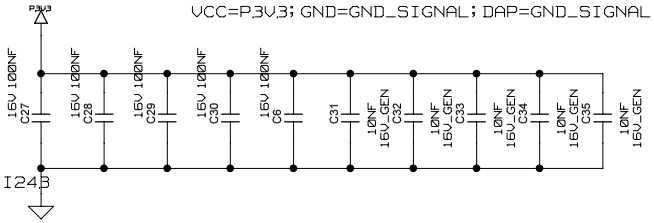
CONFIGURE SN65MLVD040
AS TYPE-1 RECEIVER (FSEN LOW)

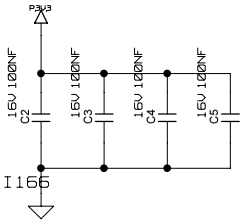






SEE PREVIOUS PAGE





CLK_P<3..0> OUT
CLK_N<3..0> OUT

ENABLE_DUT_CLK_FROM_FPGA<3..0> IN
DUT_CLK_FROM_FPGA<3..0> IN
DUT_CLK_TO_FPGA<3..0> OUT

ENABLE_CLK_TO_DUT<3..0> IN

	Fri May 05 14:48:32 2017					
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TITLE fmc_tlu_v1_lib CLOCK GENERATION -

MODULE: fmc_tlu_clock_gen

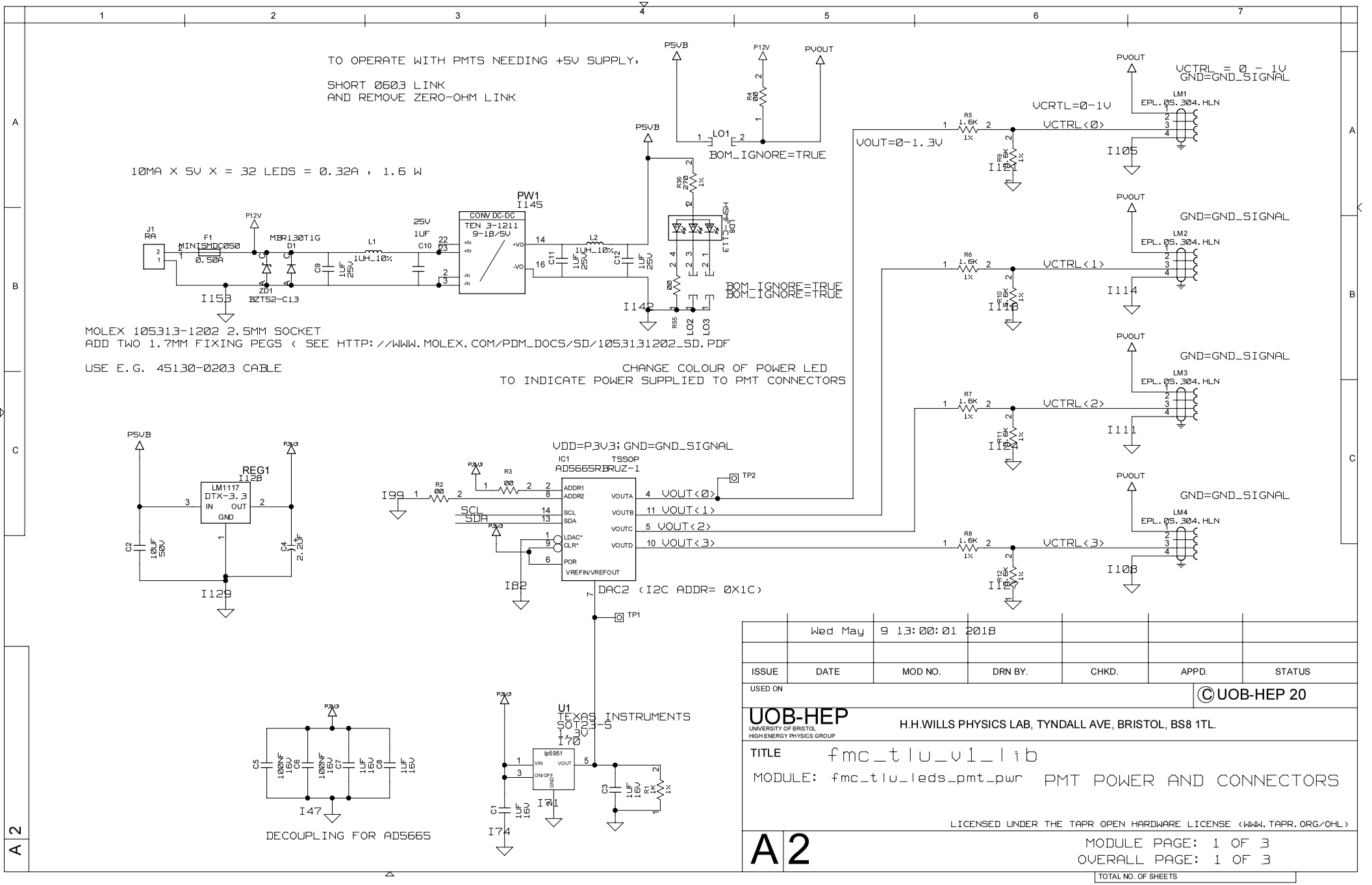
I/O BUFFERS AND LEVEL TRANSLATORS

A2

MODULE PAGE: 2 OF 2
OVERALL PAGE: 29 OF 29

TOTAL NO. OF SHEETS

12.4 Schematics for LED and PMT power module.


TO OPERATE WITH PMTS NEEDING +5V SUPPLY,
SHORT 0603 LINK
AND REMOVE ZERO-OHM LINK
10MA X 5V X = 32 LEDS = 0.32A , 1.6 W
BOM_IGNORE=TRUE
MOLEX 105313-1202 2.5MM SOCKET
ADD TWO 1.7MM FIXING PEGS (SEE HTTP://WWW.MOLEX.COM/PDM_DOCS/SD/105313120 2_SD.PDF
USE E.G. 451300203 CABLE
CHANGE COLOUR OF POWER LED
TO INDICATE POWER SUPPLIED TO PMT CONNECTORS
VDD=P3V3; GND=GND_SIGNAL
DAC2 (I2C ADDR= 0X1C)
DECOUPLING FOR AD5665
VCTRL = 0 - 1V
GND=GND_SIGNAL
VOUT=0-1.3V
VCTRL<0>
VCTRL<1>
VCTRL<2>
VCTRL<3>
VOUT<0>
VOUT<1>
VOUT<2>
VOUT<3>
PW1
I145
REG1
I128
IC1
AD5665RBRUZ-1
TSSOP
U1
TEXAS INSTRUMENTS
SOT23-5
I70
LM1
LM2
LM3
LM4
EPL.05.304.HLN
I105
I114
I111
I108
I153
I142
I99
I82
I129
I147
I174
I121
TP1
TP2
Wed May 9 13:00:01 2018
ISSUE DATE MOD NO. DRN BY. CHKD. APPD. STATUS
USED ON
©UOB-HEP 20
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HIGH ENERGY PHYSICS GROUP
H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.
TITLE fmc_tlu_v1_lib
MODULE: fmc_tlu_leds_pmt_pwr PMT POWER AND CONNECTORS
LICENSED UNDER THE TAPR OPEN HARDWARE LICENSE (WWW.TAPR.ORG/OHL)
A2
MODULE PAGE: 1 OF 3
OVERALL PAGE: 1 OF 3
TOTAL NO. OF SHEETS

LD5 IS POSITIONED
OVER CLOCK I/O

P5VB

STRANGE NUMBERING 0,1,19
DUE TO BUG IN FIRST VERSION

HSMF-C113, IF=10MA , VS = 3.3V , 5V
INGAN BLUE , VF= 3.18V, R=12 , 182
ALINGAP RED , VF = 1.8V, R=150 , 320
ALINGAP GREEN, VF = 1.95V, R=135 , 305

LED<31..0>

HSMG-C150 VF=2.2V
12V: R= 980 OHMS
5V: R= 280 OHMS

VSS=GND_SIGNAL; VDD=P3V3

IC2
PCA9539PW

SDA
SCL
I2C_RESET_N

TSSOP

EXPANDER1 (I2C ADDR= 0X77)

VSS=GND_SIGNAL; VDD=P3V3

IC3
PCA9539PW

TSSOP

EXPANDER2 (I2C ADDR= 0X76)

I215

IC5
24AA025E48T-I/SN
SOIC

SCL
SDA

100NF
16V

I208

I2C EEPROM (ADDR= 0X50)
CONTAINS PRE-PROGRAMMED
UNIQUE ID CODE

	Wed May	9 12:59:24 2018				
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TITLE fmc_tlu_v1_lib

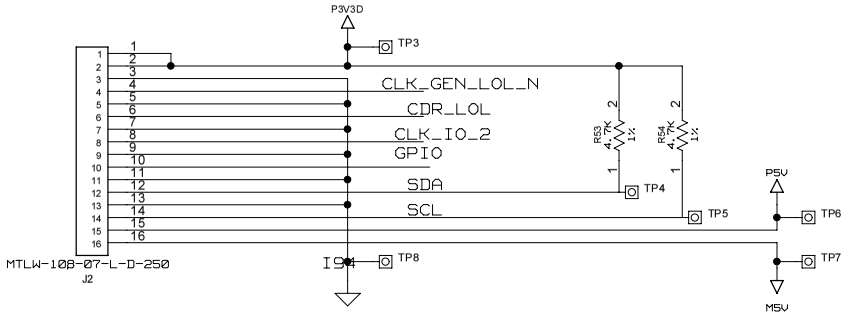
I2C I/O EXTENDERS

MODULE: fmc_tlu_leds_pmt_pwr

A2

MODULE PAGE: 2 OF 3
OVERALL PAGE: 2 OF 3

TOTAL NO. OF SHEETS



	Tue Oct 24 15:58:40 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

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TITLE fmc_tlu_v1_lib

MODULE: fmc_tlu_leds_pmt_pwr

INPUT SIGNAL CONNECTOR

A2

MODULE PAGE: 3 OF 3

OVERALL PAGE: 3 OF 3

TOTAL NO. OF SHEETS