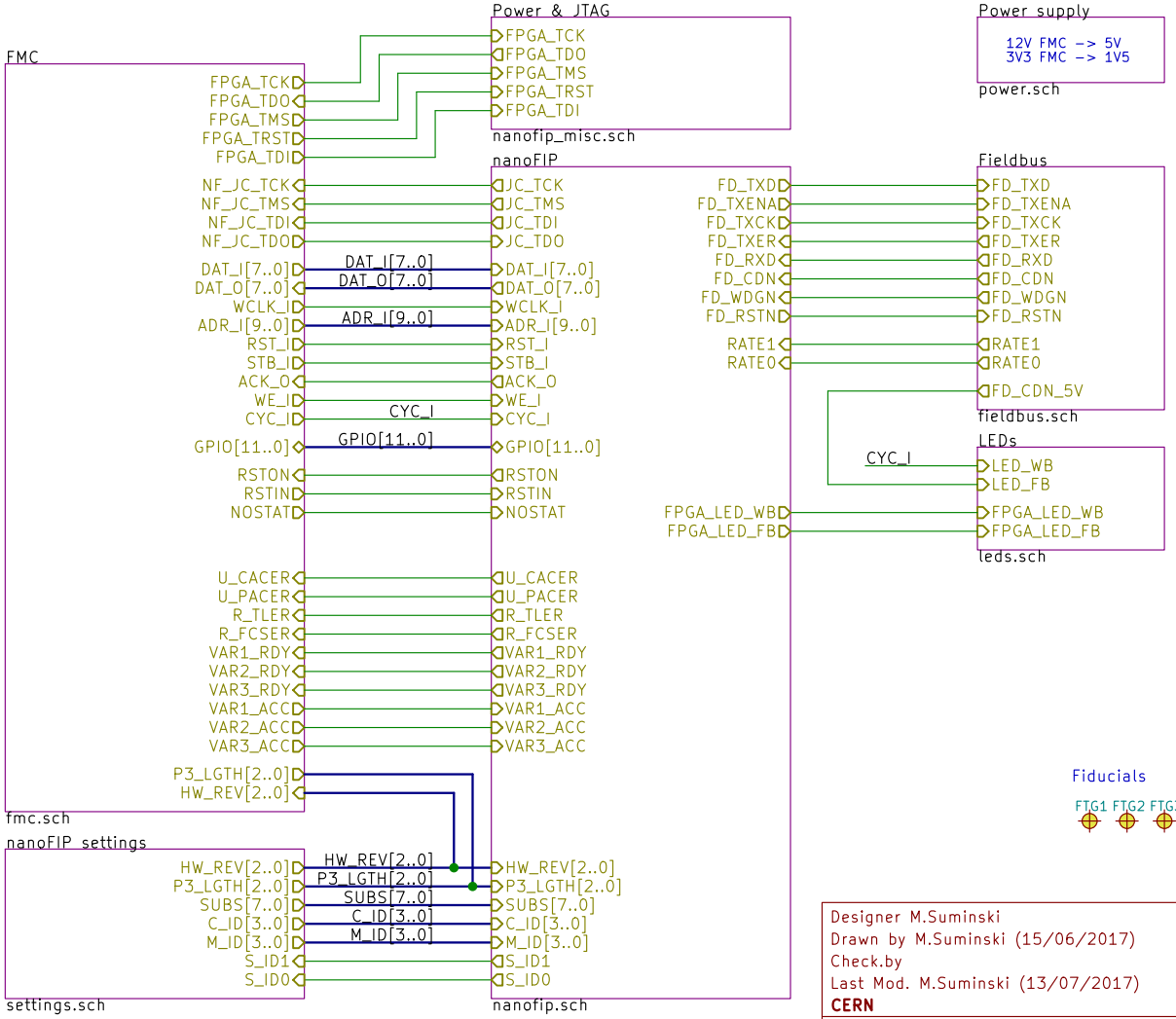
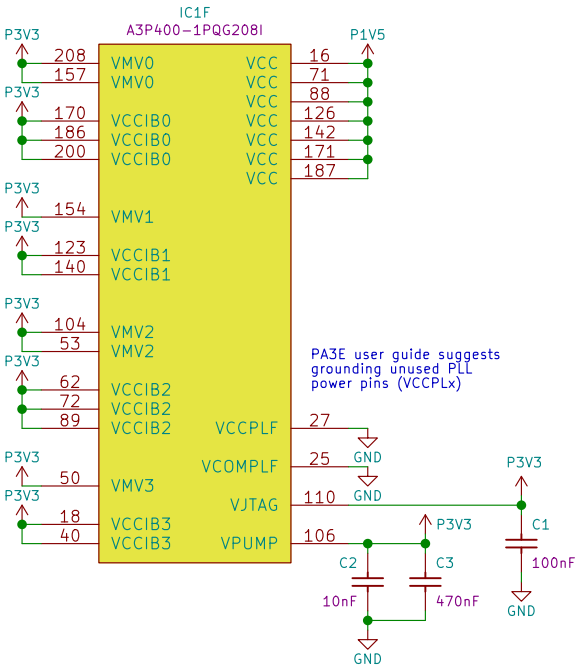
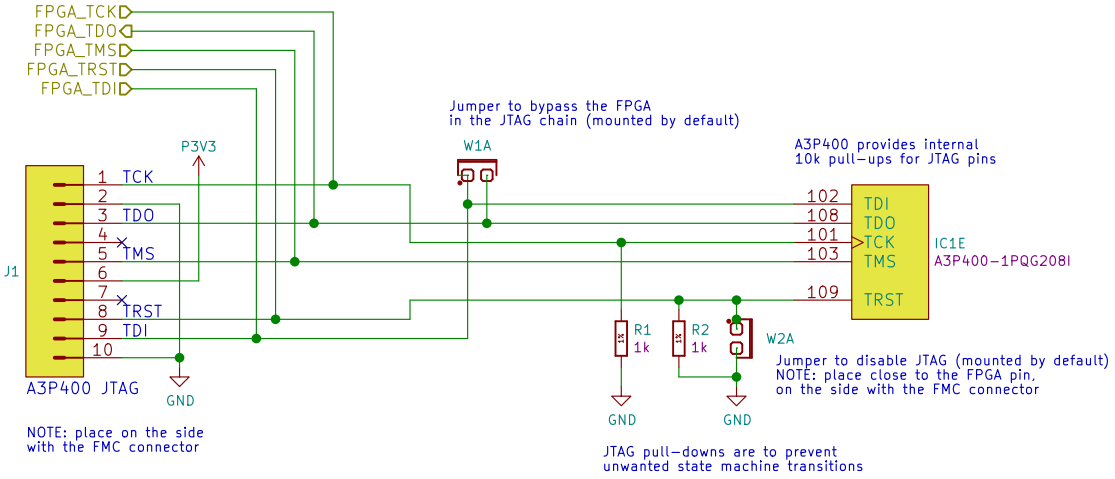
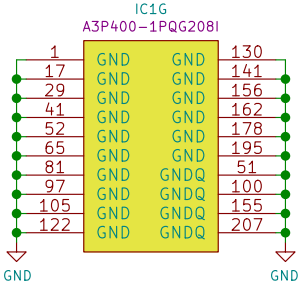
http://www.ohwr.org/projects/fmc-nanofip

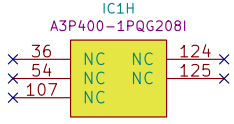


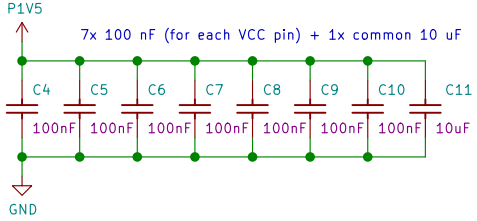
Designer M.Suminski		
Drawn by M.Suminski (15/06/2017)		
Check.by		
Last Mod. M.Suminski (13/07/2017)		
CERN		
Sheet: /		
File: fmc-nanofip.sch		
Title: FMC-nanoFIP		
Size: A4	Date: 2017-07-13	**Rev: 8**
KiCad E.D.A. kicad (2017-07-13 revision d5095252a)-master		Id: 1/8

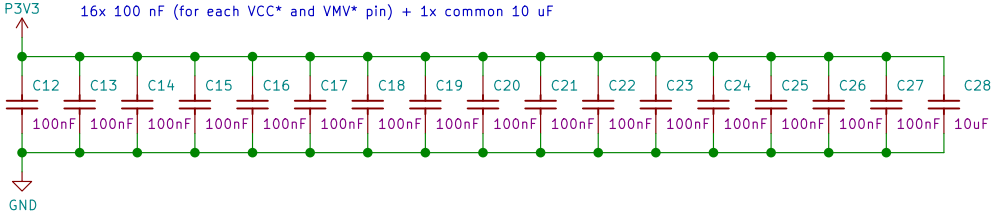






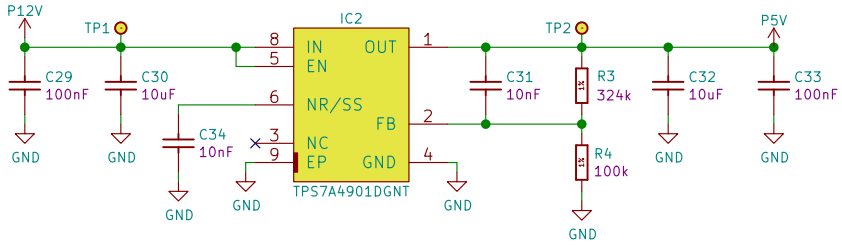






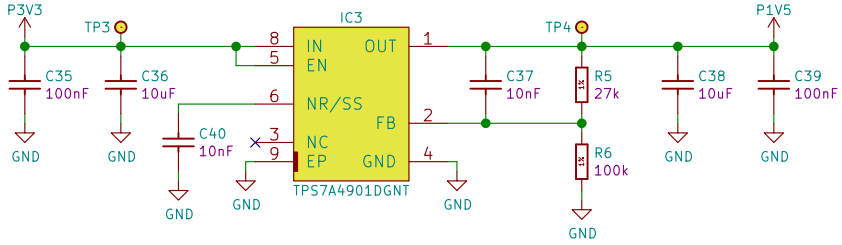
Designer M.Suminski		
Drawn by M.Suminski (15/06/2017)		
Check.by		
Last Mod. M.Suminski (13/07/2017)		
CERN		
Sheet: /Power & JTAG/		
File: nanofip_misc.sch		
Title: FMC-nanoFIP JTAG & Power		
Size: A4	Date: 2017-07-13	**Rev: 8**
KiCad E.D.A. kicad (2017-07-13 revision d5095252a)-master		Id: 2/8

Vout = (R11 / R12 + 1) * Vfb = (324k / 100k + 1) * 1.185 = 5.0244 V



place testpoints on the side without the FMC connector

Vout = (R13 / R14 + 1) * Vfb = (27k / 100k + 1) * 1.185 = 1.50495 V



Designer M.Suminski	
Drawn by M.Suminski (15/06/2017)	
Check.by	
Last Mod. M.Suminski (13/07/2017)	
CERN	
Sheet: /Power supply/	
File: power.sch	
Title: FMC–nanoFIP power supply	
Size: A4	Date: 2017–07–13 **Rev: 8**
KiCad E.D.A. kicad (2017–07–13 revision d5095252a)–master	Id: 3/8

nanoFIP bus speed

marking resistor	31.25k R7 (do not mount / 0 / No)	1M R8 (0)	2.5M R9 (do not mount / 0 / No)	5M R10 (do not mount / 0 / No)
C41	3.3uF	470nF	100nF	100nF
C47	100nF	3.3nF	1.5nF	1.5nF
C46	1nF	47pF	27pF	27pF
C44	15nF	100pF	33pF	33pF
C42, C43	47nF	not mounted	not mounted	not mounted
D6	BZV49-C8V2	BZV49-C6V2	BZV49-C6V2	BZV49-C6V2
D1, D4	BAT54S	BAV99	BAV99	BAV99
D5	BZV49-C4V7	BZV49-C3V9	BZV49-C3V9	BZV49-C3V9
R27	3R3	0R	0R	0R
R23	330R	820R	820R	820R
R30	not mounted	not mounted	27k	27k
R31	not mounted	27k	not mounted	27k
R32	27k	27k	not mounted	not mounted
R33	27k	not mounted	27k	not mounted
TR1	FIELDTR 31.25S	FIELDTR 1S	FIELDTR 2.5S	FIELDTR 2.5S

selected variant

NOTE: place a label indicating bus speed next to the marking resistors

TTL to LVTTL level conversion

IC4 SSSB231

reset until FPGA changes the output state

do not mount

NOTE: place TR1 inside the carrier board cutout area

NOTE: FIP_R_P and FIP_R_N belong to a diff pair

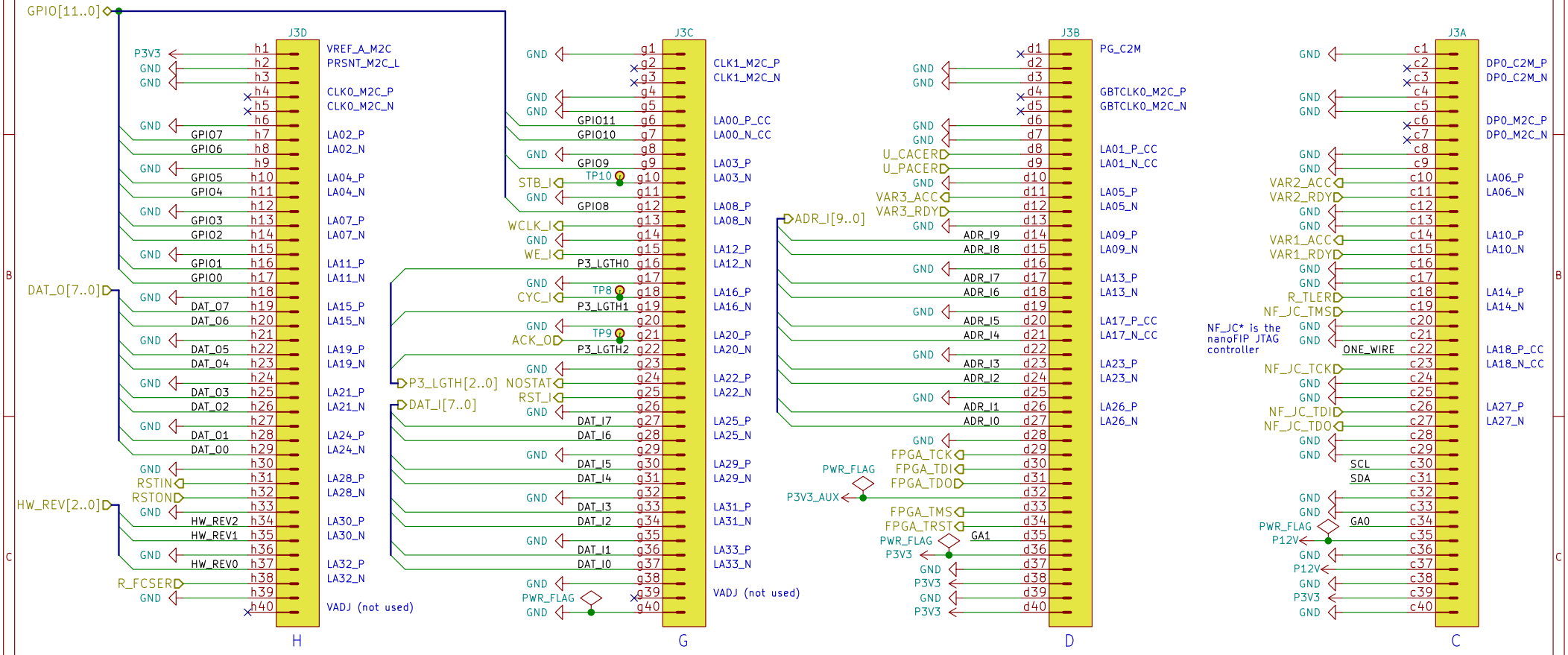
NOTE: place pin header W3 outside the carrier board cutout area

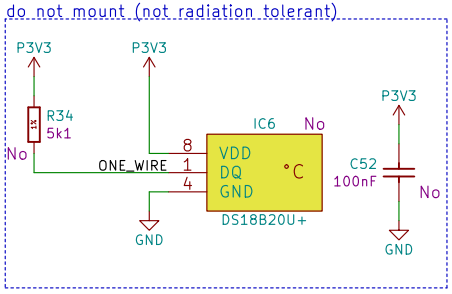
FielDrive test modes (default disabled)

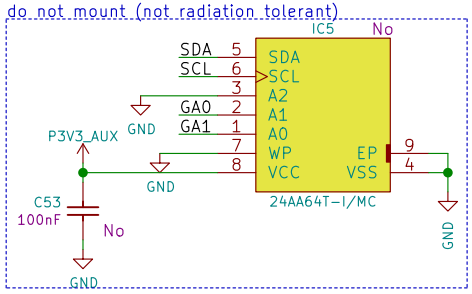
Bus speed encoding
RATE[1:0]:
00: 31.25k
01: 1M
10: 2.5M
11: 5M

Designer	M.Suminski
Drawn by	M.Suminski (15/06/2017)
Check.by	
Last Mod.	M.Suminski (13/07/2017)
	CERN
Sheet:	/Fieldbus/
File:	fieldbus.sch
Title:	***FMC-nanoFIP fieldbus interface***
Size:	A4
Date:	2017-07-13
Rev:	**8**
KiCad E.D.A.	kicad (2017-07-13 revision d5095252a)-master
Id:	4/8

NOTE: pin swapping between LA* pins possible
place test points on the side without the FMC connector

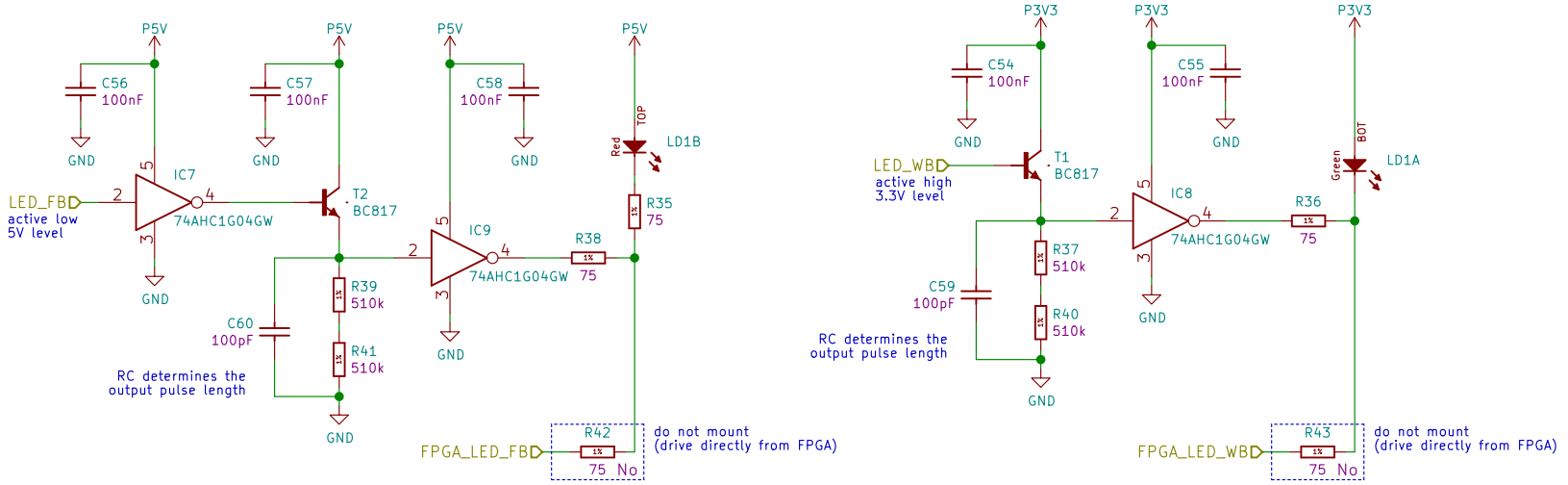




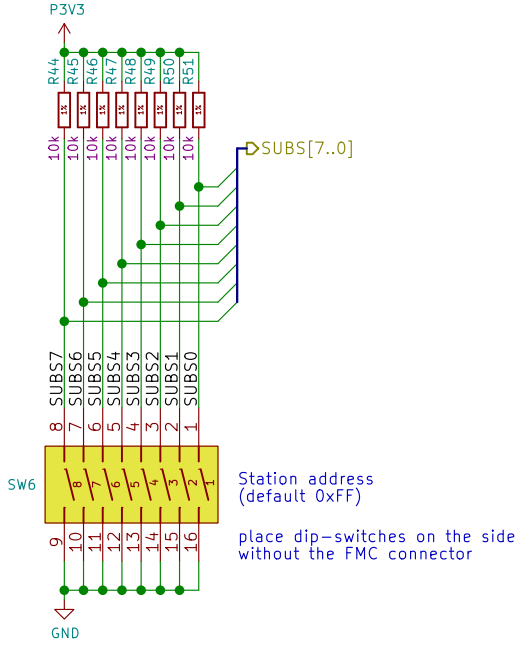


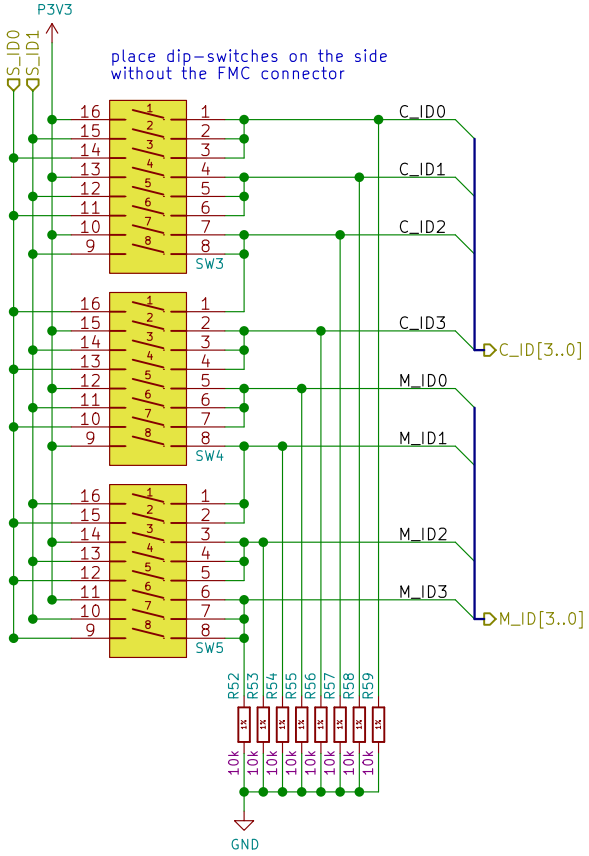
Designer	M.Suminski
Drawn by	M.Suminski (15/06/2017)
Check.by	
Last Mod.	M.Suminski (13/07/2017)
CERN	
Sheet:	/FMC/
File:	fmc.sch
Title:	**FMC–nanoFIP FMC connector (LPC)**
Size:	A4
Date:	2017–07–13
Rev:	**8**
KiCad E.D.A.	kicad (2017–07–13 revision d5095252a)–master
Id:	5/8

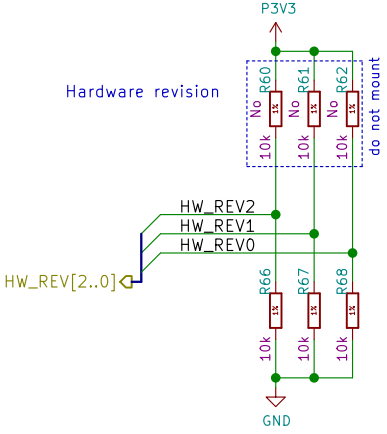
One-shot triggers to extend the LED pulse duration

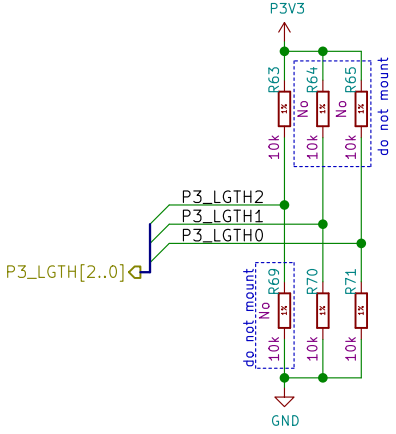


Designer	M.Suminski
Drawn by	M.Suminski (15/06/2017)
Check.by	
Last Mod.	M.Suminski (13/07/2017)
CERN	
Sheet:	/LEDs/
File:	leds.sch
Title: FMC-nanoFIP LEDs	
Size: A4	Date: 2017-07-13 — **Rev: 8**
KiCad E.D.A.	kicad (2017-07-13 revision d5095252a)-master — Id: 6/8









Produced variable data length

P3_LGTH[2:0]:
- 000: 2 bytes
- 001: 8 bytes
- 010: 16 bytes
- 011: 32 bytes
- 100: 64 bytes (default)
- 101: 124 bytes
- other: reserved

(FMC signals can override the value set with resistors)

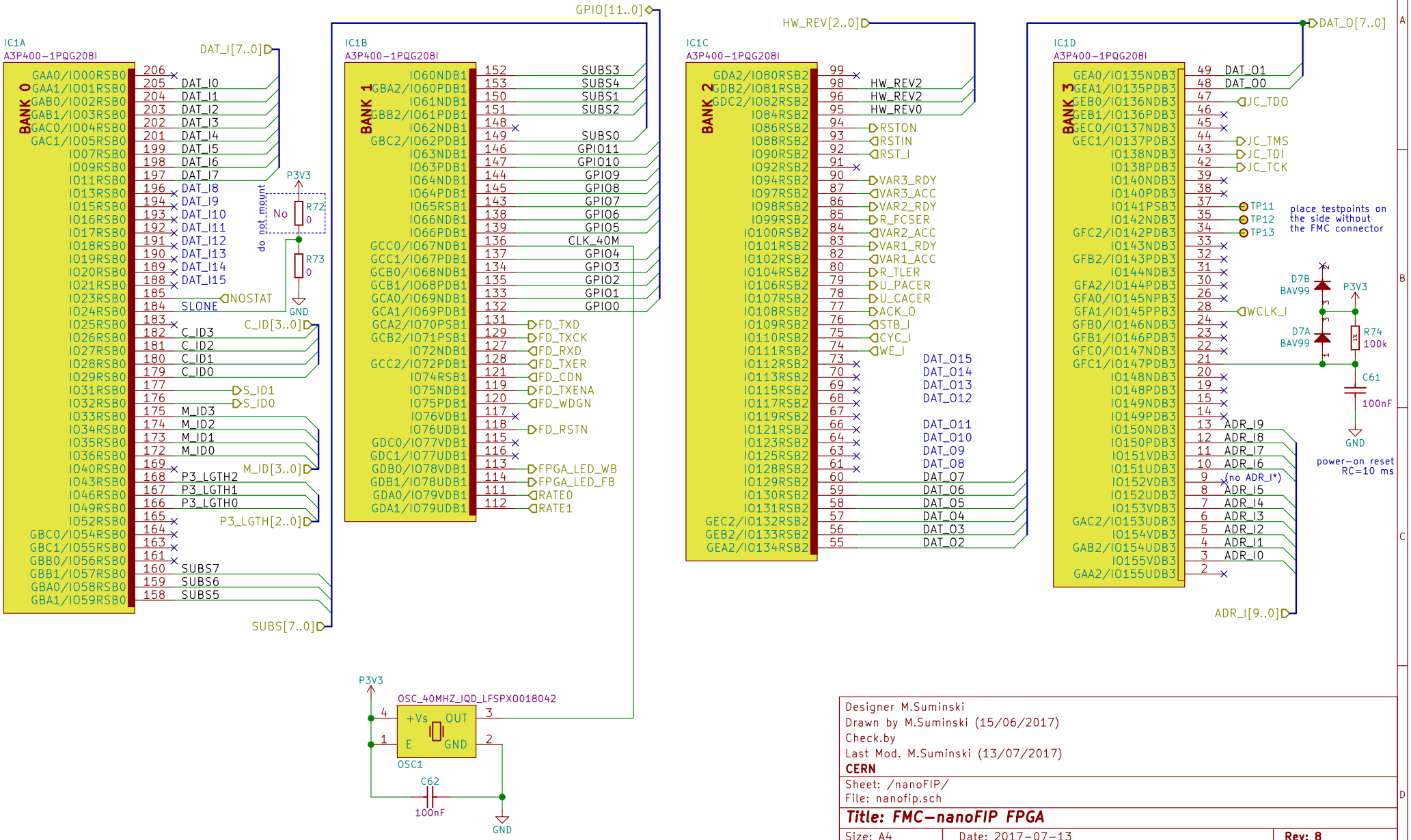
Constructor & Model ID (default 0x00)

C_ID[i]/M_ID[i] connected to: Gnd S_ID0 S_ID1 Vcc

Constructor/Model[2*i]	0	1	0	1
Constructor/Model[2*i+1]	0	0	1	1

Designer M.Suminski		
Drawn by M.Suminski (15/06/2017)		
Check.by		
Last Mod. M.Suminski (13/07/2017)		
CERN		
Sheet: /nanoFIP settings/		
File: settings.sch		
Title: FMC-nanoFIP settings		
Size: A4	Date: 2017-07-13	**Rev: 8**
KiCad E.D.A. kicad (2017-07-13 revision d5095252a)-master		Id: 7/8

NOTE: pin swapping not possible
(only GPIO pins can be moved)
nanoFIP FPGA (IC1) is preprogrammed



Designer M.Suminski		
Drawn by M.Suminski (15/06/2017)		
Check.by		
Last Mod. M.Suminski (13/07/2017)		
CERN		
Sheet: /nanoFIP/		
File: nanofip.sch		
Title: FMC-nanoFIP FPGA		
Size: A4	Date: 2017-07-13	**Rev: 8**
KiCad E.D.A. kicad (2017-07-13 revision d5095252a)-master		Id: 8/8