Object	**FMC nanoFIP PCB design review in TE-EPC-CCE**
Purpose	To check SCH and PCB of the FMC nanoFIP and the compatibility with EPC controllers.
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Date	2017-06-21 / CERN, 774-1-079
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Proposed Plan

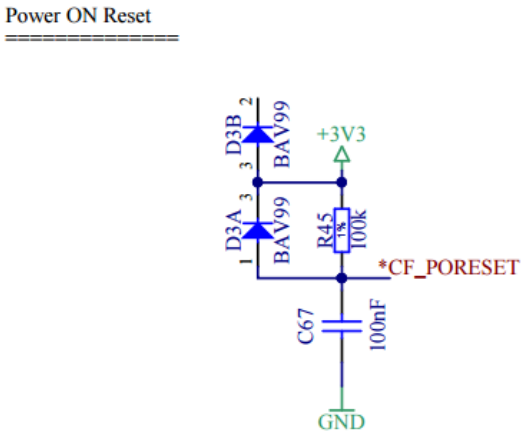
- Analyse the PCB and SCH. All data are available on OHWR [1] and [2].
- Design needs to be rad-tol up to 200Gy.

Analysis method:

Comparison of the fmc-nanofip-v6.pdf from [2] with the FGClite CB from [3].

Comments and suggestions:

- 2/7:
  - What is the clock oscillator reference? The IQD FREQUENCY PRODUCTS LF SPXO018042 clock oscillator meets the specification and can be used. Please reference to the [4]. The radiation report can be found in in the [5].
  - Power_ON rest add BAV99 for faster transient removal:



- 3/7:
  - BC807/817 gain degradation can be found in [6]. BST82 Vth degradation can be found in [7].
  - The BSS84LT1G was never irradiated. This is risky to use this reference without test campaign.

- **Suggestion 1:** delete LED_FB and LED_WB circuits and implement their functionality in the FPGA. Drive LEDs directly from the FPGA. This will make the qualification much easier.
- **Suggestion 2:** If not possible to modify the FPGA code, use the circuits with a CMOS inverter as presented on slides.
- **Comment 1:** we do not use the pull down for the TCK (R9). This resistor is defined in the Microsemi specification in [8], the FGClite implementation does not follow this recommendation.

- 4/7:
  - The TPS7A4901DRB was recommended by EN-STI and qualified. Could you please provide a reference for this?
- 6/7:
  - C46=1uF is used in the FGClite and here 10uF is proposed for 2.5MHz operation.To be verified which value is correct.
  - C52=1nF is used in the FGClite and here 1.5nF is proposed for 2.5MHz operation. To be verified which value is correct.
  - **Suggestion 3:** GND on J2 to be moved and connected to the connector.
- 7/7:
  - DS18B20 can be mounted. The component is sufficiently rad-tol: ID readings are always correct. The temperature conversion sometimes fails but after re-try works correctly. More info in [9].

Other discussion:

- Wishbone interface will be changed to serial. This requires modifications of the FPGA code so Suggestions 1 & 2 can be implemented in the FPGA.
- JTAG controller going to other cards for remote re-programmability (NF_JC_) which is used by the FGClite. A jumper should be added to short the TDI/TDO to bypass the FPGA to exclude programming of the FPGA.
- VJTAG and VPUMP higher decoupling capacitors than 100nF proposed by Eva.

References:

[1] http://www.ohwr.org/projects/fmc-nanofip/wiki
[2] http://www.ohwr.org/documents/565
[3] https://edms.cern.ch/ui/file/1605319/1/EDA-02980-V2-1_sch.pdf
[4] https://edms.cern.ch/ui/file/1605322/1/EDA-02980-V2-1_pcb-mat.pdf
[5] https://edms.cern.ch/ui/file/1503395/1/DS1616_CERN_40MHz.pdf
[6] https://edms.cern.ch/ui/file/1569689/1/CHARM_Tests_Results_1v0.pdf
[7] https://edms.cern.ch/ui/file/1583297/1/TRAD_TE_BST82_1452_CER_CS_1511_rev0.pdf
[8] https://www.microsemi.com/document-portal/doc_view/129973-lpf-ac386-an