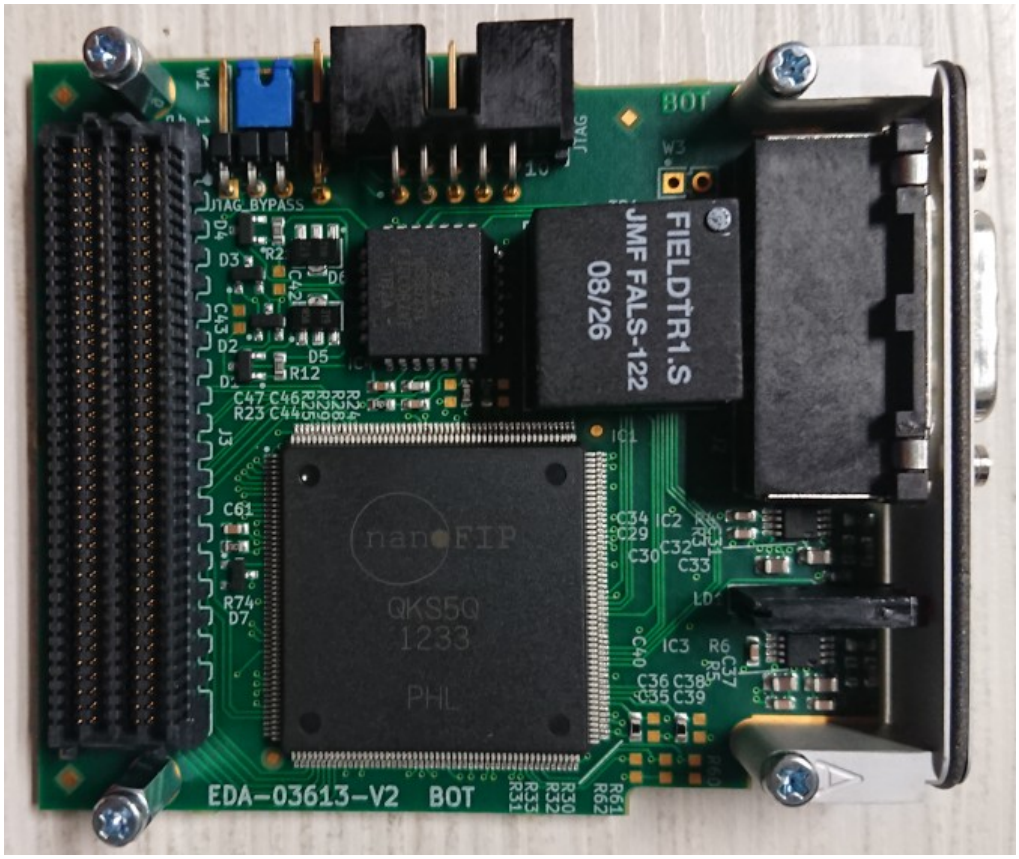
FMC-nanoFIP
User Manual



EDA-03613-V2
Interface card for the WorldFIP network in an LPC FMC form-factor

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Overview

FMC-nanoFIP mezzanine provides to an FMC carrier board a deterministic, radiation-tolerant data link compliant with the WorldFIP protocol.

The central part of the system is a Microsemi ProASIC3 flash-based FPGA, which exchanges data through a WorldFIP link and provides a memory-like interface (Wishbone bus [1]) over an FMC-LPC connector to access the data from the carrier board.

The FPGA is supported by several peripheral components: a voltage regulator producing 1.5V and a 40 MHz crystal oscillator. 3.3V power comes directly from the FMC connector. There is a number of DIP switches connected to the FPGA to program FIP related settings.

The FPGA might be reprogrammed via a standard JTAG connector available on the mezzanine or via the FMC connector using the pins specified in the FMC standard. By default the programming interface is disabled with a jumper resetting the JTAG state machine, to avoid SEE on the TAP during operation, as recommended in [2].

The WorldFIP interface is available on the front panel DB9 connector. The physical layer is implemented using a well-tested set of components, common in CERN designs: Alstom FielDrive SSSB231 transceiver and a transformer matching the link speed (FieldTR). FielDrive requires 5V power, which is delivered by a linear voltage regulator.

The front panel contains also two LEDs indicating FIP link (red) and Wishbone bus (green) activity. There are one-shot trigger circuits that are prolonging the pulses duration, as none of the FIP or Wishbone signals provide pulses lasting long enough to light a LED.

The architecture is presented on a block diagram in the Figure 1.

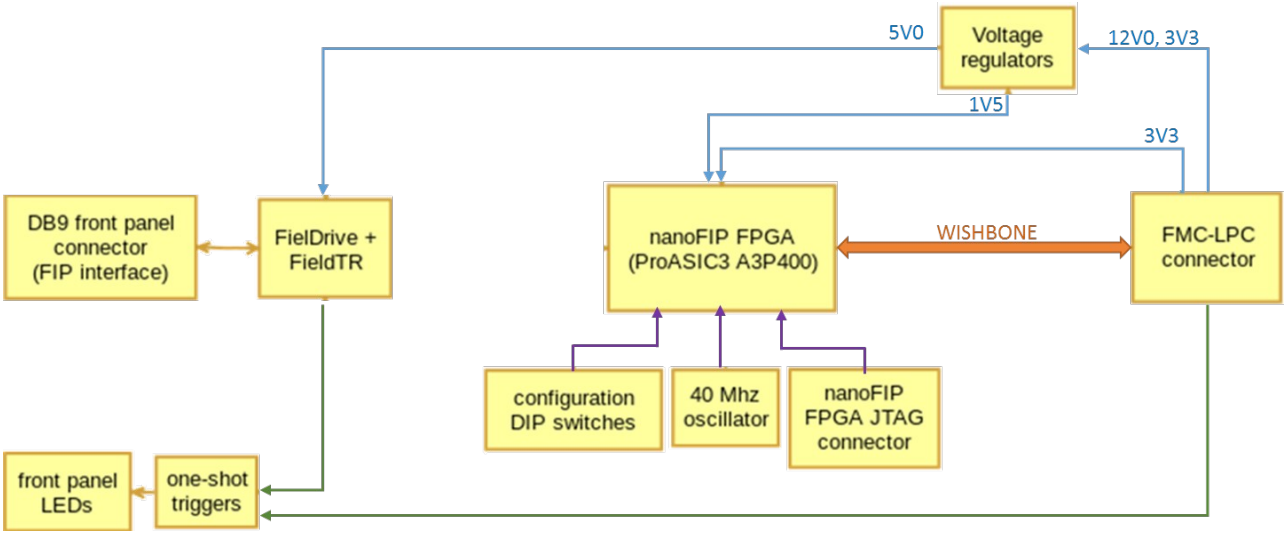

Figure 1: FMC-nanoFIP block diagram.

Variants

There are four variants of the board, each designed for a different WorldFIP link speed:

- EDA-03613-V2-0: 31.25 kbps
- EDA-03613-V2-1: 1 Mbps
- EDA-03613-V2-2: 2.5 Mbps
- EDA-03613-V2-3: 5 Mbps

Board variant might be quickly determined by checking labeled resistors on the top layer (R7-R10), as shown in the Figure 2.

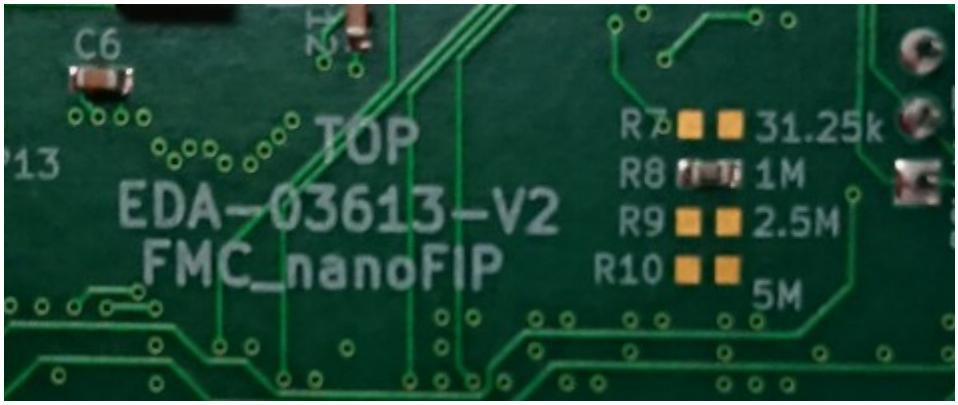

Figure 2: Resistors indicating the board variant.

Configuration

DIP switches

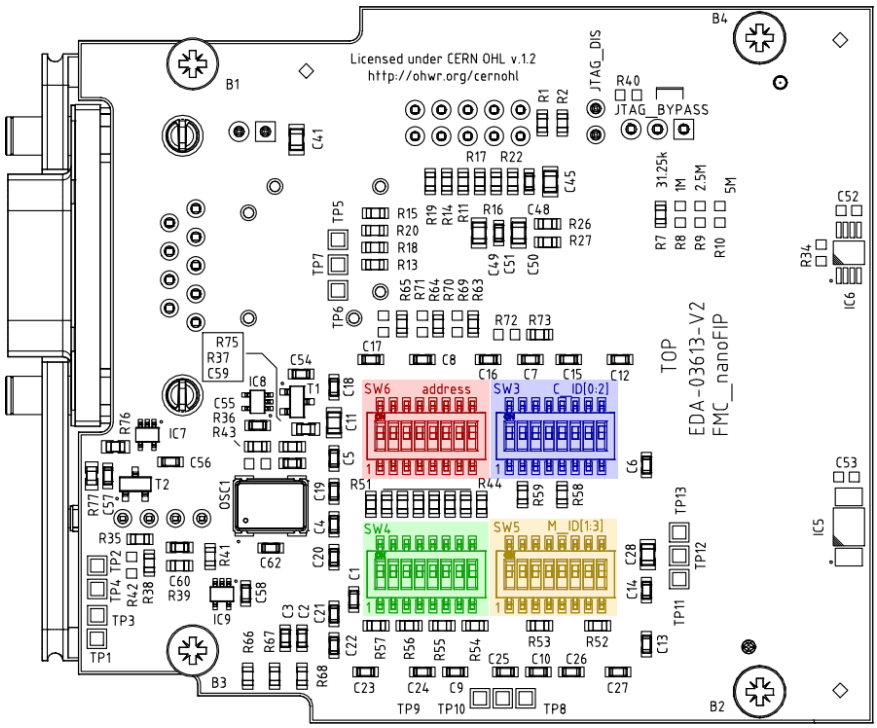

Figure 3: Configuration DIP switches.

There are four DIP switches (location shown in the Figure 3) to configure the station address, Constructor ID and Model ID of the board:

- SW6 sets the station address (default 0xFF)
- SW3 and switches 1-4 of SW4 set the Constructor ID (default 0x00)
- SW5 and switches 5-8 of SW4 set the Model ID (default 0x00)

Bits	Value	Jumper setting
C_ID[7:6]	11	SW4: 2 ON; 3,4 OFF
	10	SW4: 3 ON; 2,4 OFF
	01	SW4: 4 ON; 2,3 OFF
	00	SW4: 2,3,4 OFF
C_ID[5:4]	11	SW3: 7 ON; 8 OFF | SW4: 1 OFF
	10	SW3: 8 ON; 7 OFF | SW4: 1 OFF

	01	SW3: 7,8 OFF | SW4: 1 ON
	00	SW3: 7,8 OFF | SW4: 1 OFF
C_ID[3:2]	11	SW3: 4 ON; 5,6 OFF
	10	SW3: 5 ON; 4,6 OFF
	01	SW3: 6 ON; 4,5 OFF
	00	SW3: 4,5,6 OFF
C_ID[1:0]	11	SW3: 1 ON; 2,3 OFF
	10	SW3: 2 ON; 1,3 OFF
	01	SW3: 3 ON; 1,2 OFF
	00	SW3: 1,2,3 OFF
M_ID[7:6]	11	SW5: 6 ON; 7,8 OFF
	10	SW5: 7 ON; 6,8 OFF
	01	SW5: 8 ON; 7,8 OFF
	00	SW5: 6,7,8 OFF
M_ID[5:4]	11	SW5: 4 ON; 5,6 OFF
	10	SW5: 5 ON; 4,6 OFF
	01	SW5: 6 ON; 5,6 OFF
	00	SW5: 4,5,6 OFF
M_ID[3:2]	11	SW4: 8 ON | SW5: 1,2 OFF
	10	SW4: 8 OFF | SW5: 1 ON; 2 OFF
	01	SW4: 8 OFF | SW5: 2 ON; 1 OFF
	00	SW4: 8 OFF | SW5: 1,2 OFF
M_ID[1:0]	11	SW5: 5 ON; 6,7 OFF
	10	SW5: 6 ON; 5,7 OFF
	01	SW5: 7 ON; 6,7 OFF
	00	SW5: 5,6,7 OFF

Jumpers

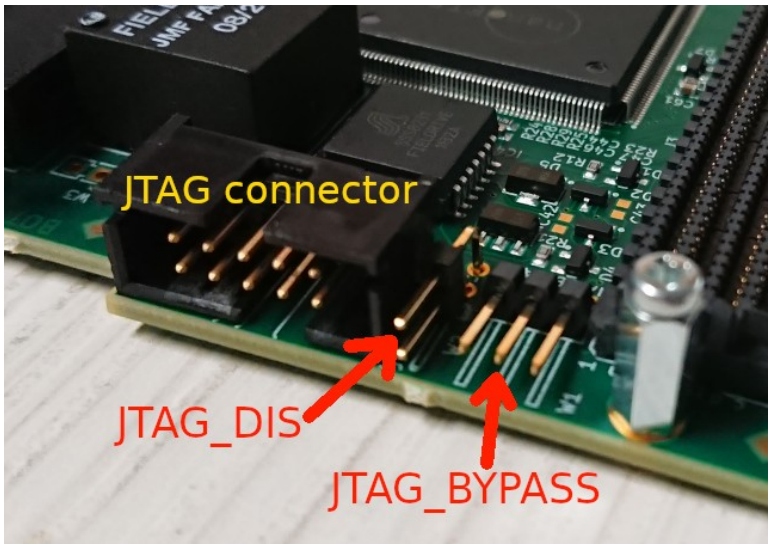

Figure 4: JTAG related jumpers.

There are two jumpers to configure the nanoFIP JTAG chain (next to the JTAG connector, see the exact localization on the Figure 4):

- JTAG_BYPASS: shorted pins 1-2 exclude the nanoFIP FPGA from the FMC JTAG chain, shorted pins 2-3 include the nanoFIP in the chain (jumper is mounted on pins 1-2 by default).
- JTAG_DIS: when mounted the nanoFIP JTAG is disabled by shorting TRST pin to the ground (jumper mounted by default).

NOTE: nanoFIP TRST signal is separated from the FMC JTAG chain as R40 is not mounted (see [4], p.2). This is done due to a strong pull-down resistor (R2), which prevents many JTAG adapters from correct operation. It is recommended to use the dedicated JTAG (J1) connector instead of using the FMC JTAG chain for reprogramming the nanoFIP FPGA if needed.

FMC pins

Two settings are available via the FMC connector pins:

- NOSTAT - disables sending of nanoFIP status together with the produced data when high (pin g24).
- P3_LGTH[2:0] - produced variable data length (default setting: 100 → 64 bytes; pins g16, g19, g22).

Refer to the nanoFIP Functional Specification [3] for more details.

Front panel

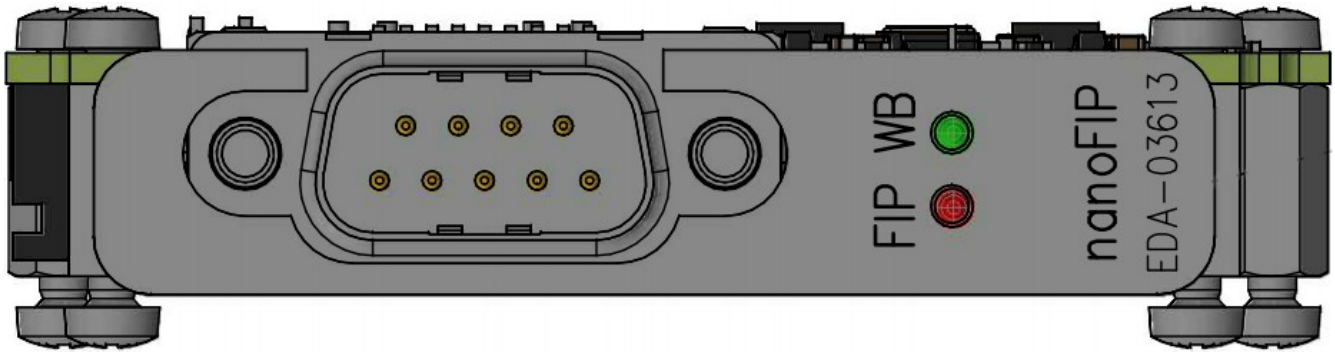

Figure 5: FMC-nanoFIP front panel.

The front panel presented in the Figure 5 provides a regular size DB9 connector to connect the mezzanine to a WorldFIP network.

There are two LEDs:

- *FIP* (red) indicates activity on the WorldFIP link
- *WB* (green) indicates activity on the Wishbone bus

Interface

WorldFIP link is available either via the front panel DB9 connector or W3 pin header on the board (the latter is normally not mounted).

Wishbone bus available on the FMC connector is used for communication with the carrier board.

Check the schematics ([4], p. 5) to see the FMC connector pinout.

JTAG chains

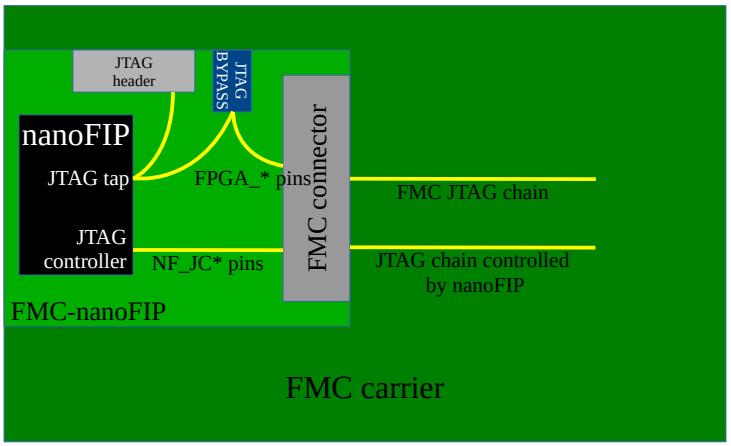

Figure 6: JTAG chains.

Figure 6 pictures two JTAG chains which cannot be interlinked.

- The first chain (FPGA_* pins [4], p. 5) is connected to the pins specified by the FMC standard. FMC-nanoFIP might be a part of this chain or bypassed, depending on the JTAG_BYPASS jumper setting and presence of R40 resistor. If R40 is not mounted, the FPGA might still be programmed using a dedicated JTAG connector (J1) compatible with FlashPro cable.

  NOTE: if FMC-nanoFIP is configured to be a part of the FMC chain and R40 is mounted then JTAG_DIS jumper must be removed, otherwise the whole chain is blocked. Even with the jumper removed, there is a strong pull-down resistor (R2) which may prevent a JTAG controller from correct operation. Please verify that your JTAG controller is able to drive TRST pin out of the low state.

- In the second chain (NF_JC_* pins [4], p. 5), nanoFIP is the JTAG controller. This is a way to reprogram other components on the carrier board using a WorldFIP link. See more details in a document describing usage of the nanoFIP JTAG controller [5].

All possible JTAG programming settings are presented in Table 1.

	Programming disabled	**Programming via JTAG header (J1)**	**Programming via FMC connector**
JTAG_DIS jumper	mounted	not mounted	not mounted
JTAG_BYPASS jumper	mounted on pins 1-2	mounted on pins 2-3	mounted on pins 2-3
R40 resistor	not mounted	does not matter	mounted

Table 1: JTAG programming settings.

References

1. Wishbone bus: https://opencores.org/howto/wishbone

2. TRST* and the IEEE JTAG 1149.1 Interface:
https://edms.cern.ch/ui/file/1097271/1.2/JTAG_bus_precautions.pdf

3. nanoFIP Functional Specification: https://edms.cern.ch/document/1107940

4. FMC-nanoFIP schematics (V1/1 Mbps variant): https://edms.cern.ch/document/1973300/1

5. WP10 Implementation of a JTAG Master Controller for the reprogramming of the "User-FPGA"
https://www.ohwr.org/projects/nanofip/wiki/wp10