The second PCB layout of the TDC has been reviewed on 20 April 2011.

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Review comments

1) Size of the vias could be smaller, specially near IC6, which makes cuts on the ground plane. Reduce them if needed.
2) Displace C50 down, on the other side of J6. This will allow a better decoupling of the +12V.
3) add a small 100nF in parallel (near) of C3 to make a proper decoupling of the +12V.
4) Remove L4 (this implies removing the P3V3_TDC plane) and enlarge (or push) the P3V3 under J6 up to the edge of the PCB.
5) Remove the texts on the power planes. This is useless and cuts the plane.
6) On IC4, properly connect thermal plane using vias directly on the thermal plane (plugged in holes).
7) Is it necessary to fill the holes on the thermal pads? (plugged in holes). A further discussion is necessary with TE/MPE.
8) Remove R21 and R22, as only one oscillator will be mounted at a time. And connect directly OSC1 pin 4 and OSC2 pin 3. The oscillator output can then be routed more directly to IC6.
9) Add 100nF capacitors under the J6 connectors (bottom side) on the power inputs (four caps on P3V3, and two on the P12V, one for each input).
10) Move C35 and C36 on the TOP layer, as they are too high.
11) Verify the silkscreen size (4 mils).