PCB Layout review 1 | 08.04.2011

The first PCB layout of the TDC has been reviewed on 8 April 2011.

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Review comments

1) remove TP1 to TP3. -> OK
2) NET VDDC is unknown, should merge it with VDDC_TDC. No: is a separate supply to TDC! (CA) -> OK
3) avoid long lines to decoupling caps. -> OK
4) add more vias on TDC chip grounds (1 via/ground pin). -> OK
5) Reduce size of +5V plane (not needed around connector J6) -> OK
6) Move C46 to C50 near the TDC chip. -> OK
7) check the height of tantalum decoupling capacitors on bottom side. 2.9mm, including the PCB thickness is the maximum height. See http://cdsweb.cern.ch/record/1172409/files/ANSI-VITA-57-1-Rev2010.pdf page 24 C13 is 1.8mm, Temp IC is 1.75mm. PCB thickness is 1.6mm. This makes 1.6+1.8=3.4mm. This is out of spec by 0.5mm. -> OK, but still move C35 and C36 on TOP layer.
8) move down +5V supply near IC8 / IC9. -> OK
9) On IC6, avoid traces between pads and thermal plane (can be problematic when soldering). -> OK
10) If necessary, add 2 more planes. -> was not necessary, OK
11) Add OHWR text on PCB: "Licensed under CERN OHL v.1.0" -> OK
11a) Add "http://ohwr.org/projects/fmc-tdc" -> OK
12) Replace SMC footprints by LEMO. Finally decided to not add the choice to replace LEMOs by SMCs. -> OK
13) Check that the vias under IC6 on thermal pad are not filled... (shown as "plugged in holes"). -> Need further discussion...
14) Add LHC name (to be confirmed by Erik). Do not put it, there will be a sticker with LHC name on the PCB. EB/MC -> OK
15) Verify that high speed signals do not cross different power planes, as for TDC data and control signals (crossing between P3V3_TDC and P5V0). -> OK
16) Properly route DC/DC converter (IC3, L1, D2) with a topside ground area as specified in the TPS5420 datasheet. -> OK
17) Reduce size of the trace between oscillator (OSC1 or OSC2) and the PLL (IC6). Maybe swap IC5 and OSC1/OSC2. -> OK
18) Design the front-panel. -> TBD
19) Add capacitors around FMC connector for filtering supply and better paths for return currents. -> OK, some 100nF/50V still needed near PS inputs on the bottom side. Move C50 on the other side of J6.