The document describes different tests on the TDC mezzanine board that aim at assessing its performance. You could also consult the TDC precision documentation.

**Test Setup 1 | Cable Length**

We use the PCIE_FMC_TESTBENCH5 front end in the 864-1-A17 lab where we plug two SPEC carrier boards as Figure 1 indicates.

SPEC 1 carries a Fine Delay mezzanine, used as pulse generator. SPEC 2 carries the TDC mezzanine under test. The CLOCK FAN_OUT board is also used. Figure 2 shows how pulses should be arriving to each one of the TDC channels.

A dedicated python testing program is responsible for the continuous retrieval of the timestamps and their manipulation: only timestamps corresponding to rising edges are kept and they are subtracted by pairs. This way the delay introduced by the coaxial cable is the constant value on which the precision testing is based.

![Test setup 1](image1)

*Figure 1: Test setup 1*

![Pulses arriving to the TDC input channels](image2)

*Figure 2: Pulses arriving to the TDC input channels 2 and 4*
The board #007 was tested at two different moments. 10 M measurements were acquired per test. Figures 3 and 4 show the 10 M data for the two tests.

Note in Figure 3 the 14 spikes and in Figure 4 the 9 spikes at around mean-value ±4 ns. This 4 ns offset comes from the ACAM fine time; we believe it is caused by a bug in the ACAM chip. The error rate is around 1 wrong timestamp per 2 M. We have remarked that this issue could be related with the Fine Delay issue on the ACAM R-mode, where wrong measurements of around ±1.5 ns were reported every few millions. The resolution in R-mode is 3 times higher than in I-mode and the errors seen in I-mode (4ns) are 3 times the ones in in R-mode (1.5*3 = 4ns). We are in contact with ACAM for the clarification of the issue.

Table 1 summarizes the measurements main statistics.

<table>
<thead>
<tr>
<th>Board</th>
<th>Data Volume</th>
<th>Mean (ps)</th>
<th>Sigma (ps)</th>
<th>Min (ps)</th>
<th>Max (ps)</th>
<th>Max Min (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>#007</td>
<td>10M</td>
<td>10407</td>
<td>83</td>
<td>6080</td>
<td>15040</td>
<td>8960</td>
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<td>10M</td>
<td>10407</td>
<td>84</td>
<td>6080</td>
<td>14976</td>
<td>8896</td>
</tr>
</tbody>
</table>

Table 1: Summary from measurements of Figures 3 and 4
Figure 5 shows the histogram of the measurements from Figure 3. The darker line represents the histogram using 25 bins and the lighter line using 8960 bins.

Figure 5: Histograms from measurements of Figures 3

Figure 6 zooms into Figure 5 to show clearly the 14 spikes at the extremes of the graph.

Figure 6: Zoom into Figure 5

Figure 7 shows together the histograms of the measurements from Figure 3 and Figure 4.

Figure 7: Histograms from measurements of Figures 3 and 4
Removing the ±4 ns spikes through data processing, gives the following clean measurements.

![Graph showing test setup 1 measurements without ±4 ns spikes](image1)

**Figure 8: Test Setup 1 Test#1 measurements without ±4 ns spikes**

![Graph showing test setup 2 measurements without ±4 ns spikes](image2)

**Figure 9: Test Setup 1 Test#2 measurements without ±4 ns spikes**

Table 2 summarizes the main statistics without the ±4 ns spikes.

<table>
<thead>
<tr>
<th>Board</th>
<th>Data Volume</th>
<th>Mean (ps)</th>
<th>Sigma (ps)</th>
<th>Min (ps)</th>
<th>Max (ps)</th>
<th>Max Min (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>#007</td>
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<td>10407</td>
<td>83</td>
<td>9960</td>
<td>11168</td>
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</tr>
<tr>
<td>#007</td>
<td>10M</td>
<td>10407</td>
<td>84</td>
<td>9984</td>
<td>11264</td>
<td>1280</td>
</tr>
</tbody>
</table>

**Table 2: Summary from measurements of Figures 6 and 7**

Regarding the accuracy of the measurements, note that instead of 10'000 ps, which is the difference in cable length, we are measuring 10'407 ps; this comes from the part-to-part skew of the channels input buffers and the different path delays on the board. Some part could also be coming from the CLOCK FAN_OUT board. The calibration procedure will eliminate this offset.
Test Setup 2 | Cesium 1 PPS

We use the PCIE_FMC_TESTBENCH7 front end in the 864-1-A19 lab where we plug one SPEC carrier board. As pulse generator we use the 1 PPS output of the Cesium Clock. Figure 10 shows the setup and Figure 11 shows the pulses arriving to the TDC input channel.

A dedicated python testing program is responsible for the continuous retrieval of the timestamps and their manipulation: only timestamps corresponding to rising edges are kept and they are subtracted by pairs. This way we are expecting constantly measurements of 1 second.

Figure 10: Test Setup 2

Figure 11: Pulses arriving to the TDC input channel 1
Figure 12 shows in blue the 400 K measurements that were acquired during ~10 days. In green are the temperature measurements from the One-Wire temperature sensor on the TDC board.

Note that the timebase accuracy of the TDC application is by specification ±4 ppm; for a measurement of 1 s this translates to a margin of ±4’000’000 ps. From Table 3, the span of our measurement results was limited to < 200’000 ps. In Figure 12 in pink we have highlighted the drift per degree.

Figure 12: Test Setup 2 timestamp measurements (in blue) and temperature measurements (in green). There is around 13’000 ps drift per °C.

Figure 13: Histogram from timestamp measurements of Figure 12
Table 3 summarizes the measurements main statistics.

<table>
<thead>
<tr>
<th>Board</th>
<th>Data Volume</th>
<th>Mean (ps)</th>
<th>Sigma (ps)</th>
<th>Min (ps)</th>
<th>Max (ps)</th>
<th>Max-Min (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>#004</td>
<td>400K</td>
<td>9999999914857</td>
<td>13789</td>
<td>999999773063</td>
<td>999999962880</td>
<td>189816</td>
</tr>
</tbody>
</table>

Table 3: Summary from timestamp measurements of Figure 11

Note that in these measurements because of the ±4ppm span, the eventual ±4ns spikes cannot be distinguished.

We continued on this setup by reconfiguring the DAC of the TDC mezzanine. The DAC controls the VCXO where the TDC timebase accuracy is based on. We changed the DAC value from 1V65 (DAC word 0xA8F5) to 1V66 (DAC word 0xAA00) and that shifted the measurements mean value. Figure 14 shows both data spanning over around 6 hours at a relatively stable temperature. Note though that since the tests took place at different moments, the temperature stability is not the same for the two versions.

Figure 14: Test Setup 2 measurements with different DAC values

Figure 15: Histogram from measurements of Figure 14

Table 4: Summary from measurements of Figure 14

<table>
<thead>
<tr>
<th>Board</th>
<th>Data Volume</th>
<th>Mean (ps)</th>
<th>Sigma (ps)</th>
<th>Min (ps)</th>
<th>Max (ps)</th>
<th>Max-Min (ps)</th>
</tr>
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<tbody>
<tr>
<td>#004 DAC 1.66V</td>
<td>11K</td>
<td>999999994843</td>
<td>3339</td>
<td>999999976501</td>
<td>1000000008588</td>
<td>32087</td>
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<tr>
<td>#004 DAC 1.65V</td>
<td>11K</td>
<td>999999918992</td>
<td>2890</td>
<td>999999908160</td>
<td>999999929856</td>
<td>21696</td>
</tr>
</tbody>
</table>

Table 4: Summary from measurements of Figure 14

Regarding the accuracy of the measurements, the calibration procedure will set the DAC to its optimal value.
Test Setup 3 | Pendulum

We use the PCIE_FMC_TESTBENCH7 front end in the 864-1-A19 lab where we plug one SPEC carrier board. As pulse generator we use the output of the CNT 91R Pendulum configured at 1ms period. Figure 16 shows the setup and Figure 17 shows the pulses arriving to the TDC input channel.

A dedicated python testing program is responsible for the continuous retrieval of the timestamps and their manipulation: only timestamps corresponding to rising edges are kept and they are subtracted by pairs. This way we are expecting constantly measurements of 1 ms. The

Figure 16: Test Setup 3

Figure 17: Pulses arriving to the TDC input channel 1. Not here that in comparison with the previous tests we get 128 measurements of 1ms per 128 rising timestamps. In the previous test with the cesium clock the subtraction was done different and we were getting 64 measurements per 128 rising timestamps.
The board #004 was tested at three different moments. 10 M measurements were acquired per test. In Figure 18 we have put together in different colors the 10 M data for the three test sets.

Note in Figure 18 the spike at around mean-value ±4 ns on one set of measurements. The spike in this case appears both at +4ns and -4ns, one after the other; note however that both spikes have occurred from the same one wrong timestamp; this is because as Figure 17 describes, in this setup we are subtracting every timestamp from its previous, and not timestamps as different pairs.

![Figure 18: Test Setup 3, 3 sets of measurements](image)

<table>
<thead>
<tr>
<th>Board</th>
<th>Data Volume</th>
<th>Mean (ps)</th>
<th>Sigma (ps)</th>
<th>Min (ps)</th>
<th>Max (ps)</th>
<th>Max-Min (ps)</th>
</tr>
</thead>
<tbody>
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<td>#004 DAC 1.66V</td>
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<td>96</td>
<td>999995691</td>
<td>1000004389</td>
<td>8698</td>
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<tr>
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<td>96</td>
<td>99999416</td>
<td>1000000532</td>
<td>1216</td>
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<tr>
<td>#004 DAC 1.66V</td>
<td>10 K</td>
<td>999999980</td>
<td>96</td>
<td>99999418</td>
<td>1000000554</td>
<td>1136</td>
</tr>
</tbody>
</table>

Table 5: Summary from measurements of Figure 18
Removing the ±4 ns spike through data processing, gives the following clean measurements.

**Figure 19:** Test Setup 3, 3 sets of measurements without ±4 ns spikes

<table>
<thead>
<tr>
<th>Board</th>
<th>Data Volume</th>
<th>Mean (ps)</th>
<th>Sigma (ps)</th>
<th>Min (ps)</th>
<th>Max (ps)</th>
<th>Max-Min (ps)</th>
</tr>
</thead>
<tbody>
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<td>#004 DAC 1.66V</td>
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<tr>
<td>#004 DAC 1.66V</td>
<td>10 K</td>
<td>999999975</td>
<td>96</td>
<td>999999416</td>
<td>1000000632</td>
<td>1216</td>
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<tr>
<td>#004 DAC 1.66V</td>
<td>10 K</td>
<td>999999980</td>
<td>96</td>
<td>999999418</td>
<td>1000000554</td>
<td>1136</td>
</tr>
</tbody>
</table>

**Table 6:** Summary from measurements of Figure 19
**Test Setup 4 | Sweeping**

We use the PCIE_FMC_TESTBENCH5 front end in the 864-1-A17 lab where we plug two SPEC carrier boards as Figure 20 indicates.

SPEC 1 carries a Fine Delay mezzanine, used as pulse generator at different frequencies. SPEC 2 carries the TDC mezzanine under test.

A dedicated python testing program is responsible for setting the fine delay output period to a range of values from 100 ns to 150 us with steps of 20 ns \(^1\). For each period value, 128 pulses are sent. The TDC timestamps are retrieved and manipulated: only timestamps corresponding to rising edges are kept and they are subtracted by pairs.

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\[^1\] Because of system limitations the sweeping above 150us is currently not possible. In detail because of the TDC and FD drivers incompatibility, the FD board is used uncalibrated; this makes the values above 150us giving errors > 4ppm, so there would be no reliable reference for our testing.
Figure 22 shows the 500 K data ranging from 100 ns to 150 us.

Figure 22: Test Setup 4 measurements

Zooming into Figure 22 brings us to Figure 23 that shows the first steps of this test. Note the 64 measurements per step.

Figure 23: Zoom in Figure 20

The measurements stayed within the range of the accuracy of the TDC plus the FD: 
\[\pm 700 \text{ ps} \pm 4 \text{ ppm}\] + \[\pm 500 \text{ ps} \pm 4 \text{ ppm}\].
The following figures show the measurements with two different DAC values at 100ns and 150 us.

Figure 24: Measurements at around 100 ns with different DAC values

Figure 25: Measurements at around 150 us with different DAC values

Conclusions

The tests have confirmed the general reliability of the TDC board. The precision is within the [±700ps +timebase] specification.

The issue of the ±4ns spikes with 1 wrong timestamp every few millions would need to be clarified in collaboration with the ACAM engineers.

The calibration procedure would eliminate the offsets coming from the different channel paths.

The calibration procedure would also seek for the optimal DAC value.

On our long runs with the Cesium 1 PPS, we remarked a drift of around 13’000 ps per °C. Note that there will be no temperature compensation in our application; adding however White Rabbit would completely eliminate this temperature drifting.