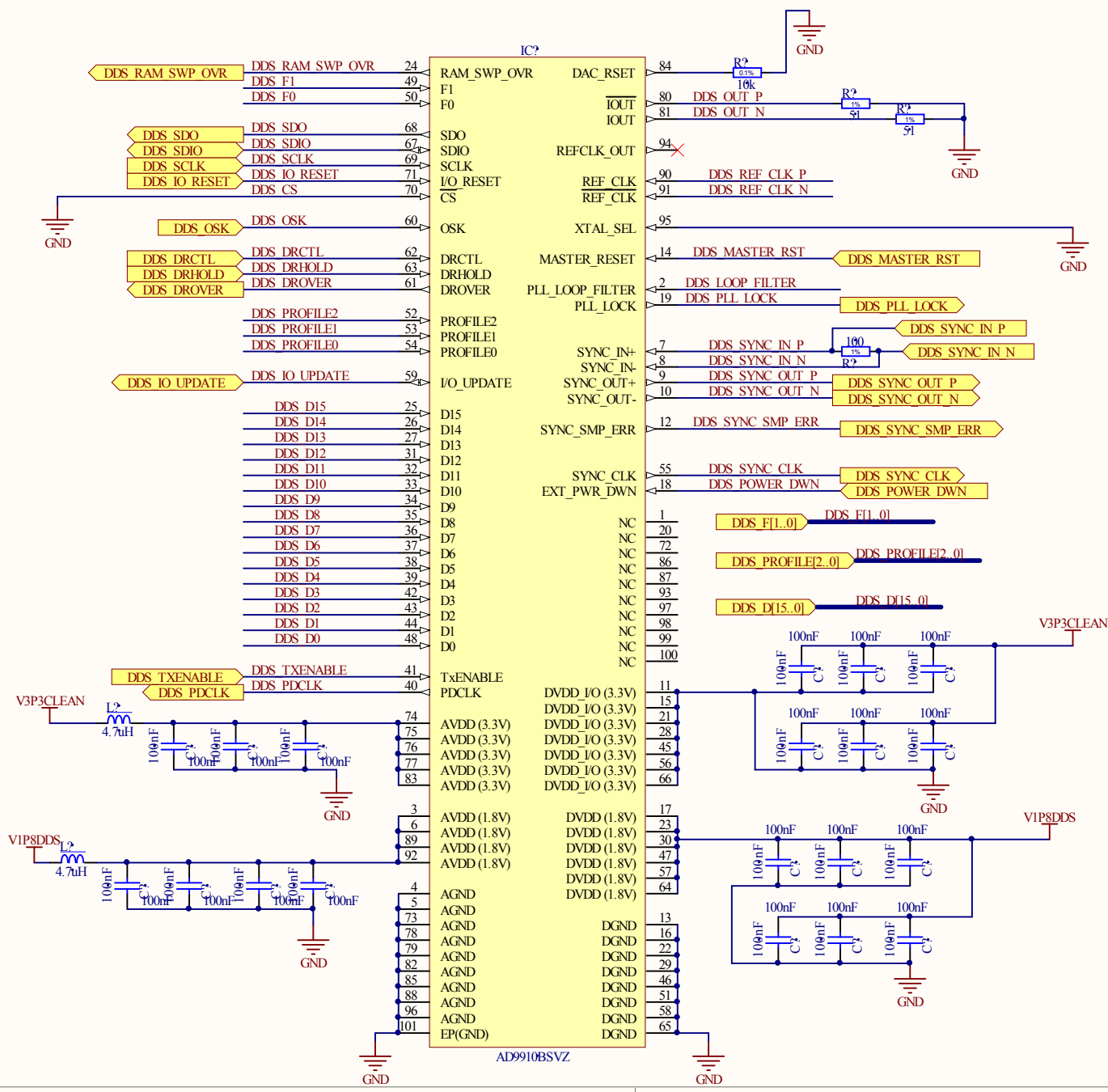
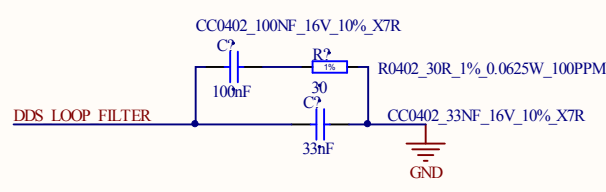
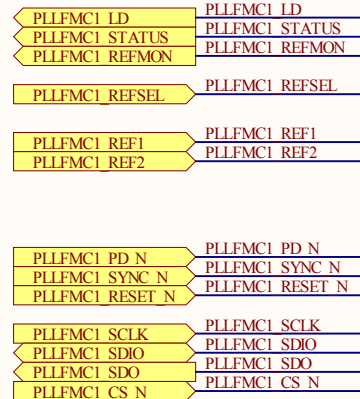
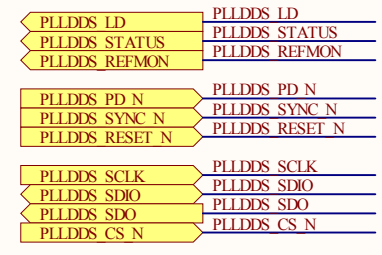
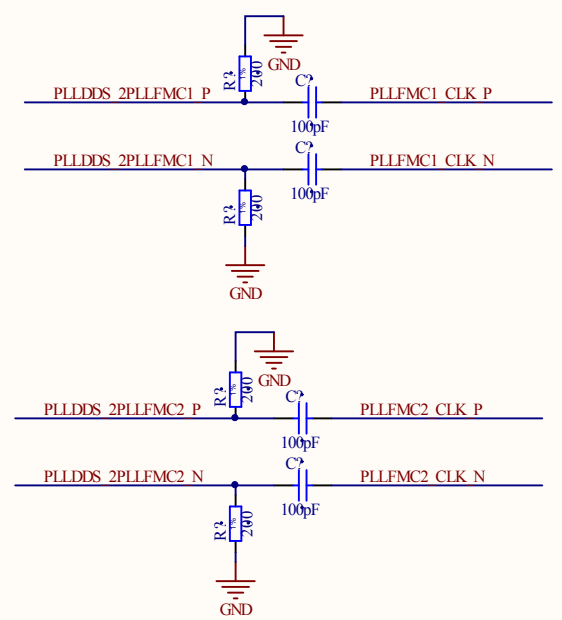
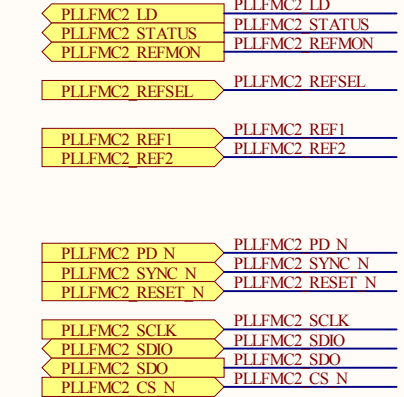


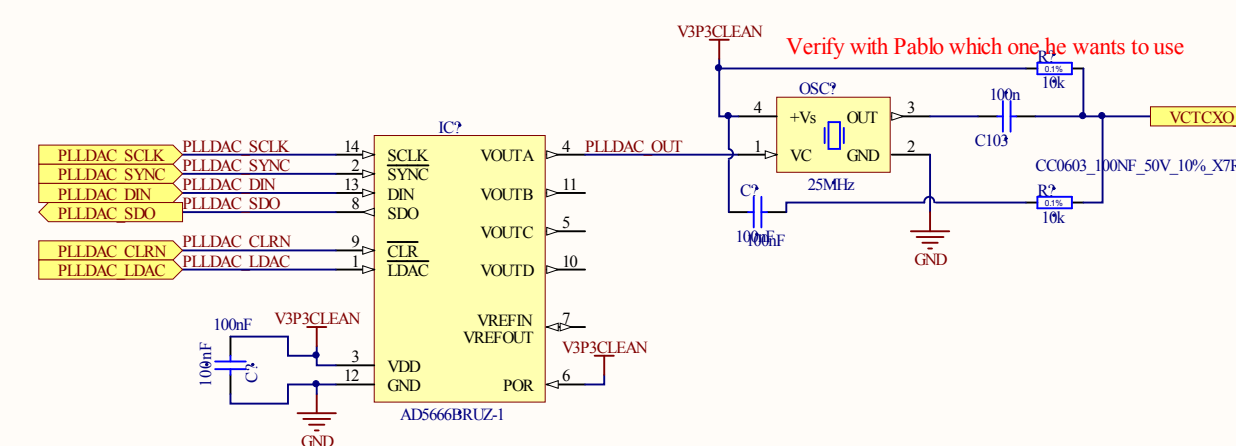
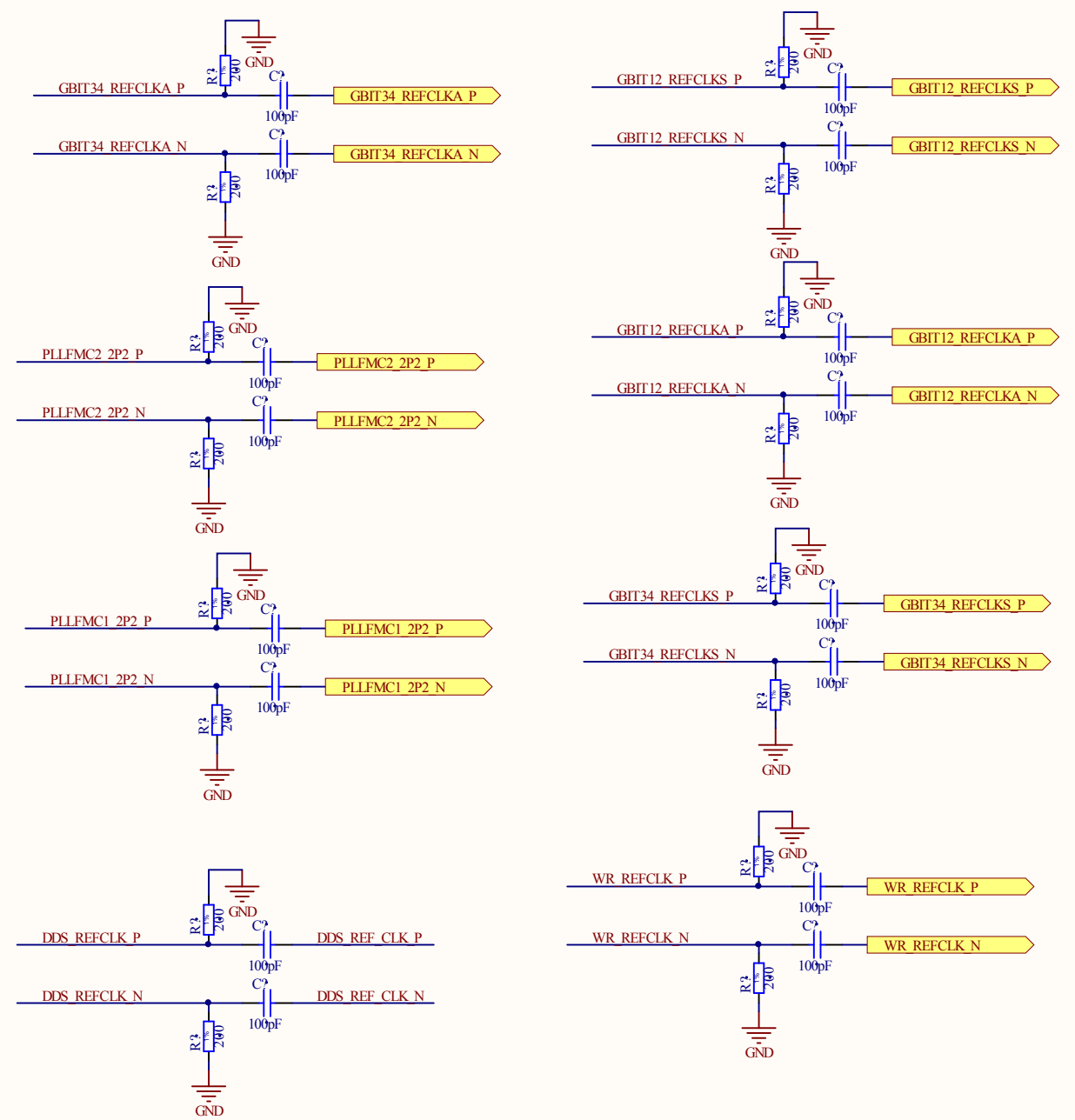
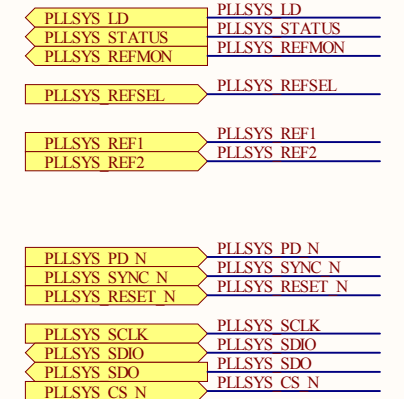
PhaseDetector @ 40MHz

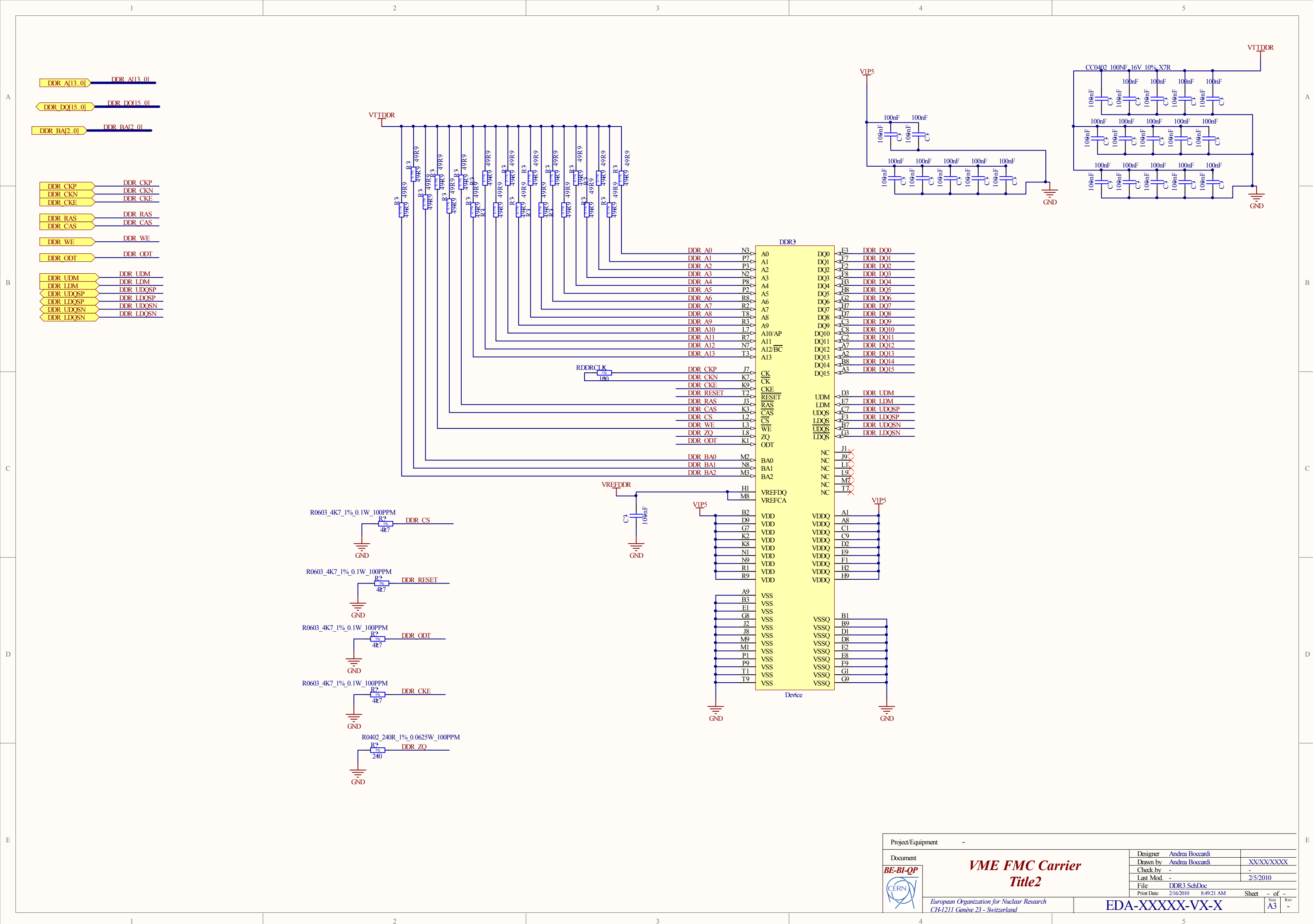


PhaseDetector @ 40MHz

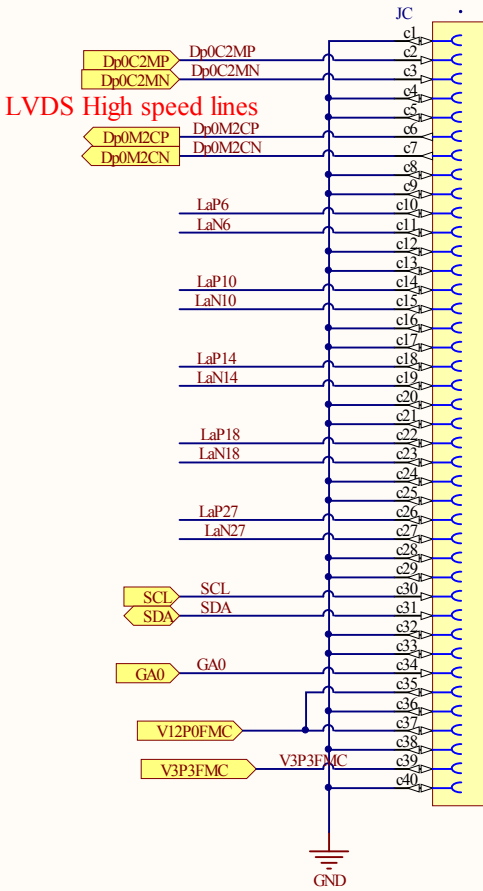
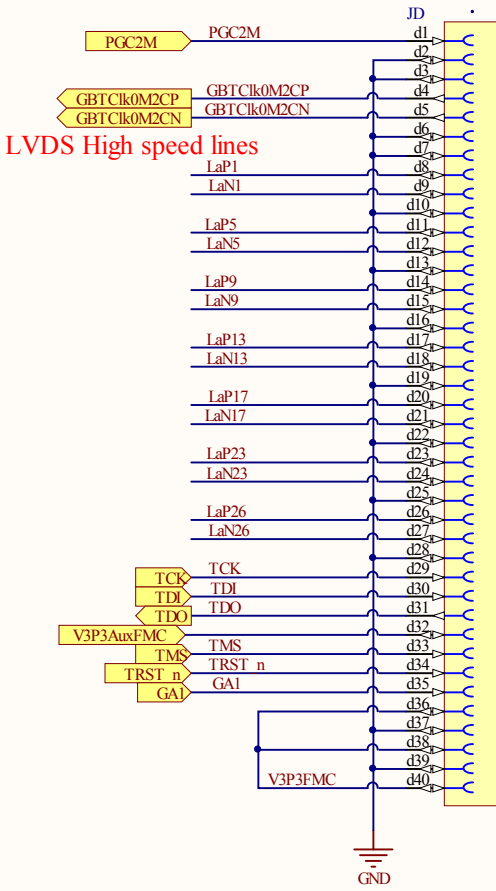
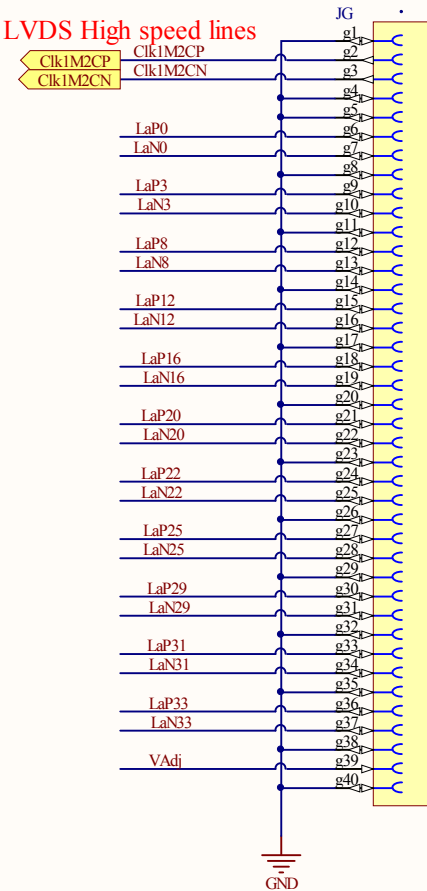
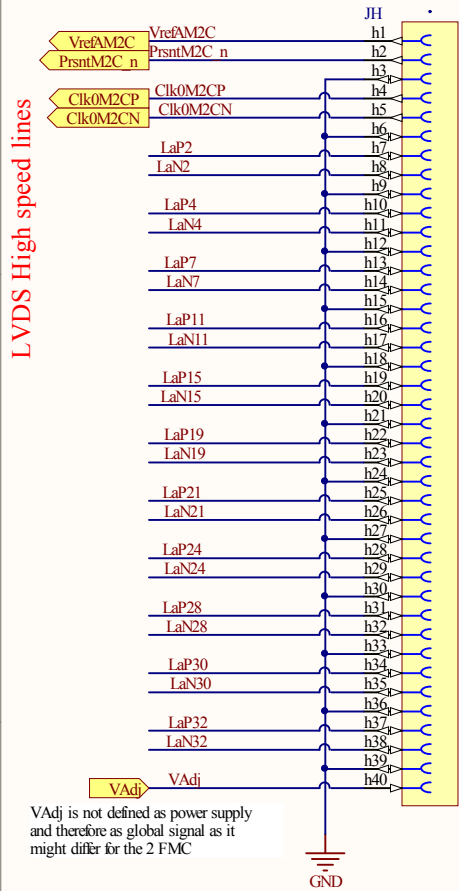


PhaseDetector @ 40MHz

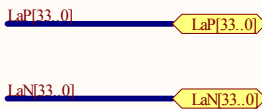




Low Pin Count Rows

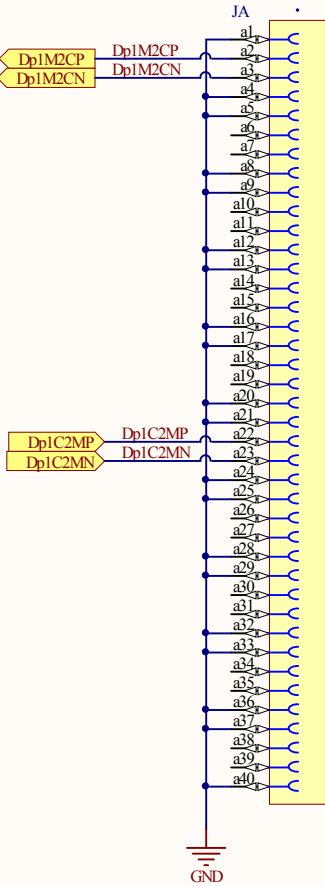
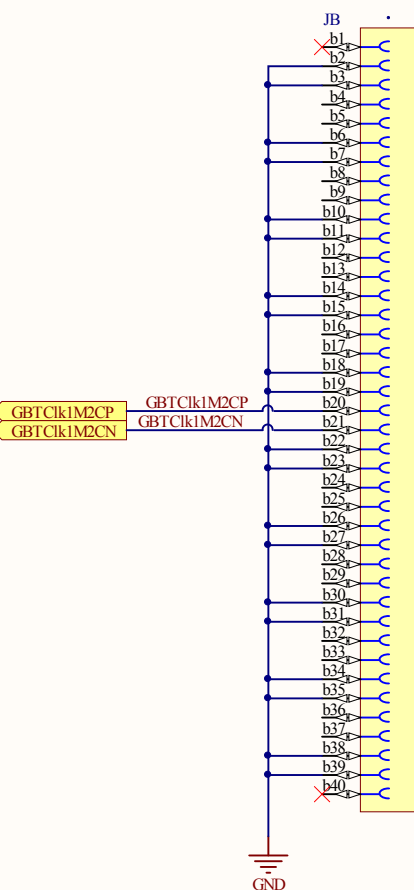
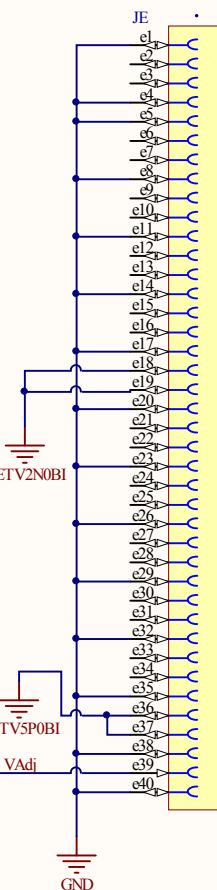
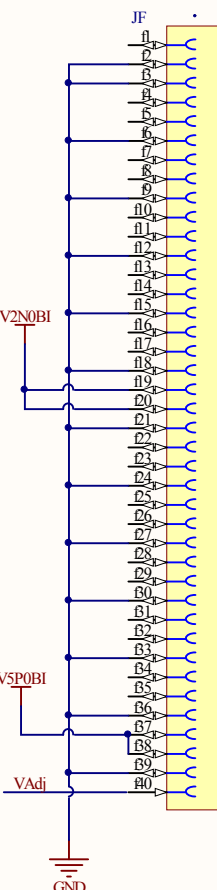
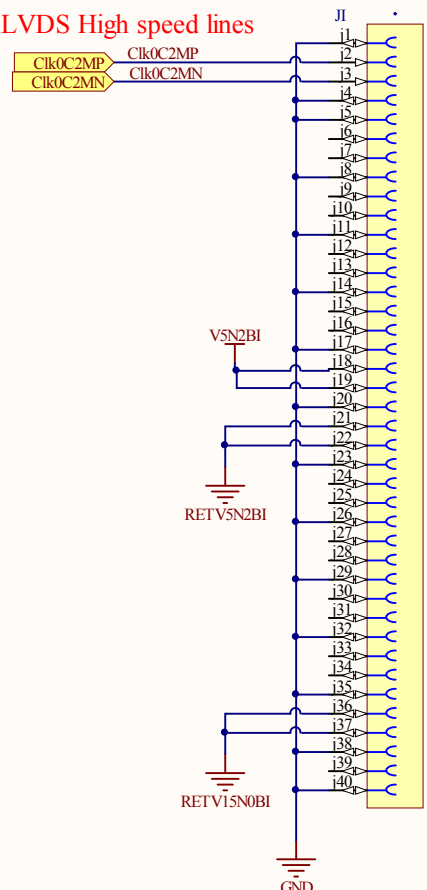
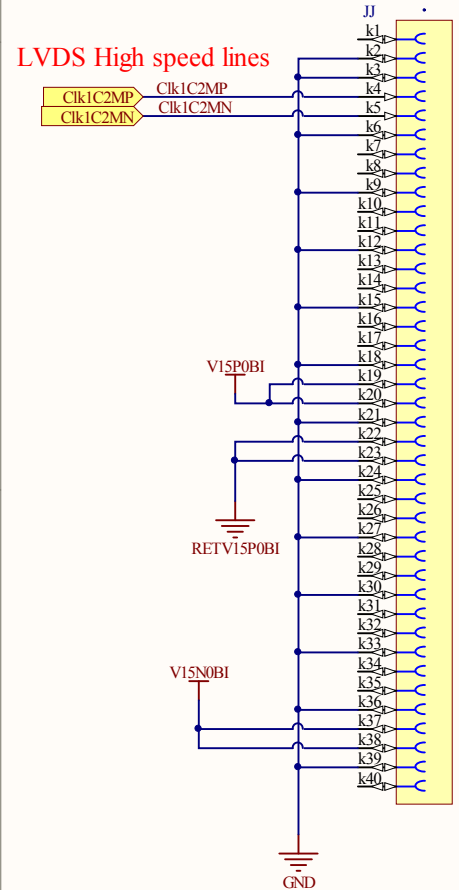


LaP and LaN are LVDS lines



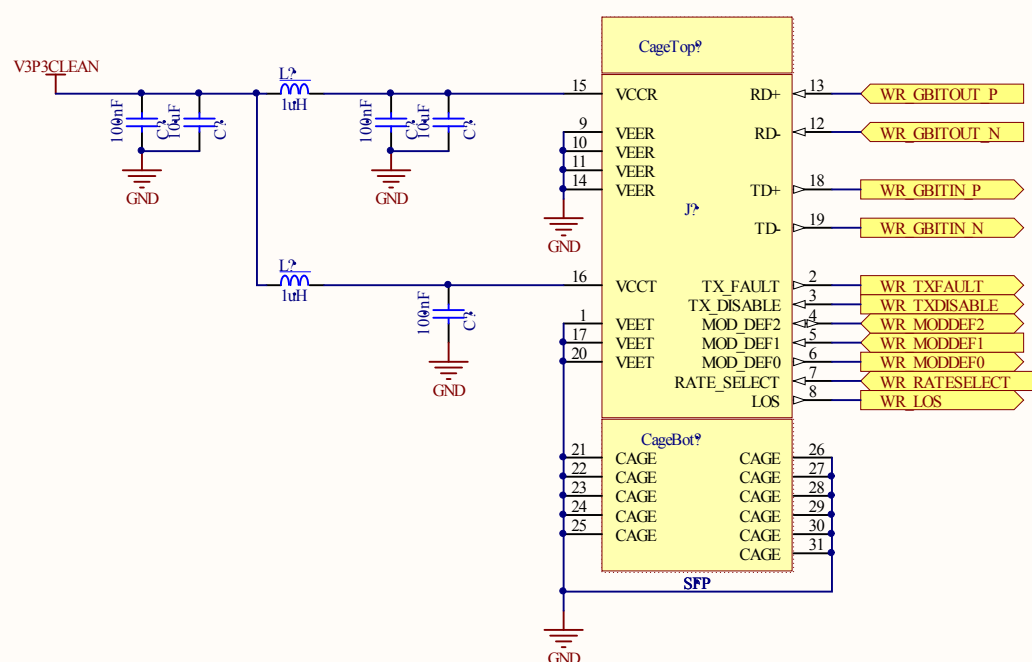
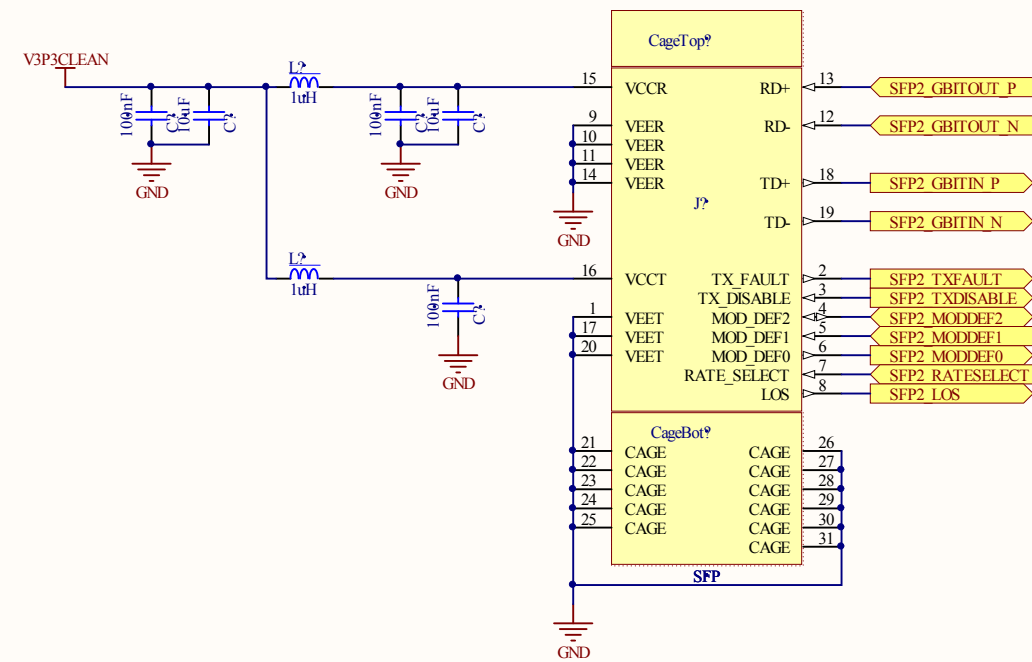
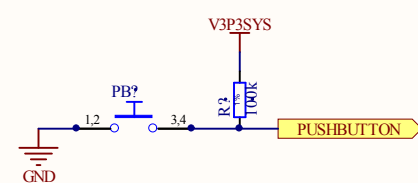
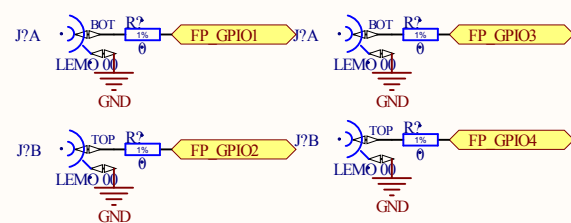
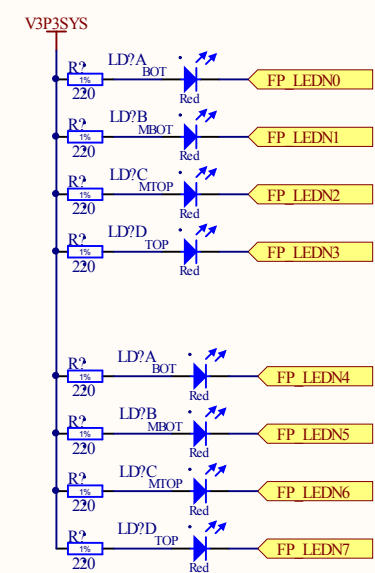
NB: the LVDS pairs must have a differential impedance of 100 ohm and be routed with no skew between the P and the N lines. The skew between the various La pairs should be kept as low as possible.

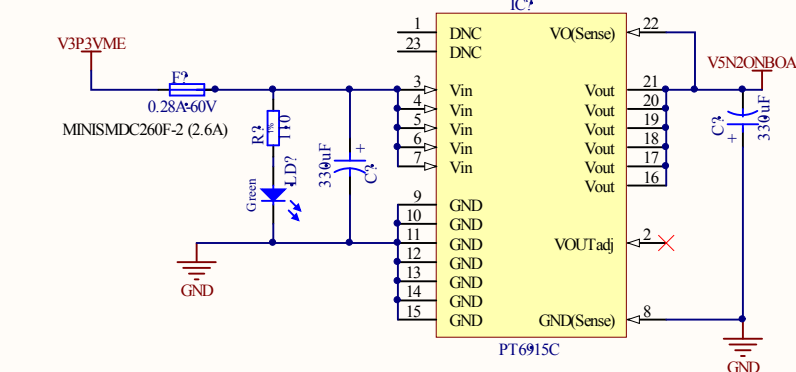
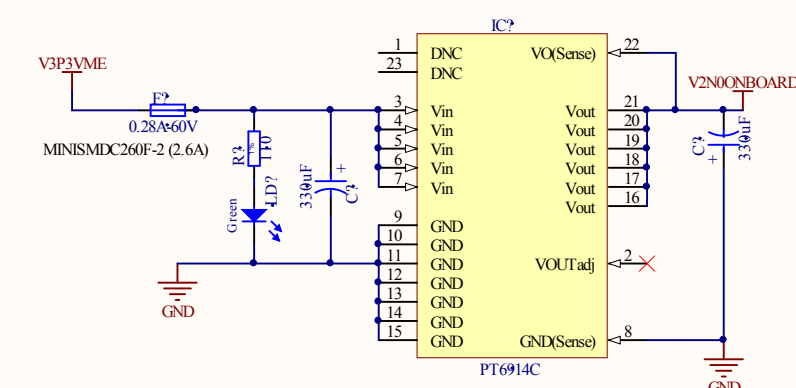
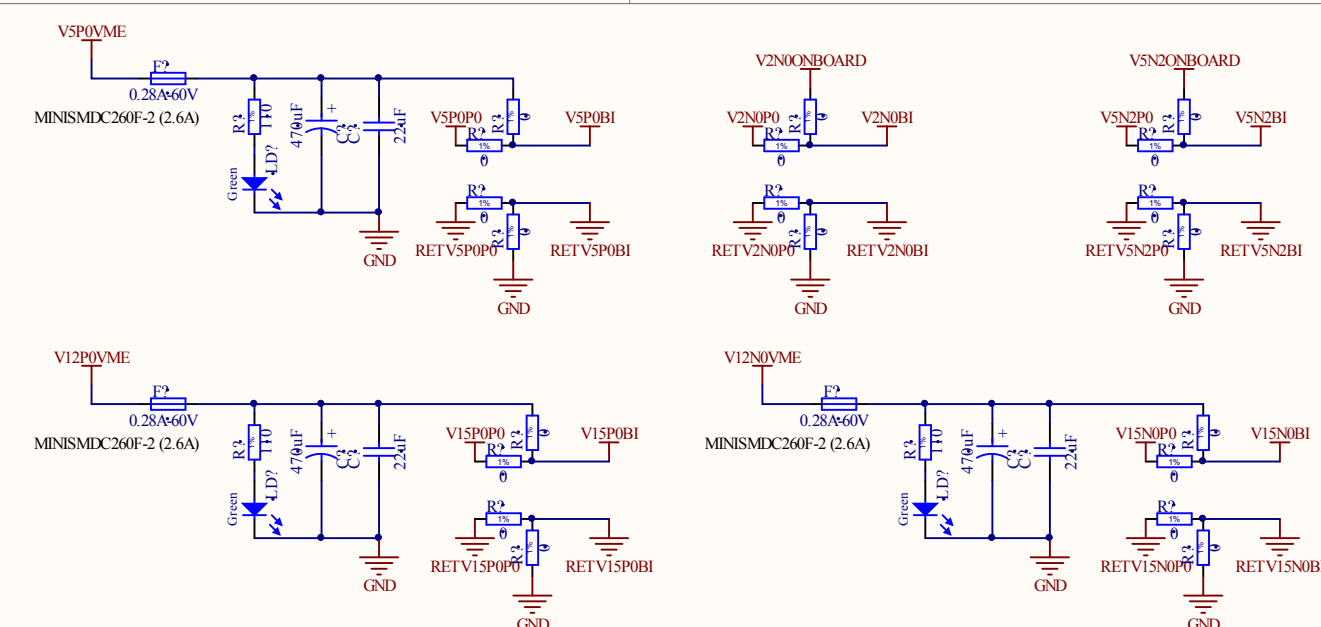
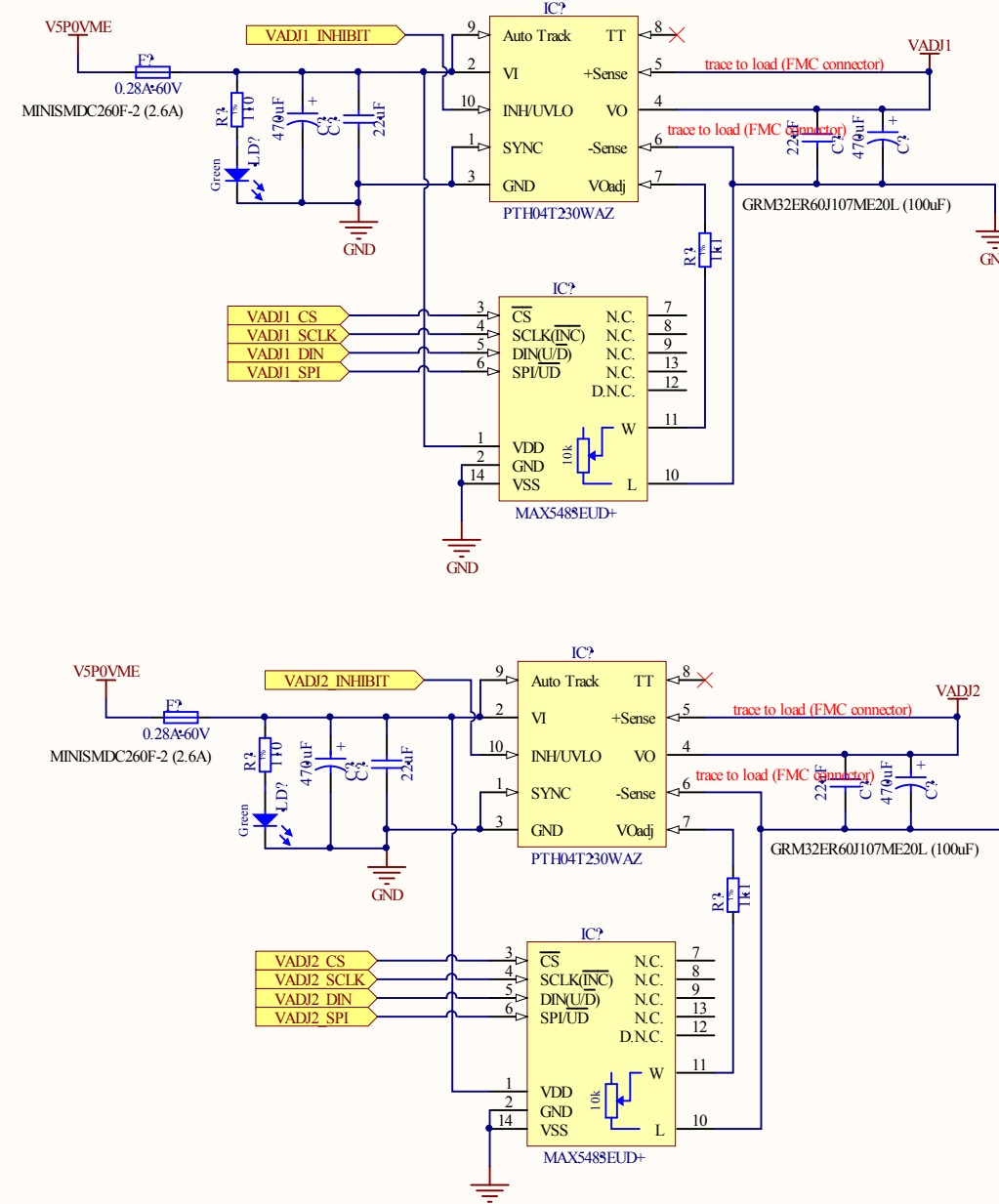
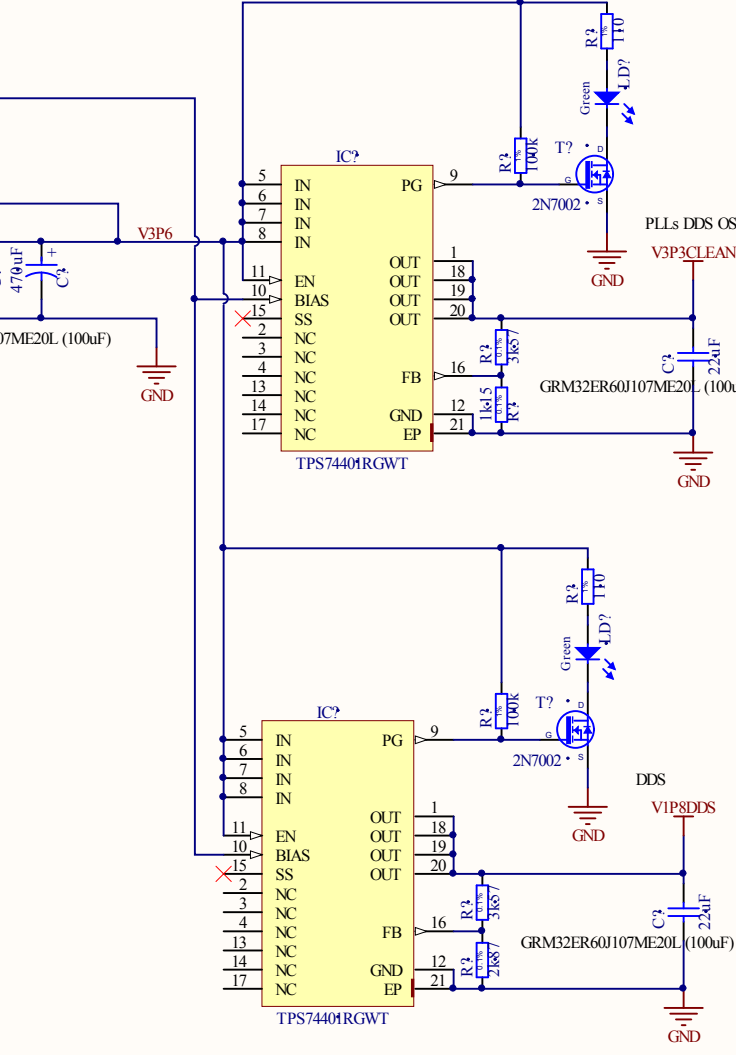
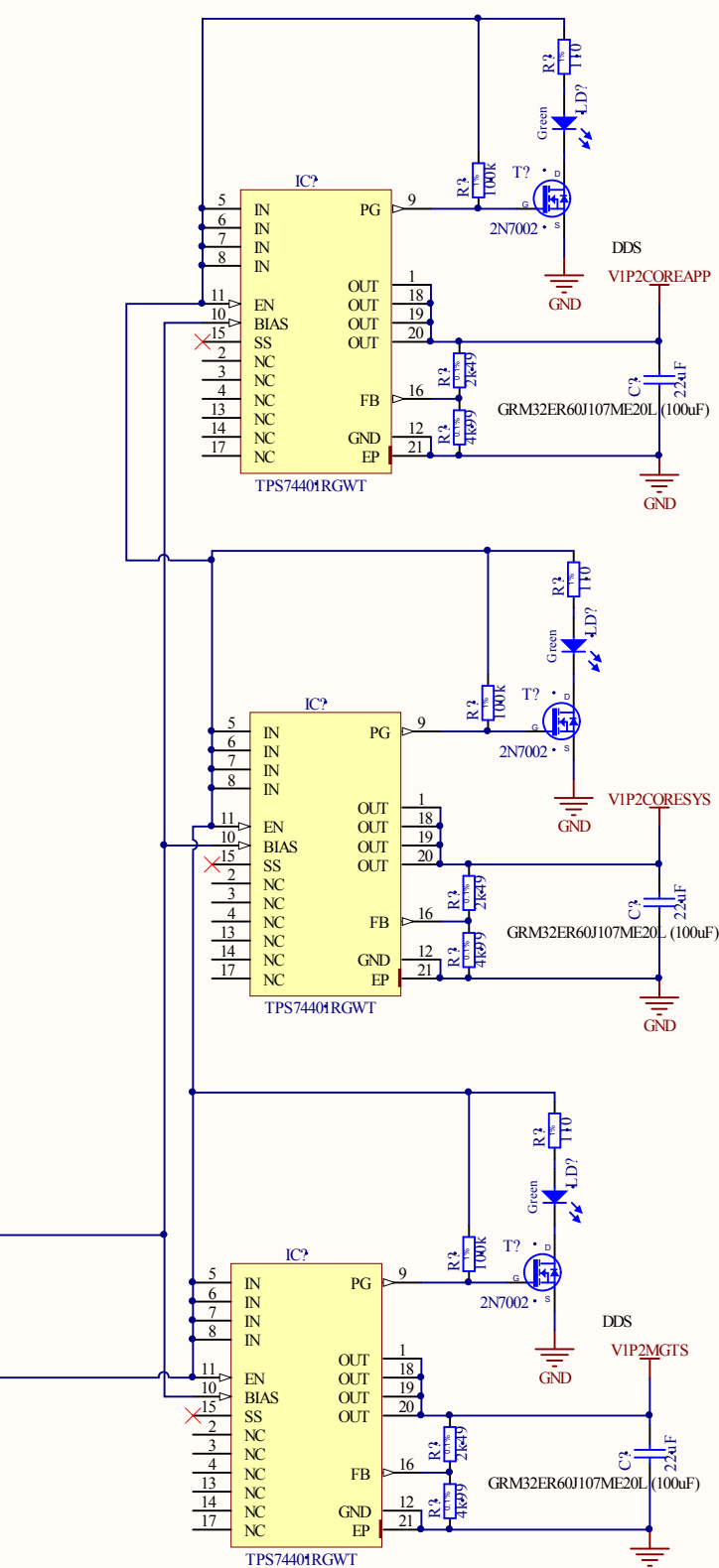
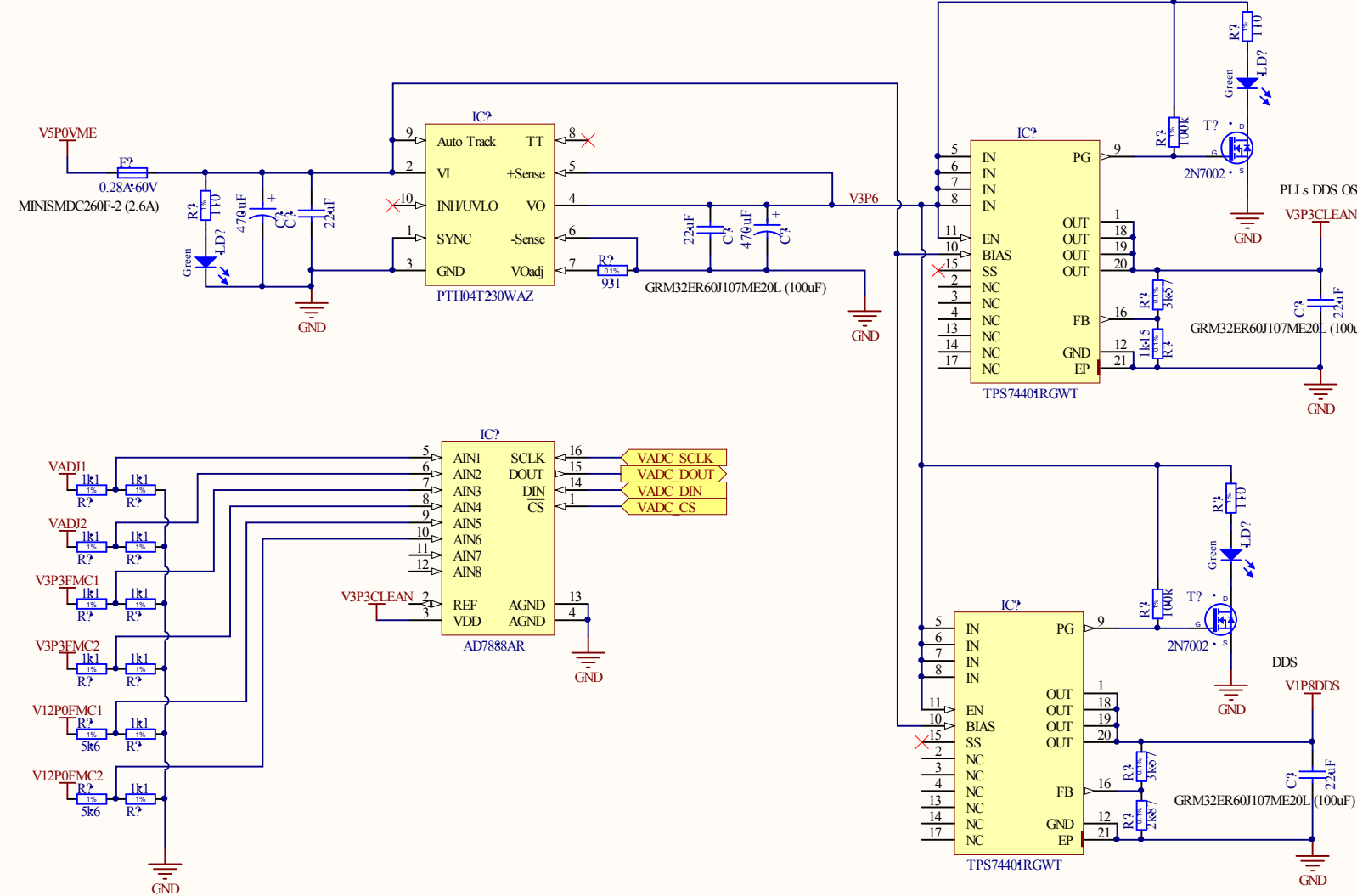
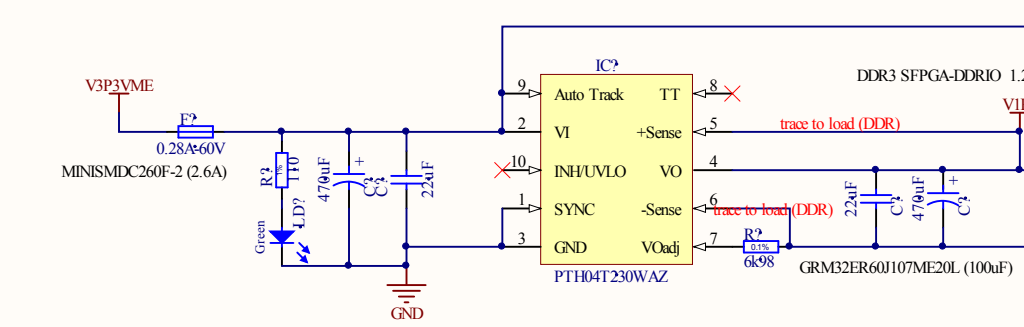
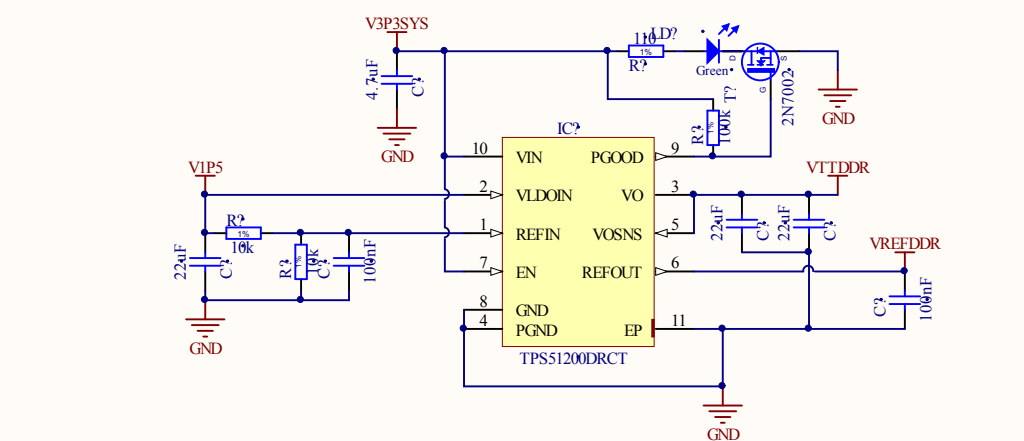
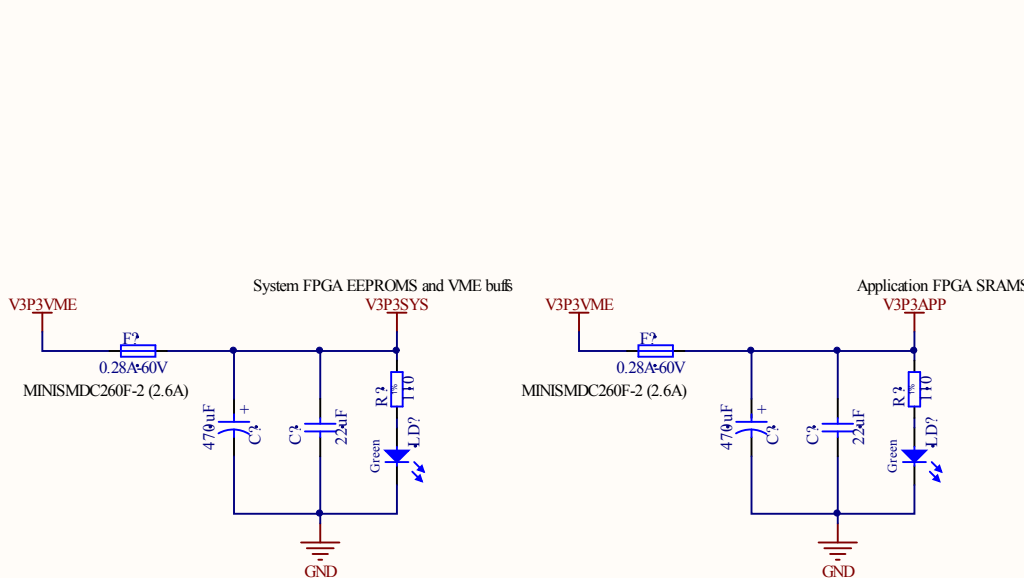
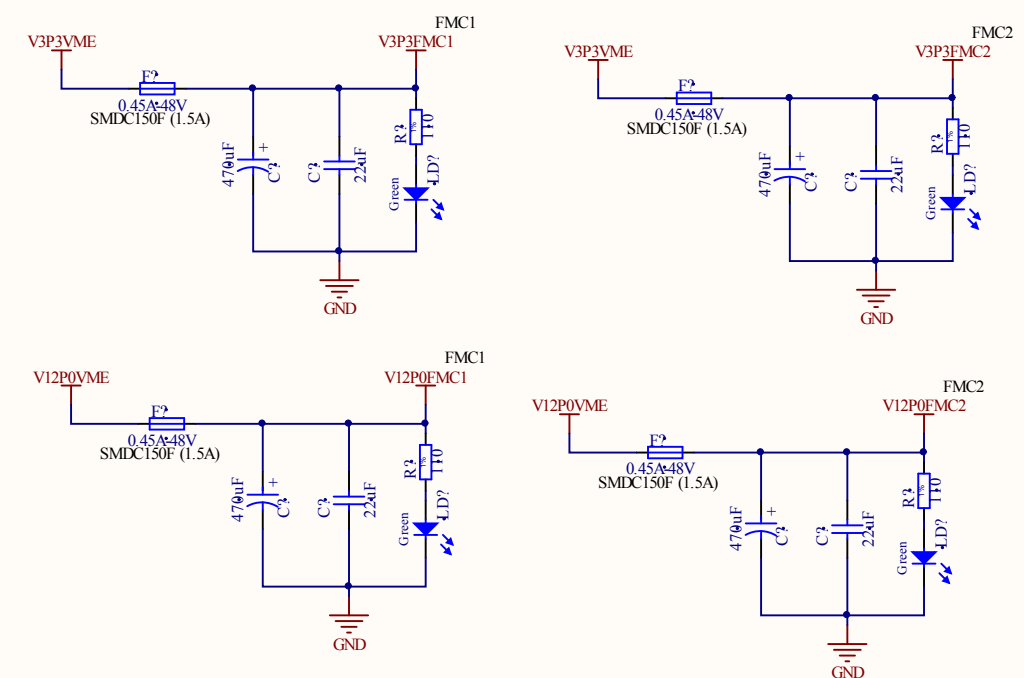
High Pin Count Rows



Project/Equipment		-	
Document		Designer	Andrea Boccardi
BE-BI-OP		Drawn by	Andrea Boccardi
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CERN		Last Mod.	2/10/2010
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		Rev	-

VME FMC Carrier
FMC Connector





ADDRESS[24..0] ADDRESS[24..0] DATA[35..0] DATA[35..0]

Replace with the 3V3 version (same pinout)

