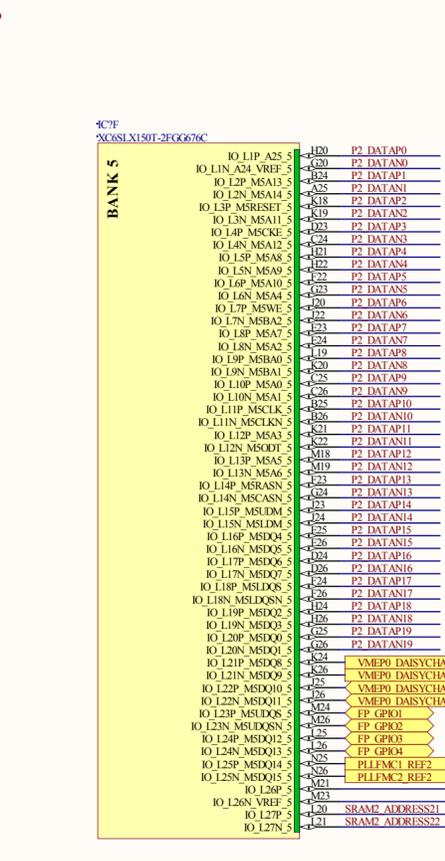
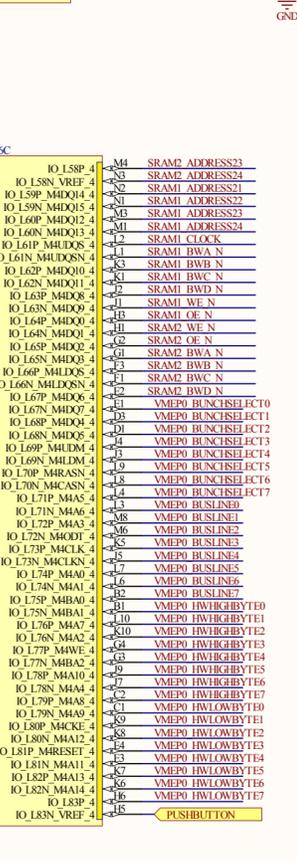
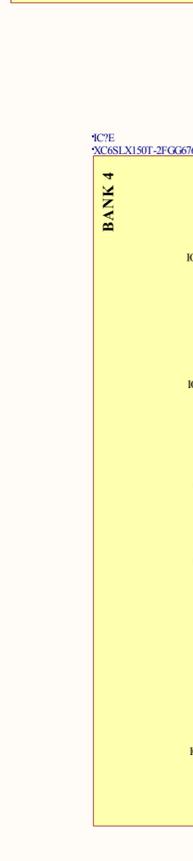
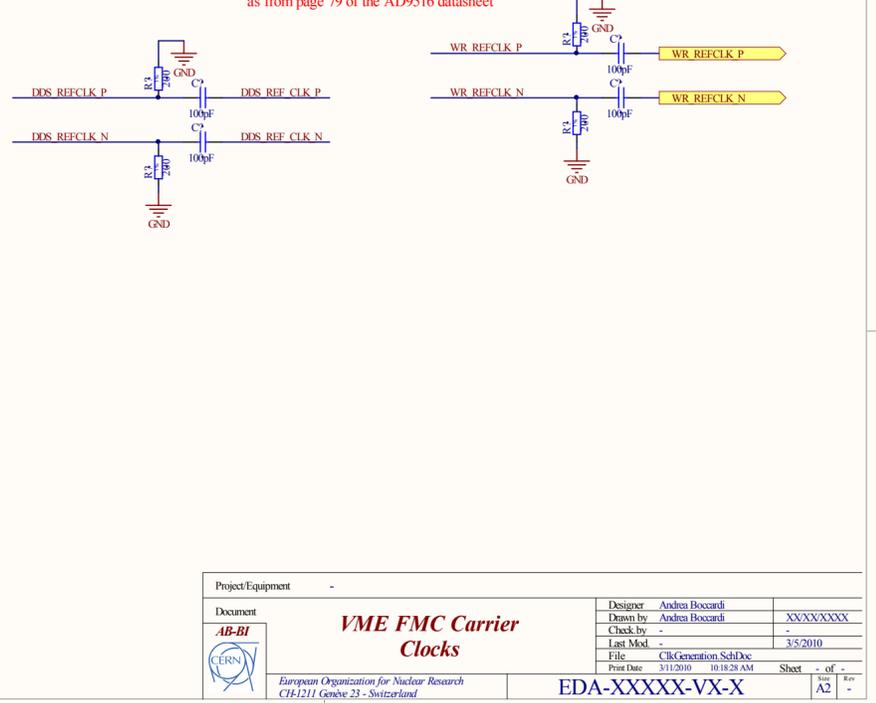
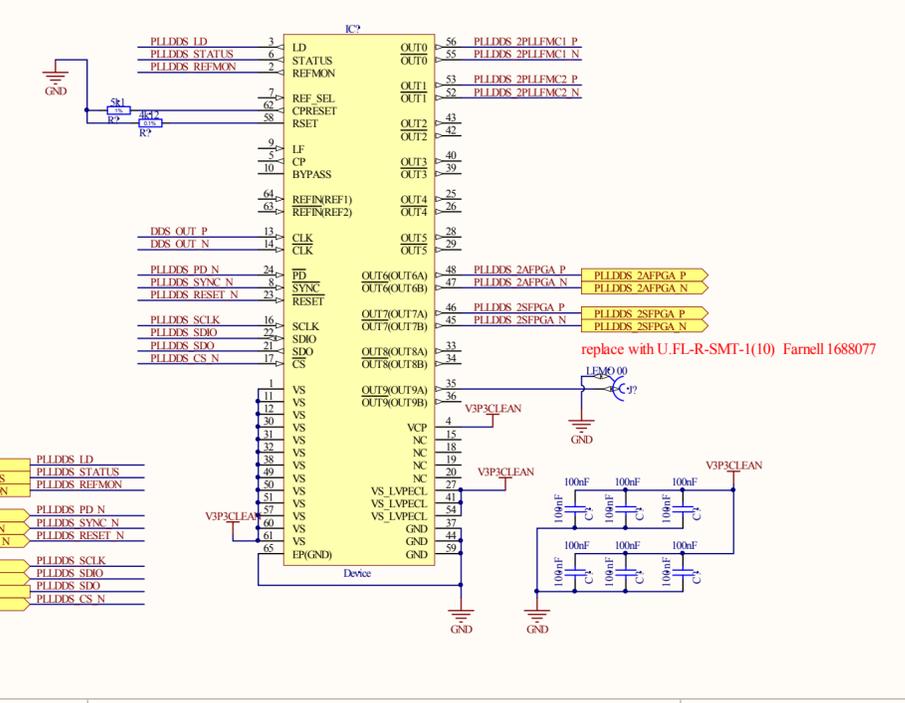
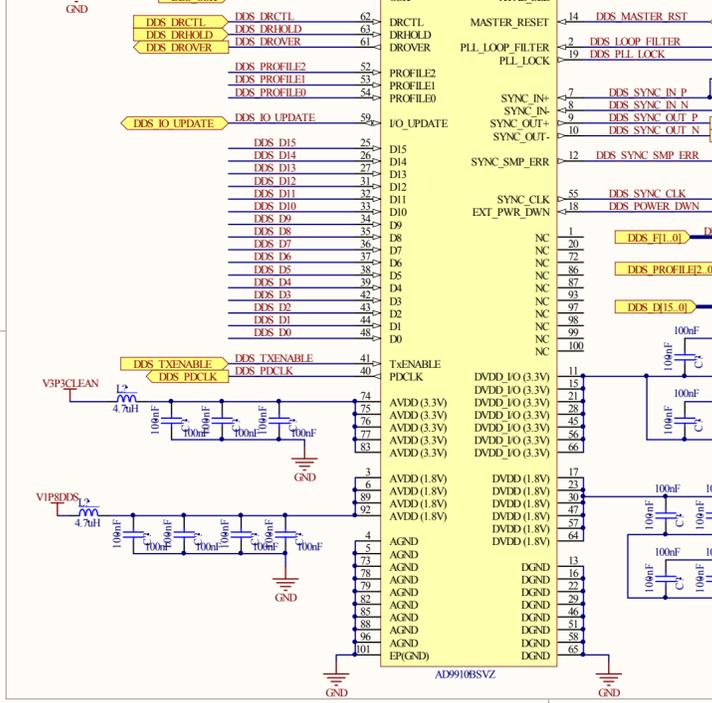
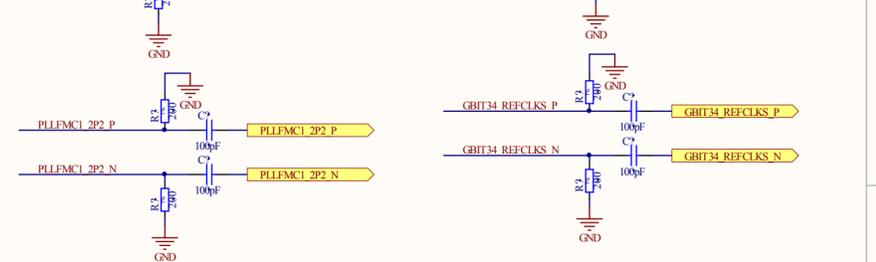
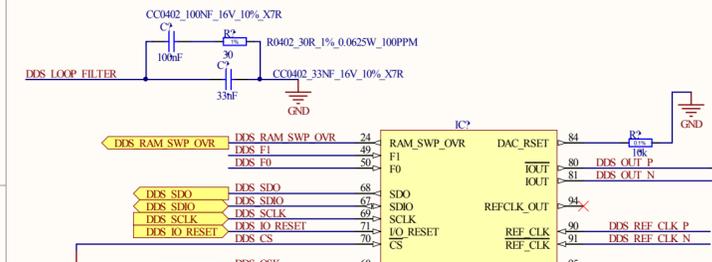
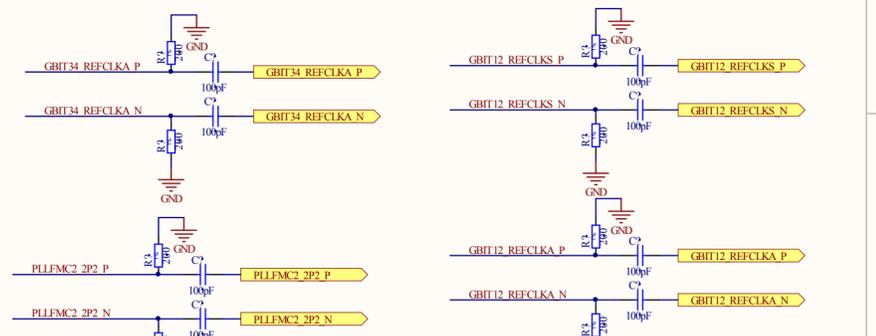
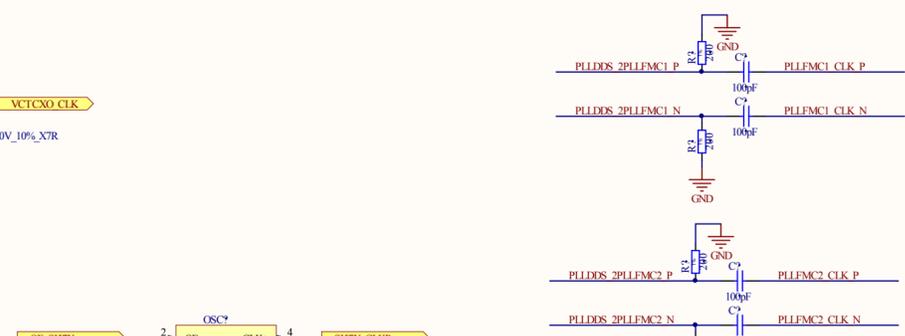
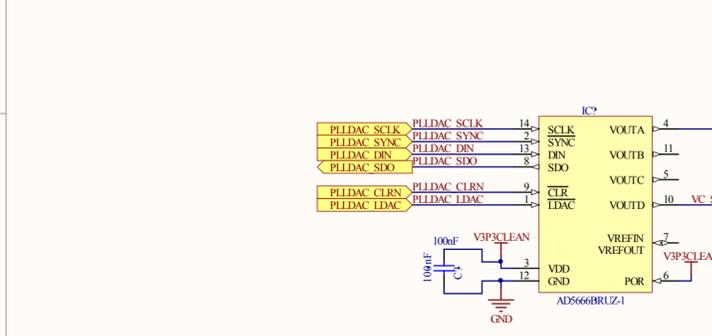
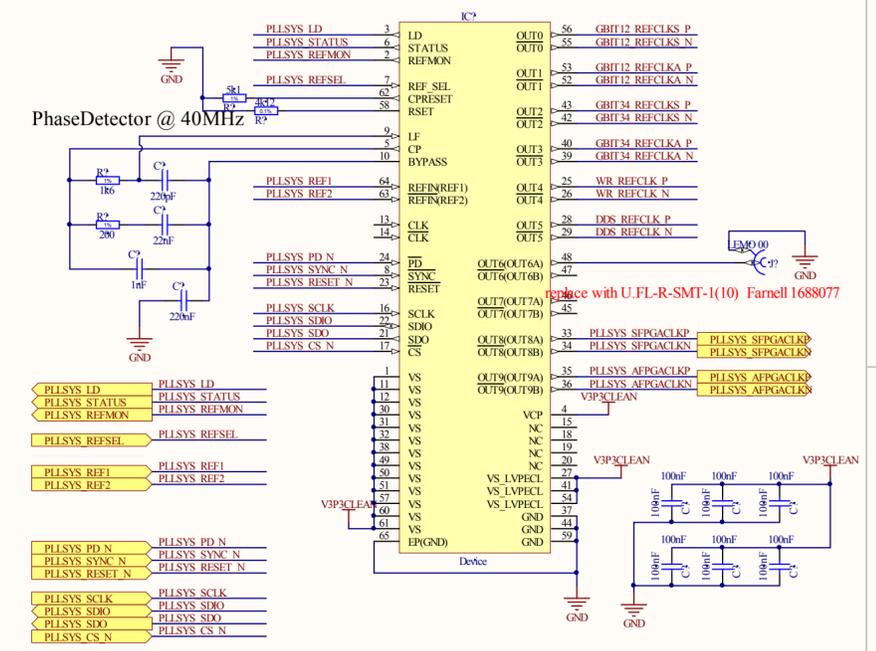
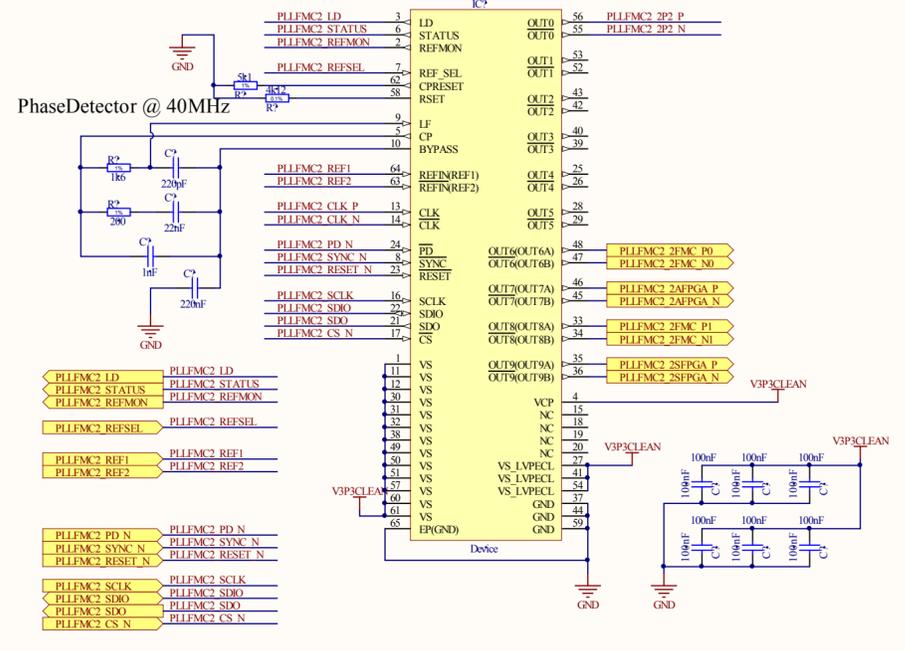
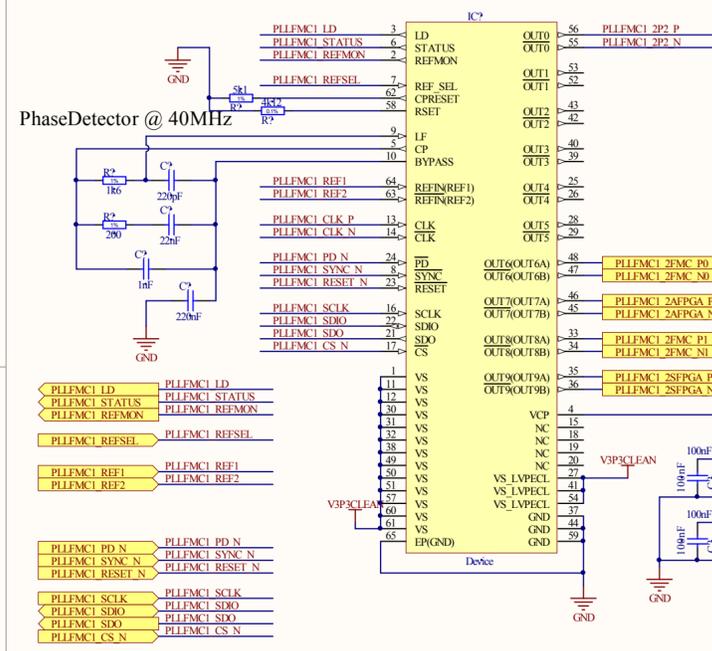


the VREF could not be used for the 2nd mezzanine
The 2nd mezzanine has 2 differential IO pairs less





as from page 79 of the AD9516 datasheet

replace with U.FL-R-SMT-1(10) Farnell 1688077

Project/Equipment	-	Designer	Andrea Boccardi
Document	-	Drawn by	Andrea Boccardi
AB-BI	VME FMC Carrier Clocks	Check by	-
ERN		Last Mod.	3/5/2010
		File	ClkGeneration_SchDoc
		Print Date	3/11/2010 10:18:28 AM
		Sheet	- of -
			A2

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EDA-XXXXX-VX-X

- DDR A[13..0] DDR A[13..0]
- DDR DQ[15..0] DDR DQ[15..0]
- DDR BA[2..0] DDR BA[2..0]

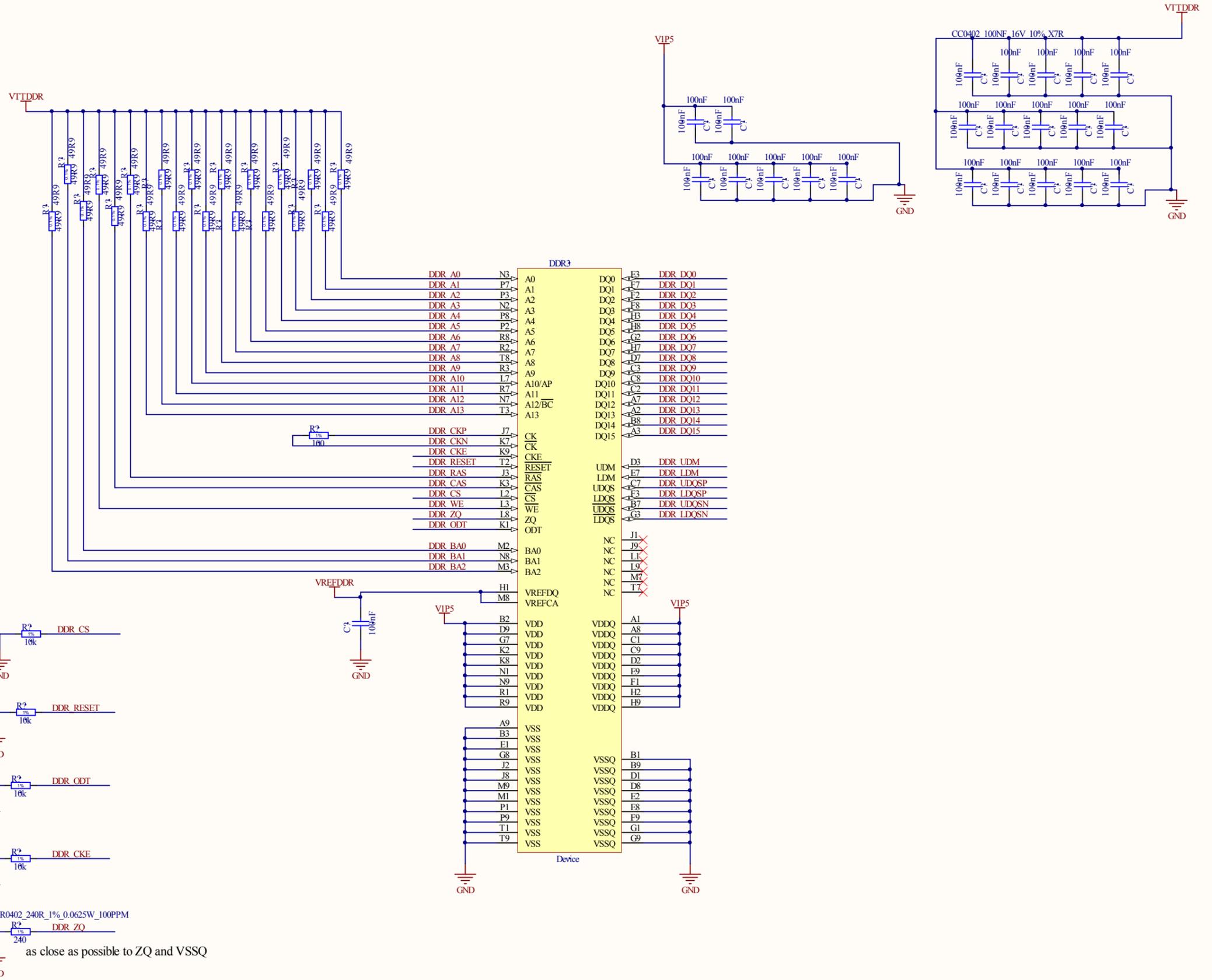
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- DDR CKN DDR CKN
- DDR CKE DDR CKE

- DDR RAS DDR RAS
- DDR CAS DDR CAS

- DDR WE DDR WE

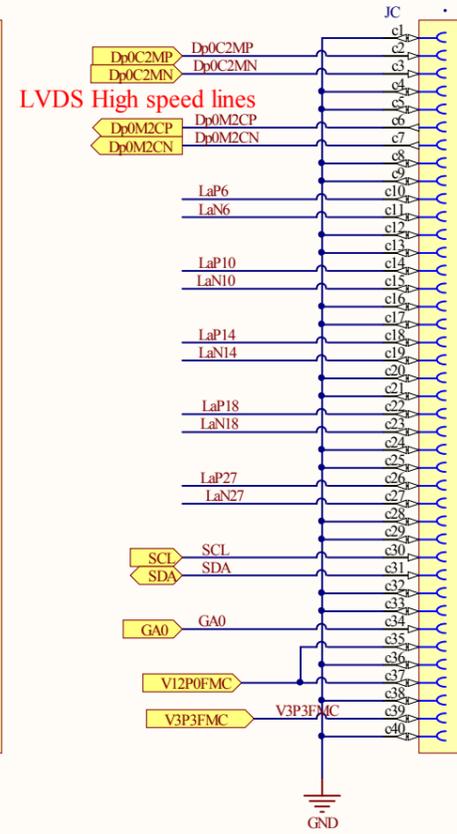
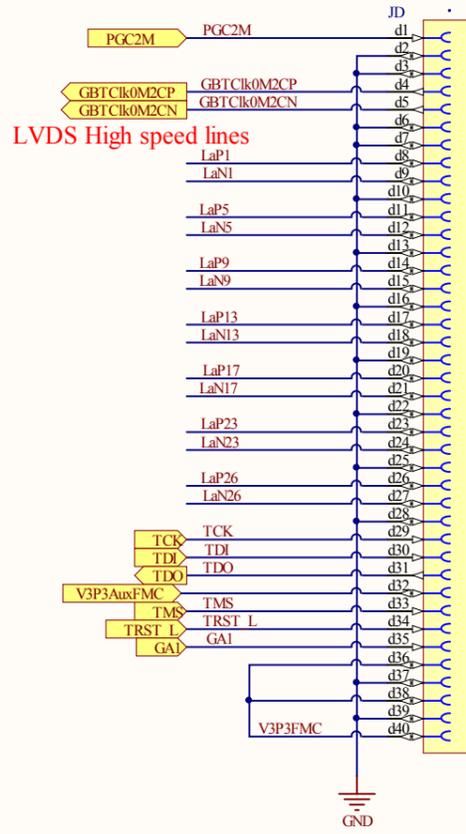
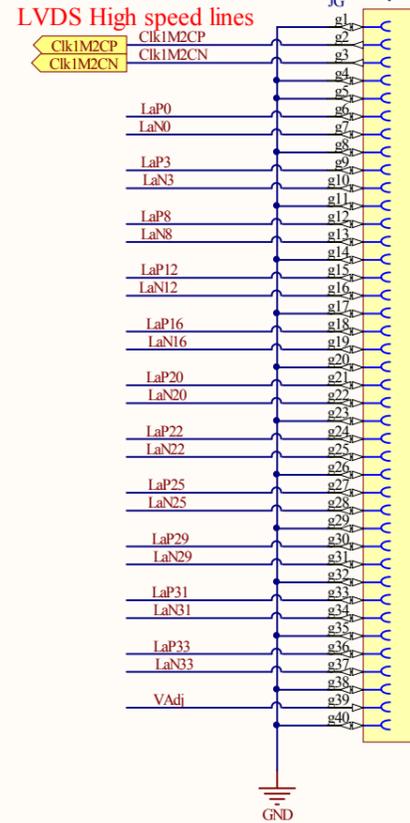
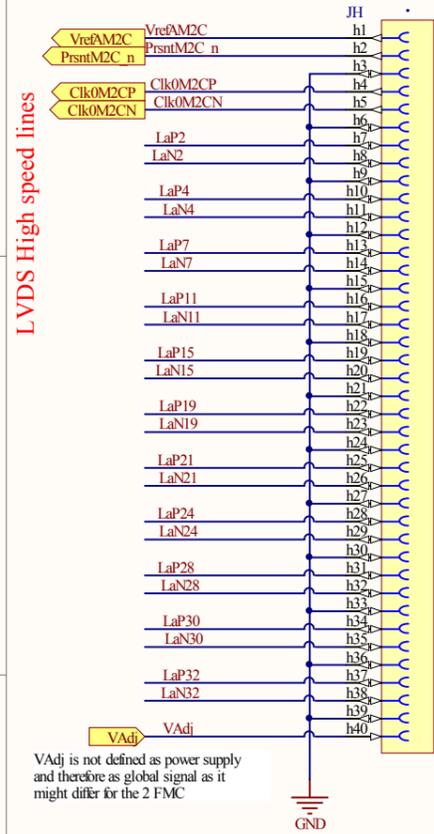
- DDR ODT DDR ODT

- DDR UDM DDR UDM
- DDR LDM DDR LDM
- DDR UDOSP DDR UDOSP
- DDR LDOSP DDR LDOSP
- DDR UDOSN DDR UDOSN
- DDR LDOSN DDR LDOSN

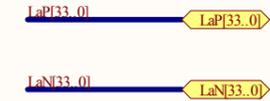


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Designer	Andrea Boccardi	Check by	XXXX/XXXX
Drawn by	Andrea Boccardi	Last Mod	3/5/2010
File	DDR3.SchDoc	Print Date	3/11/2010 10:18:29 AM
Sheet	- of -	Size	A3
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland		EDA-XXXXX-VX-X	

Low Pin Count Rows

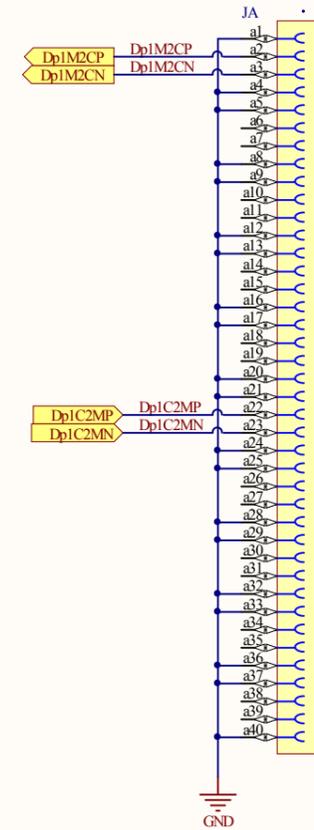
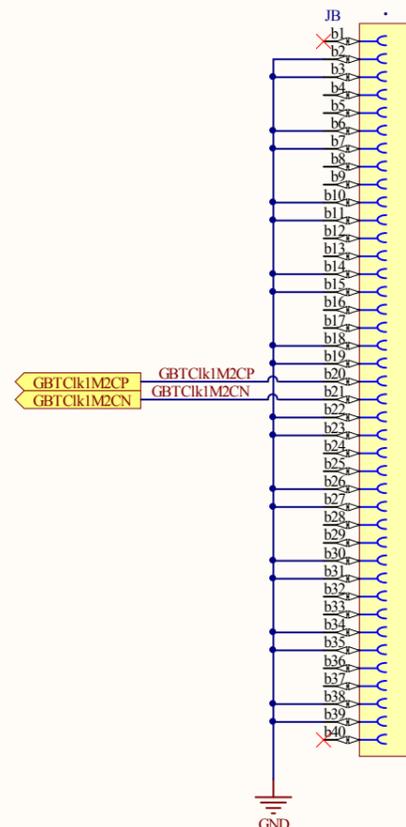
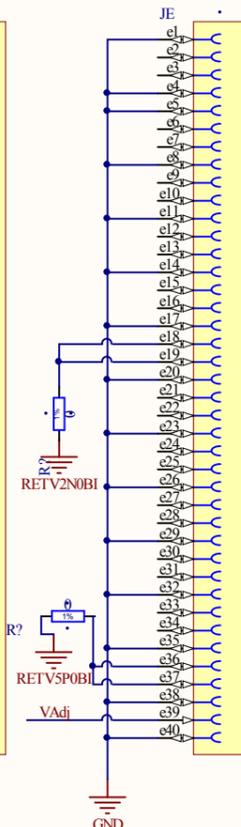
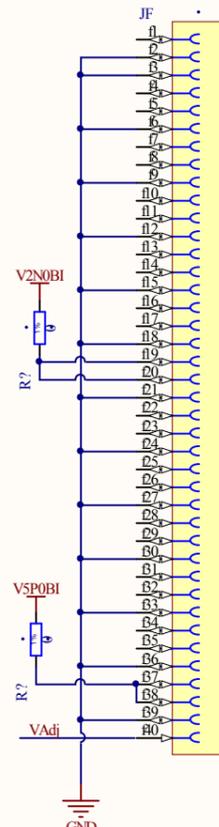
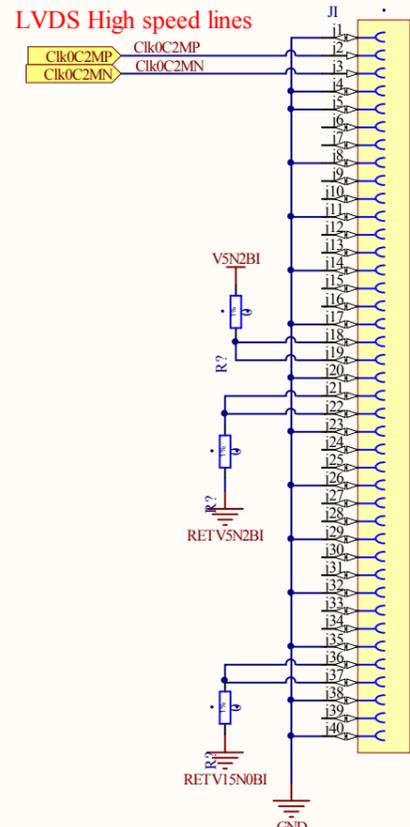
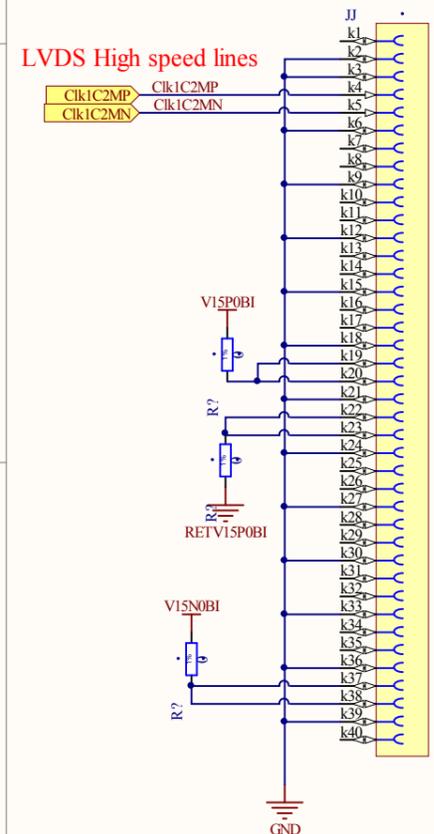


LaP and LaN are LVDS lines

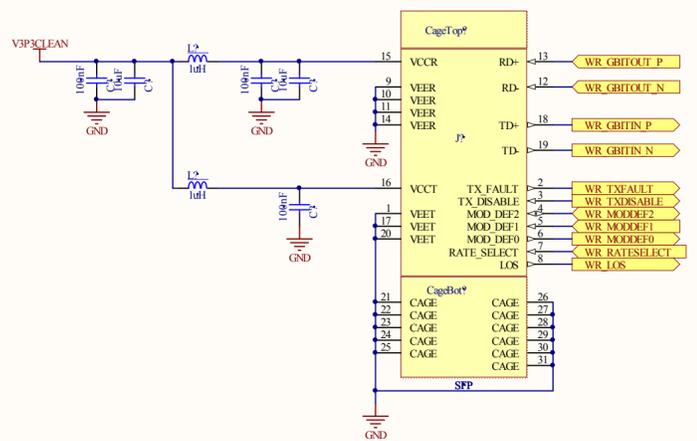
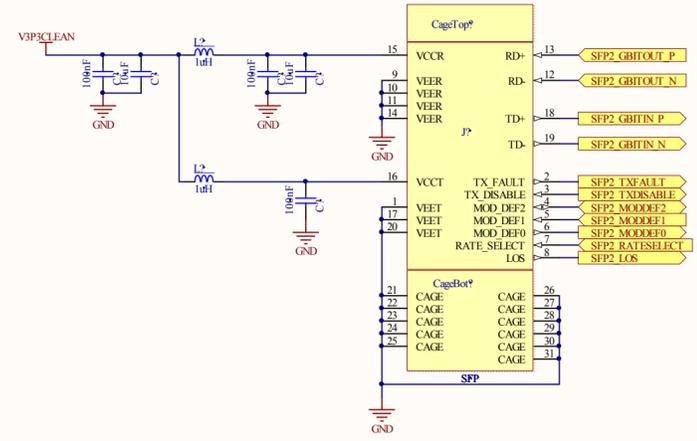
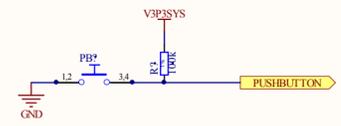
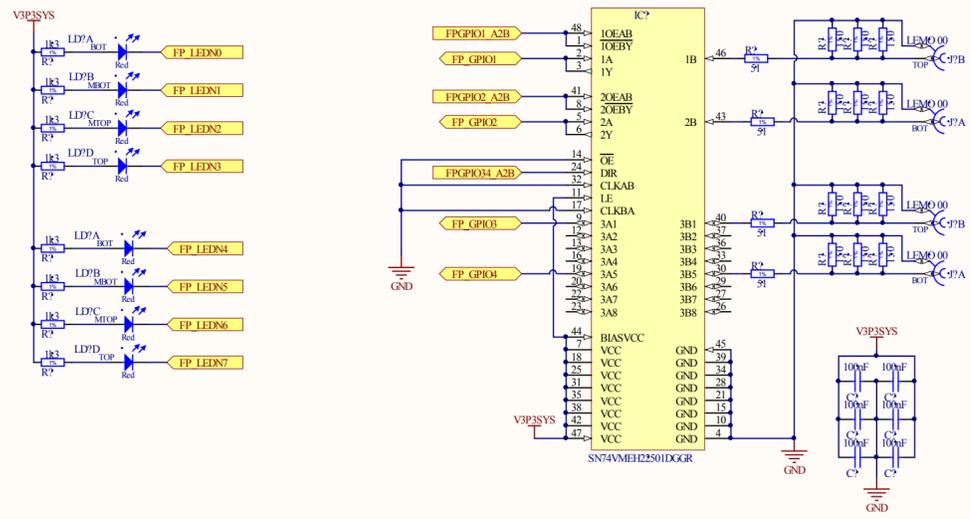


NB: the LVDS pairs must have a differential impedance of 100 ohm and be routed with no skew between the P and the N lines. The skew between the various La pairs should be kept as low as possible.

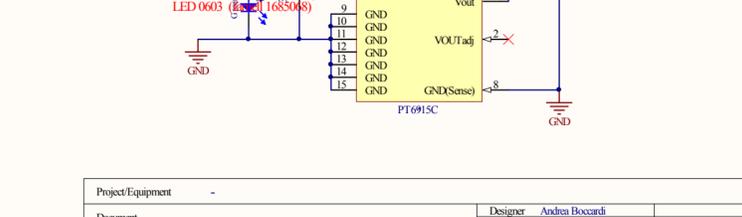
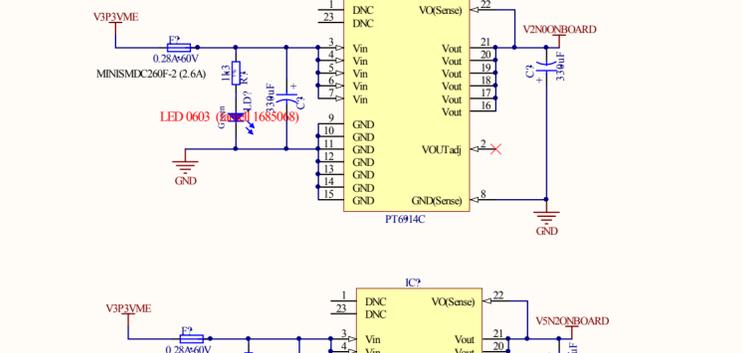
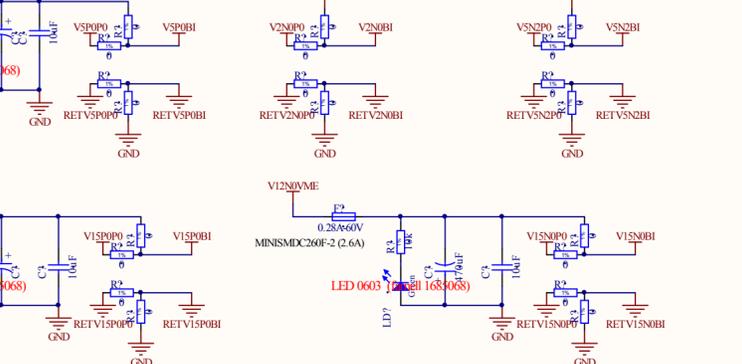
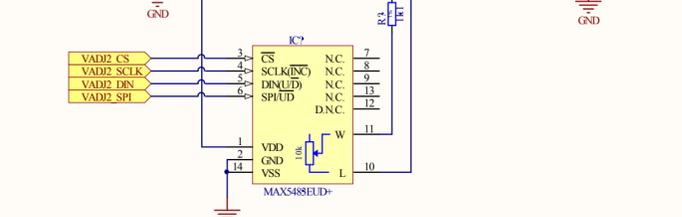
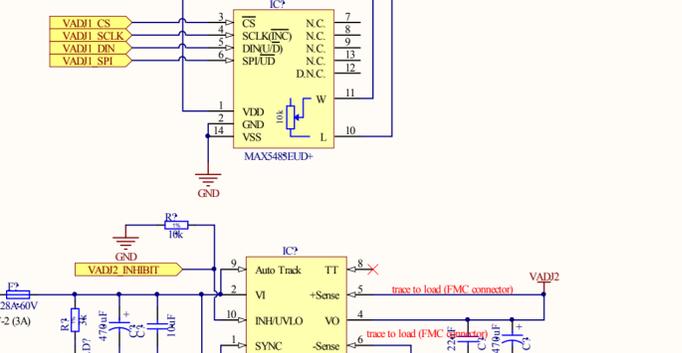
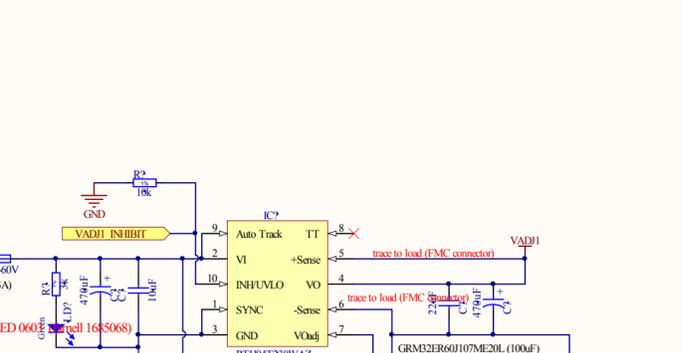
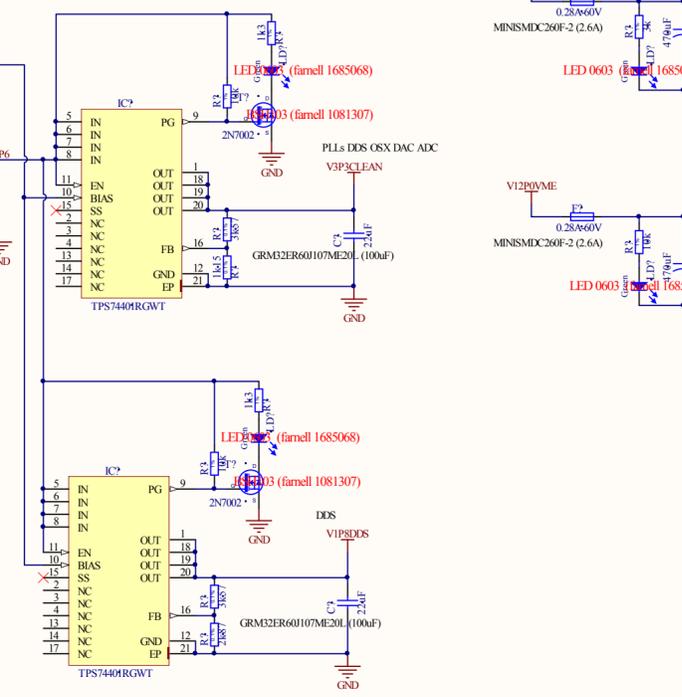
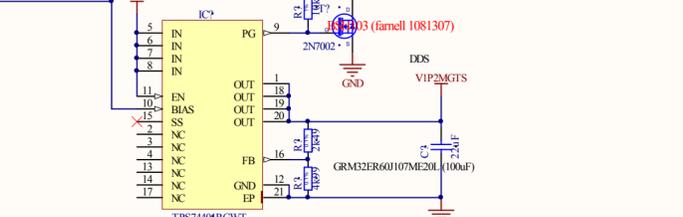
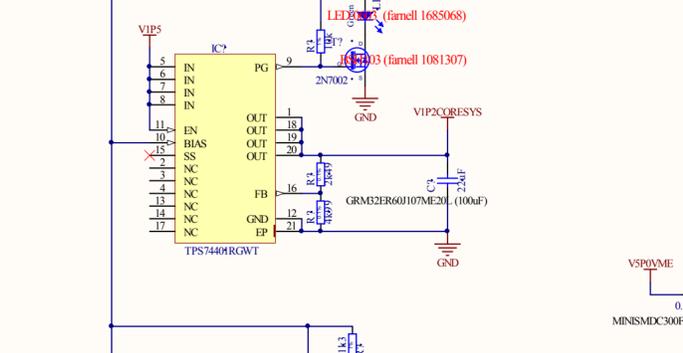
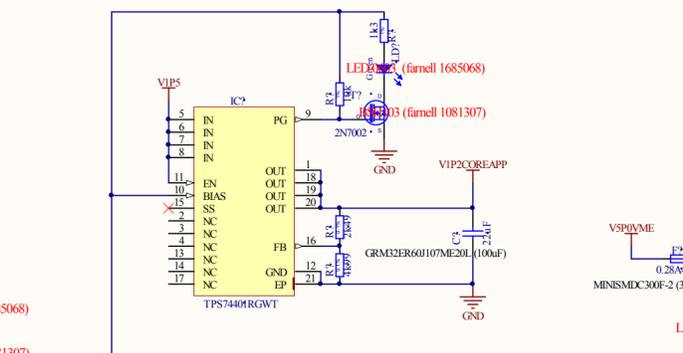
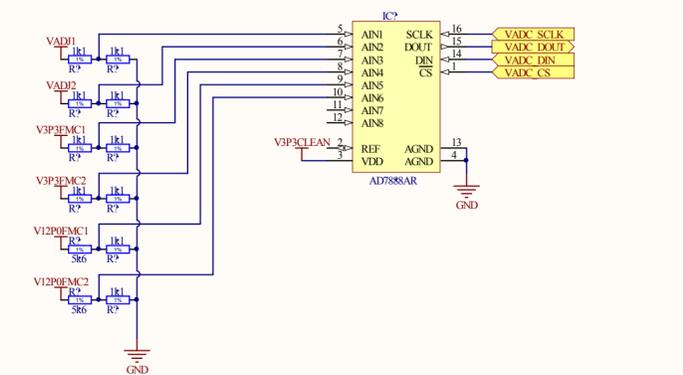
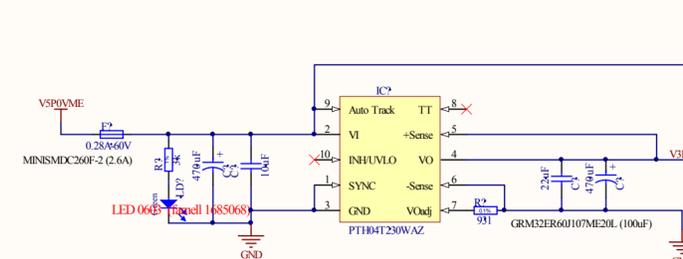
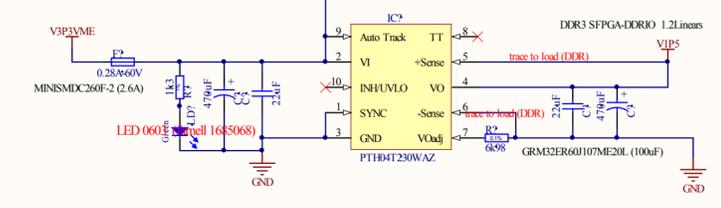
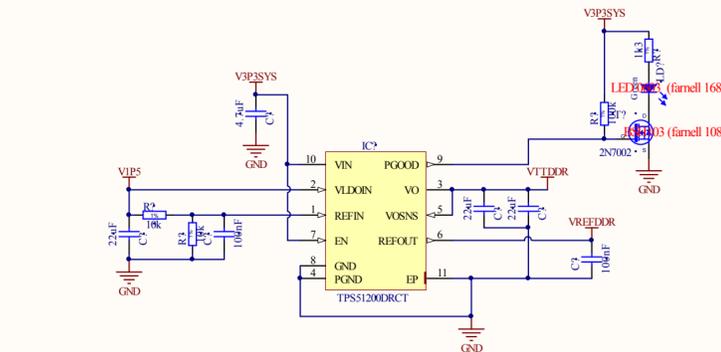
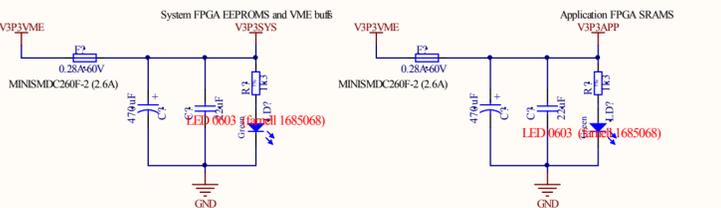
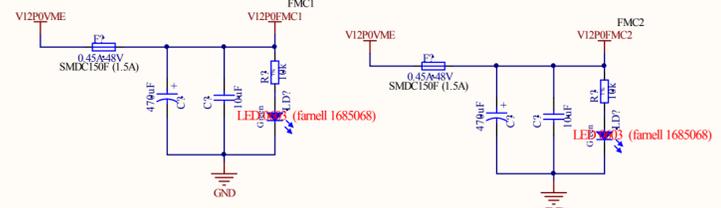
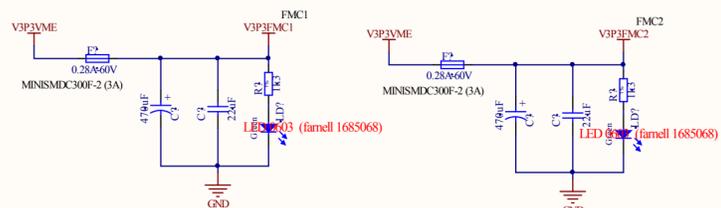
High Pin Count Rows



Project/Equipment		-	
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Designer	Andrea Boccardi	Drawn by	Andrea Boccardi
Check by	-	Last Mod	3/5/2010
File	FmcConnector.SchDoc	Print Date	3/11/2010 10:18:29 AM
Sheet	- of -	Size	A3
Rev	-	EDA-XXXXX-VX-X	



replace ALL the leds for ROHM - SML-311DTT86K - LED 0603 FAIBLE COURANT ORANGE (farnell 1685067)



Project/Equipment	-	Designer	Andrea Boccardi
Document	-	Drawn by	Andrea Boccardi
AB-BI	-	Check by	-
ERN	-	Last Mod.	3/11/2010
	-	File	PowerSupplies_SchDoc
	-	Print Date	3/11/2010 10:18:30 AM
	-	Sheet	- of -
	-	Rev	A2

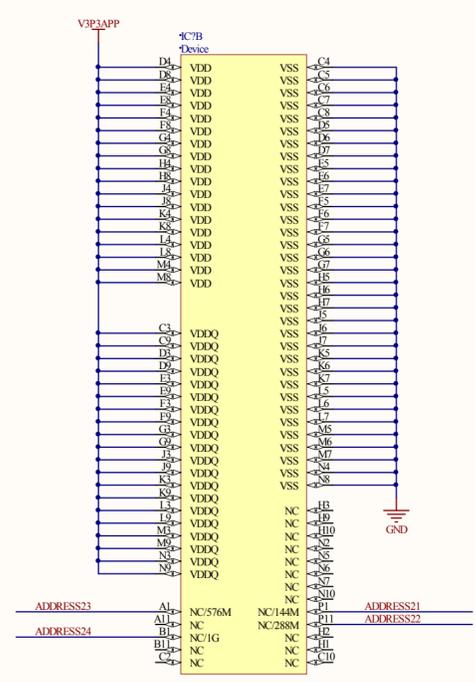
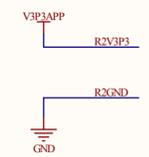
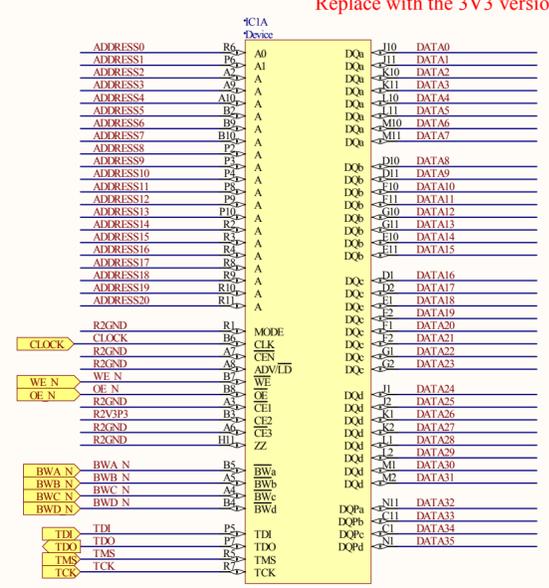
VME FMC Carrier Power Supplies

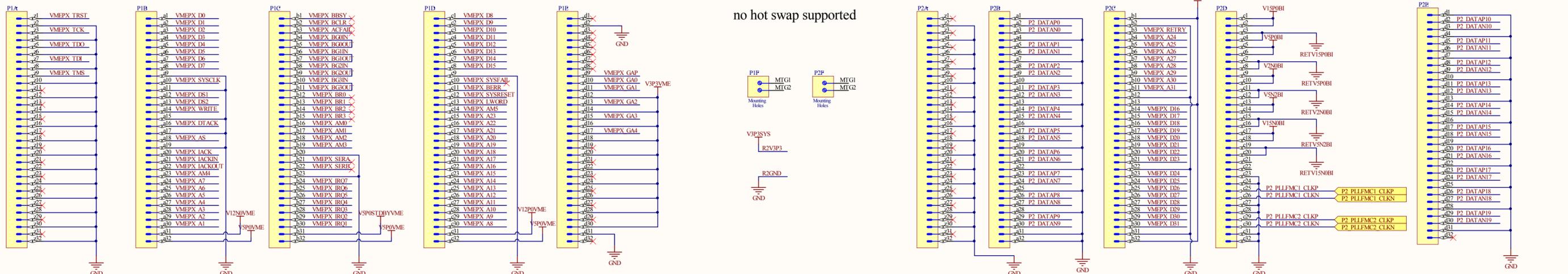
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EDA-XXXXX-VX-X

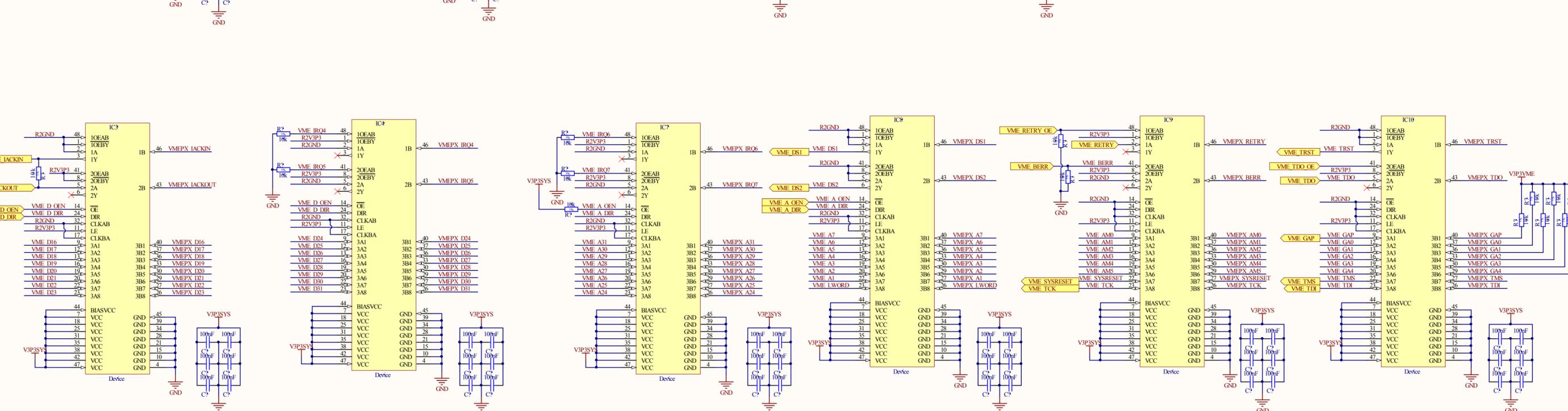
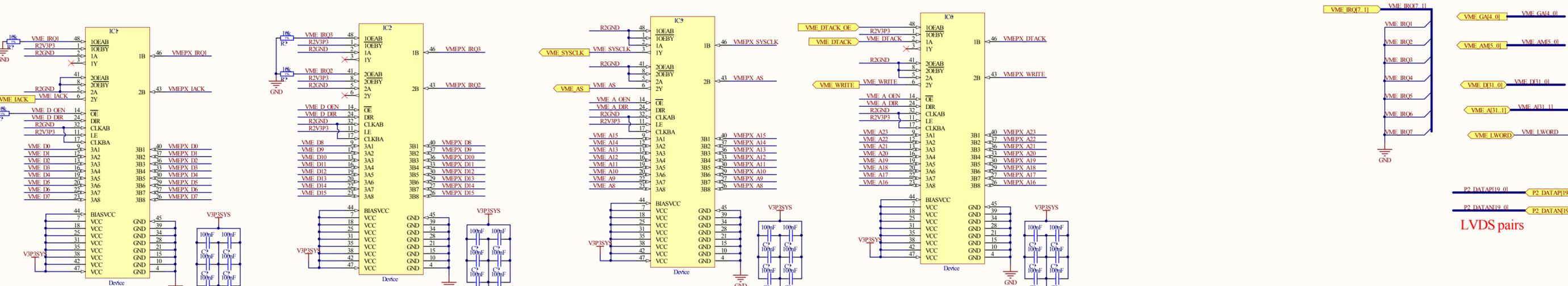
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Replace with the 3V3 version (same pinout)





no hot swap supported

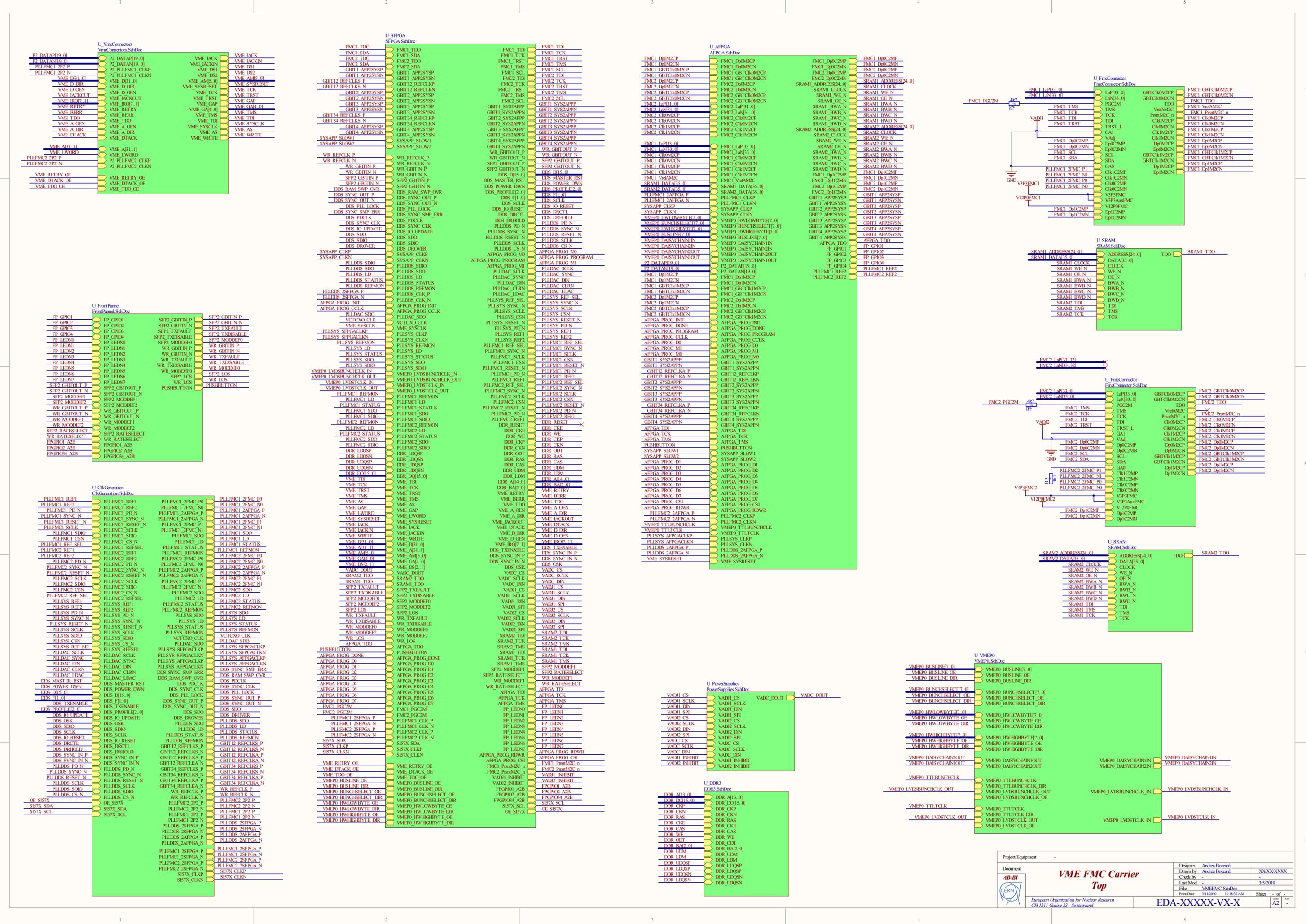


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Document	AB-BI	Designer	Andrea Boccardi
		Drawn by	Andrea Boccardi
		Check by	-
		Last Mod.	3/5/2010
		File	VmeConnectors_SchDoc
		Print Date	3/11/2010 10:18:31 AM
		Sheet	- of -
			A2

**VME FMC Carrier
VME P1 & P2**

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EDA-XXXX-VX-X



Project/Equipment		
Document		
AB-BI		
ERIN		
Designer	Andrea Boccardi	XX/XX/XXXX
Drawn by	Andrea Boccardi	XX/XX/XXXX
Check by	-	-
Last Mod	-	3/5/2010
File	VMEFMC_SchDoc	
Print Date	3/11/2010 10:18:22 AM	Sheet - of -
Printed		A2

VME FMC Carrier
Top

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EDA-XXXXX-VX-X

