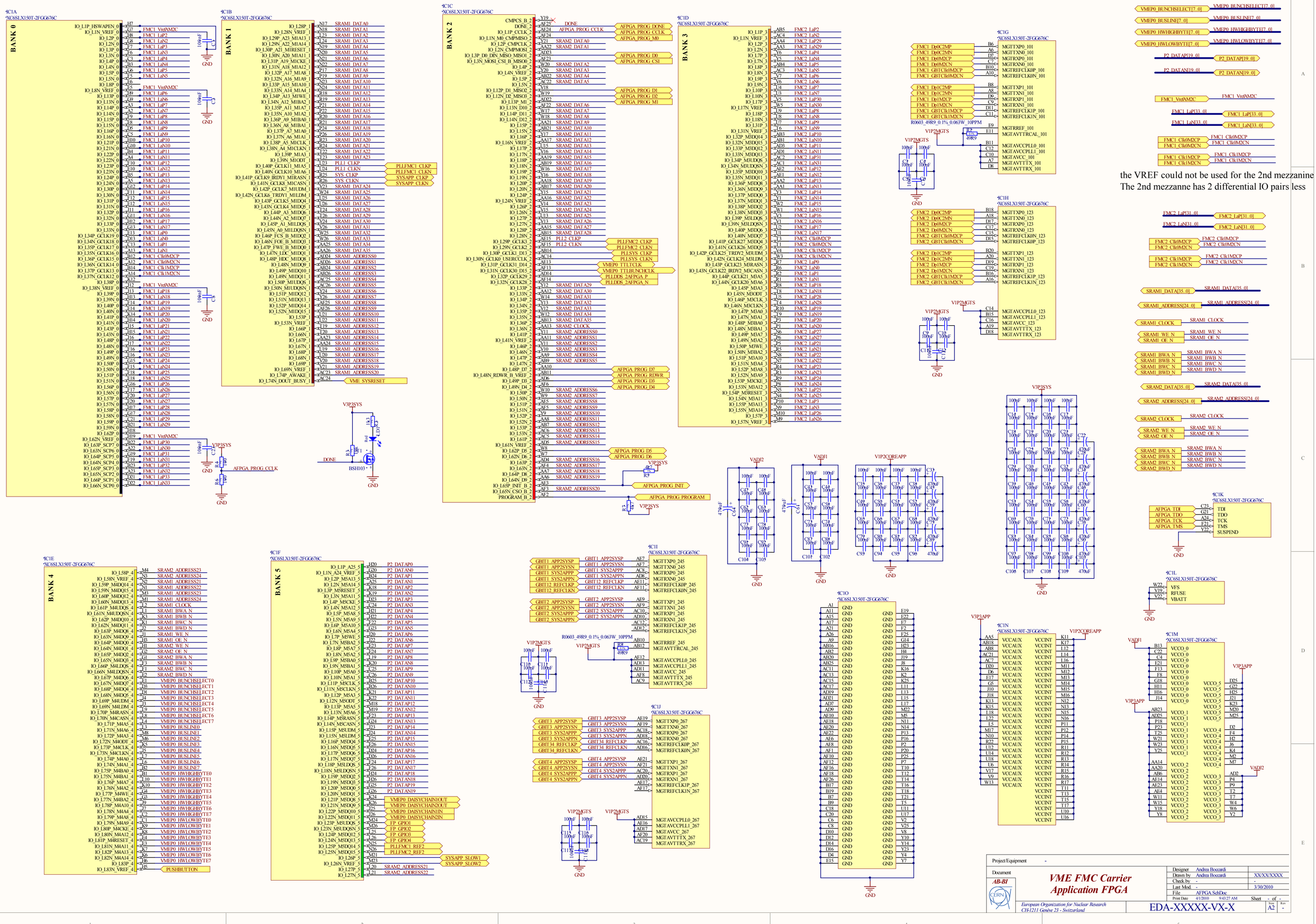

BANK 0
BANK 1
BANK 2
BANK 3
BANK 4
BANK 5
the VREF could not be used for the 2nd mezzanine
The 2nd mezzanne has 2 differential IO pairs less
Project/Equipment -
Document
AB-BI
VME FMC Carrier
Application FPGA
European Organization for Nuclear Research
CH-1211 Geneve 23 - Switzerland
EDA-XXXXX-VX-X
Designer Andrea Boccardi
Drawn by Andrea Boccardi
Check by -
Last Mod -
File AFPGA.SchDoc
Print Date 4/1/2010 9:43:27 AM
Sheet - of -
Size A2
Rev -

PhaseDetector @ 40MHz

PhaseDetector @ 40MHz

PhaseDetector @ 40MHz

as from page 79 of the AD9516 datasheet

Project/Equipment	-
Document	AB-BI
Designer	Andrea Boccardi
Drawn by	Andrea Boccardi
Check by	-
Last Mod	-
File	ClkGeneration.SchDoc
Print Date	4/1/2010 9:43:28 AM
Sheet	- of -
Size	A2
Rev	-

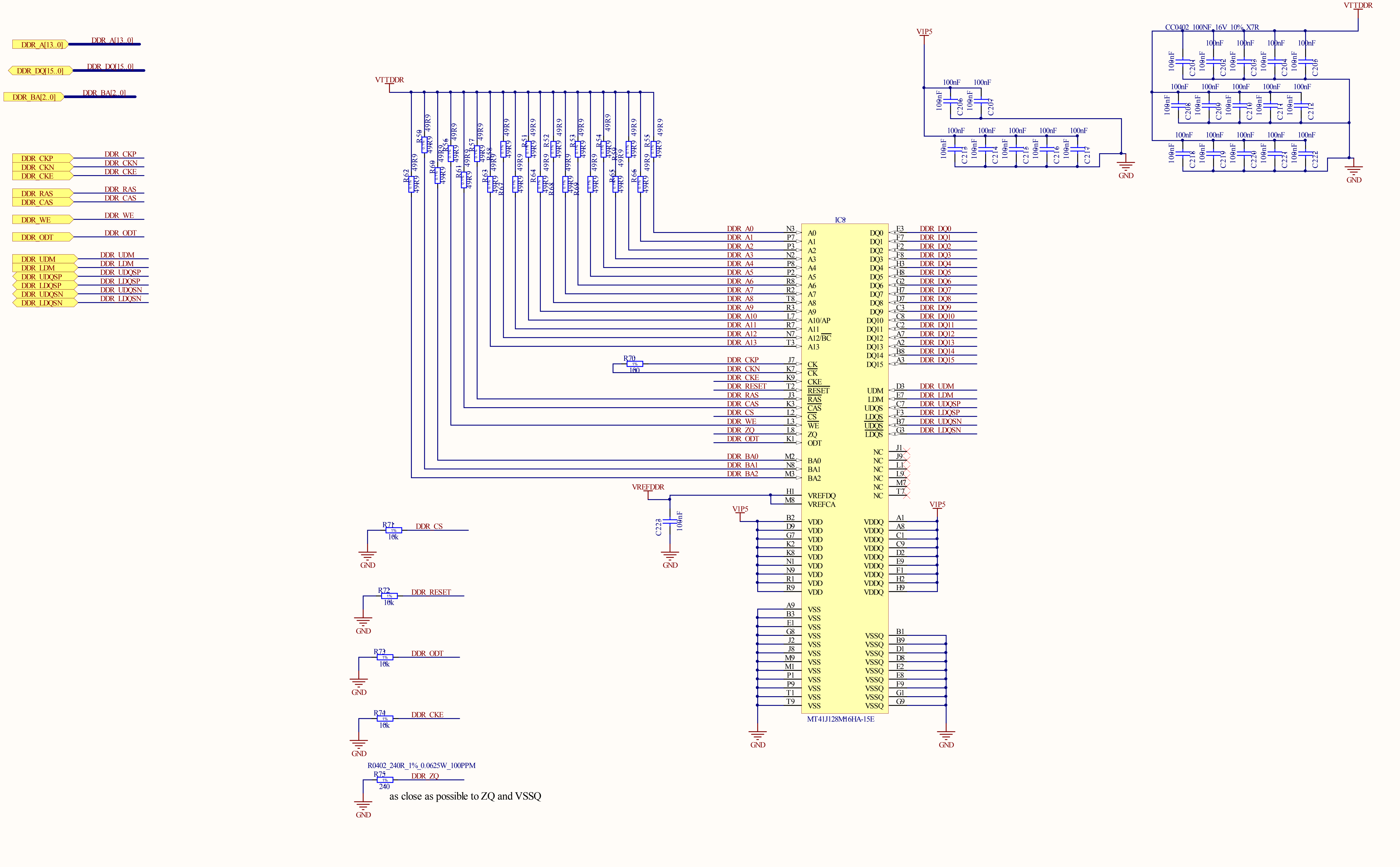
VME FMC Carrier Clocks

European Organization for Nuclear Research
CH-1211 Geneve 23 - Switzerland

EDA-XXXXX-VX-X

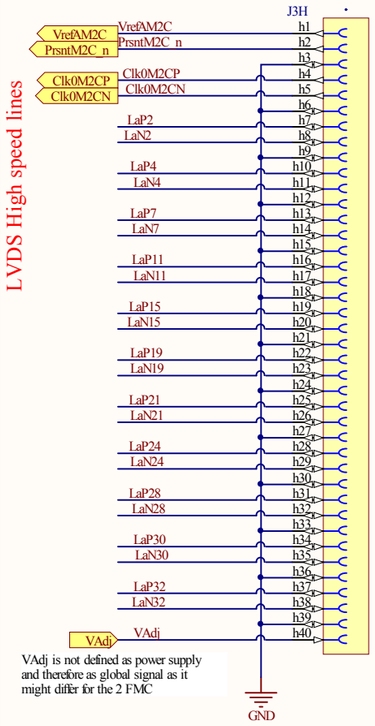
XX/XX/XXXX

3/30/2010

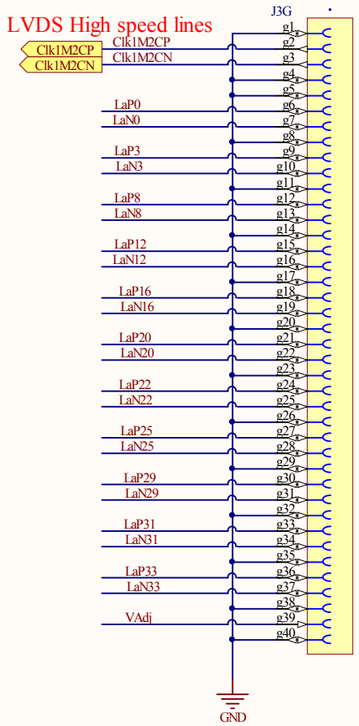


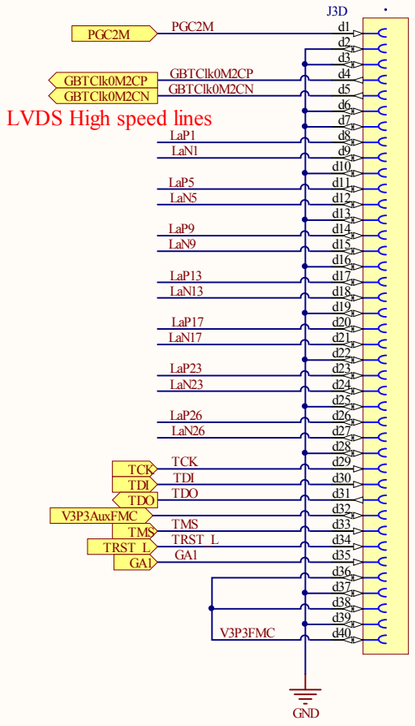
Project/Equipment	-
Document	VME FMC Carrier DDR3
	BE-BI-QP
	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland
Designer	Andrea Boccardi
Drawn by	Andrea Boccardi XX/XX/XXXX
Check.by	- -
Last Mod.	- 3/30/2010
File	DDR3.SchDoc
Print Date	4/1/2010 9:43:28 AM
Sheet	- of -
Size	A3
Rev	-
	EDA-XXXXX-VX-X

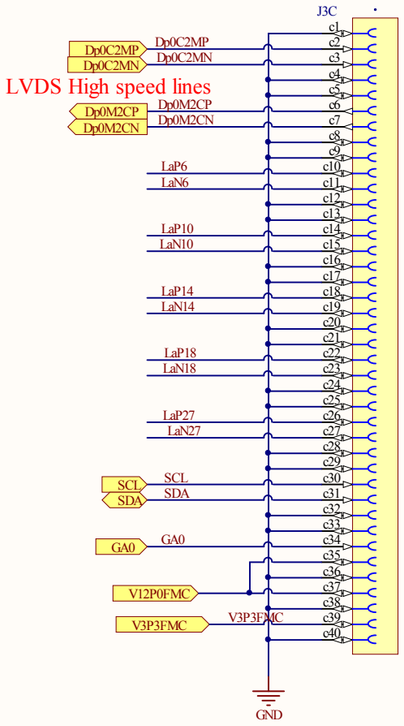
Low Pin Count Rows



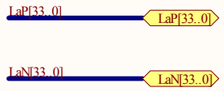
VAdj is not defined as power supply and therefore as global signal as it might differ for the 2 FMC



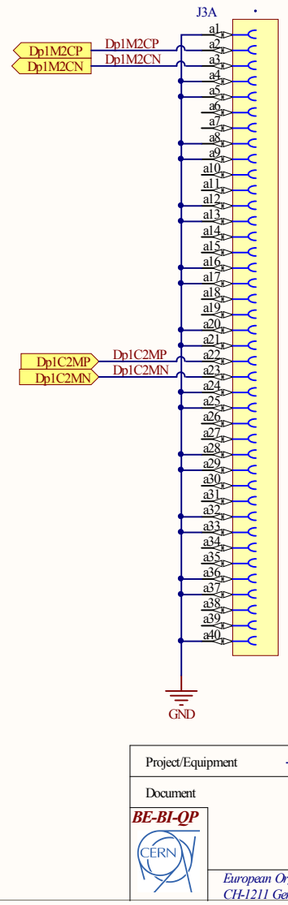




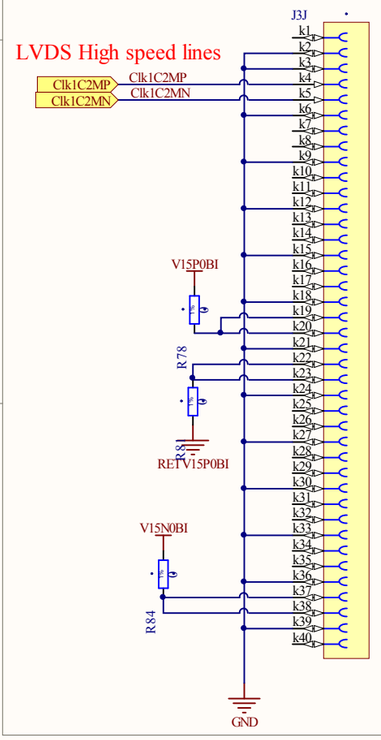
LaP and LaN are LVDS lines

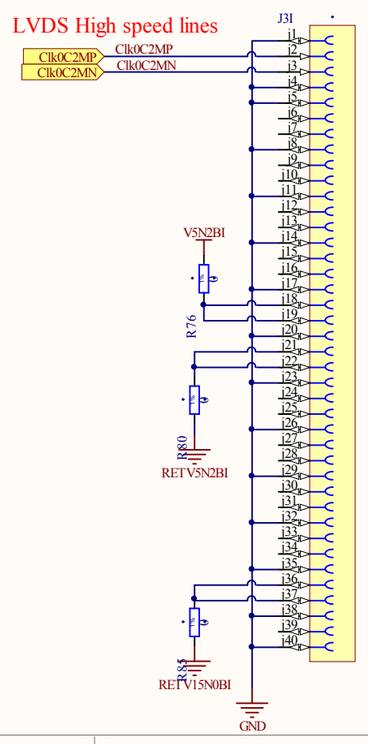


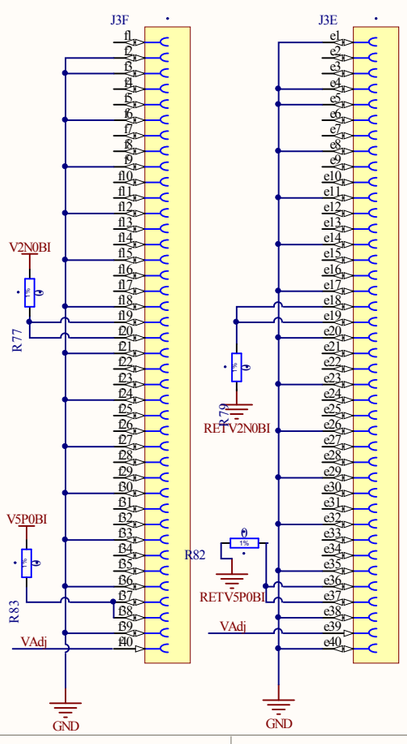
NB: the LVDS pairs must have a differential impedence of 100 ohm and be routed with no skew between the P and the N lines. The skew between the various La pairs should be kept as low as possible.

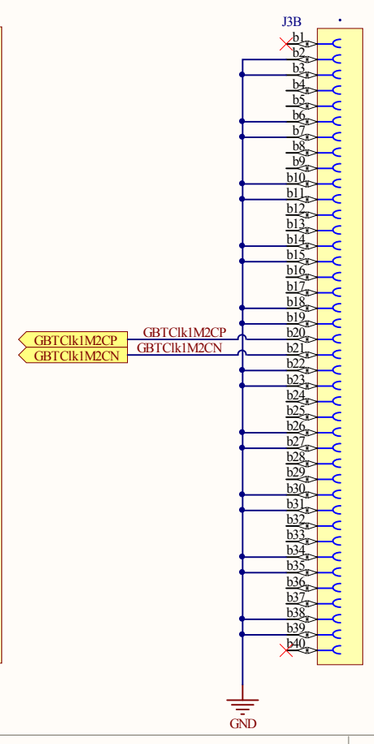


High Pin Count Rows

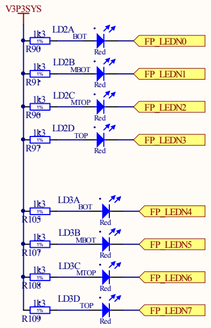


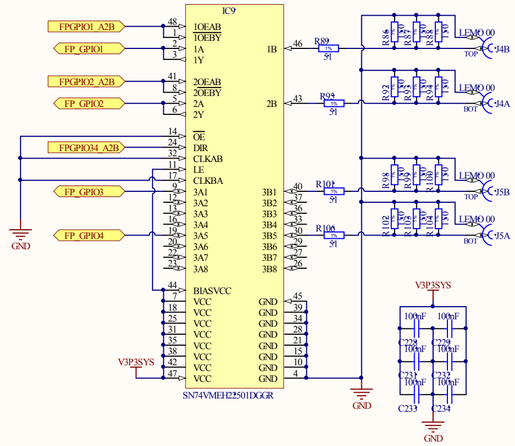


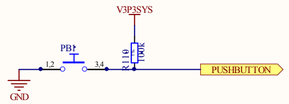


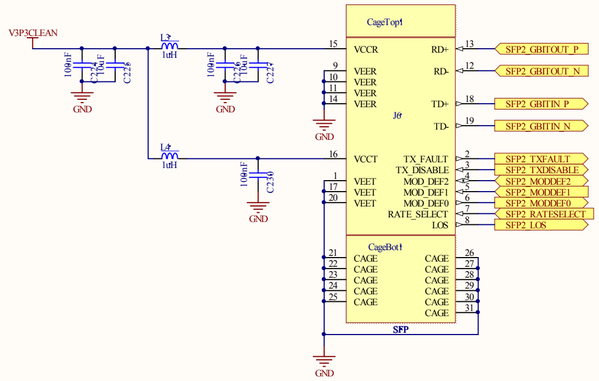


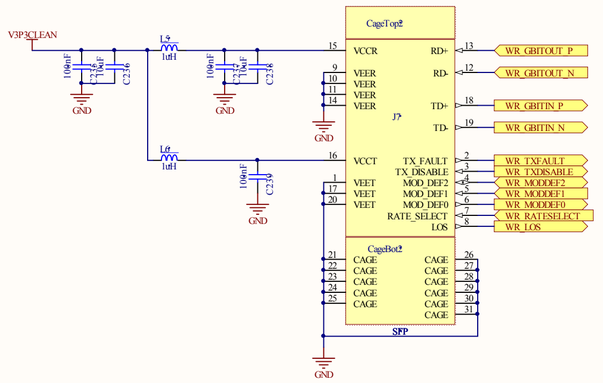
Project/Equipment	-		
Document	VME FMC Carrier FMC Connector	Designer	Andrea Boccardi
		Drawn by	Andrea Boccardi XX/XX/XXXX
		Check by	- -
		Last Mod.	- 3/30/2010
		File	FmcConnector.SchDoc
		Print Date	4/1/2010 9:43:28 AM Sheet - of -
BE-BI-QP	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3 Rev -



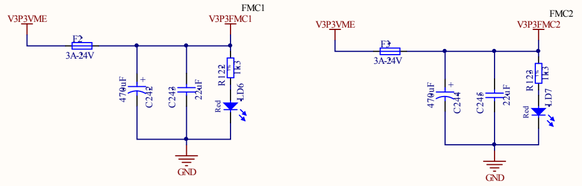


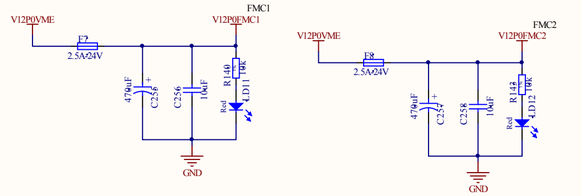


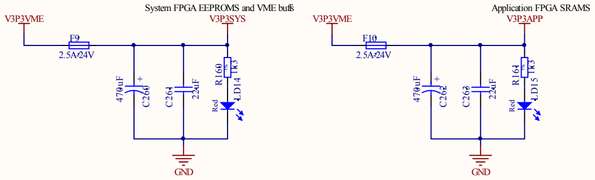


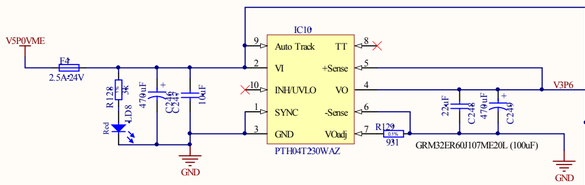


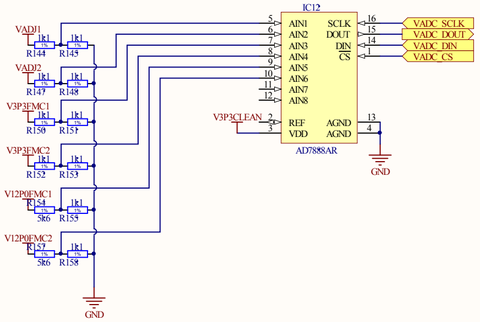
Project/Equipment	-		
Document	*VME FMC Carrier Front Panel*	Designer: Andrea Boccardi	
AB-BI		Drawn by: Andrea Boccardi	XXXXXXXX
		Check by: -	-
		Last Mod: -	3/30/2010
		File: FrontPannel.SchDoc	
		Print Date: 4/1/2010 9:43:28 AM	Sheet - of -
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size: A2	Rev: -

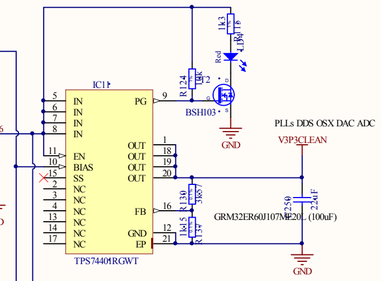


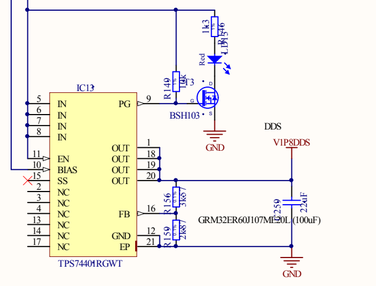


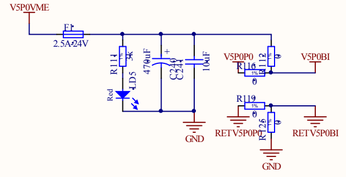


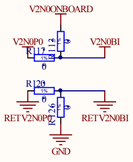


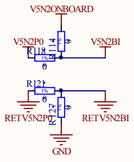


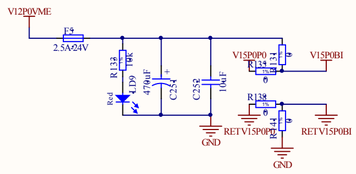


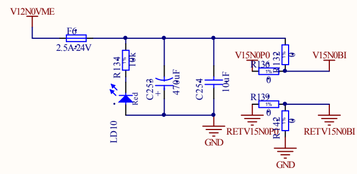


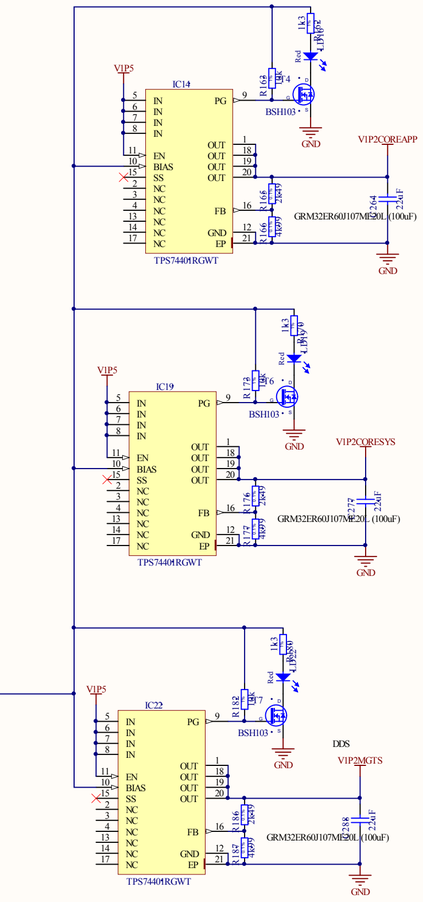


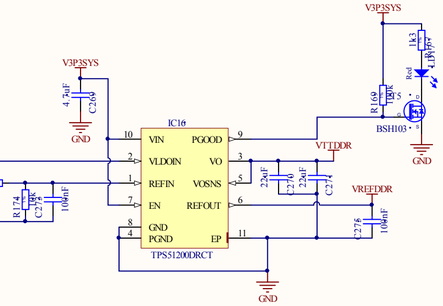


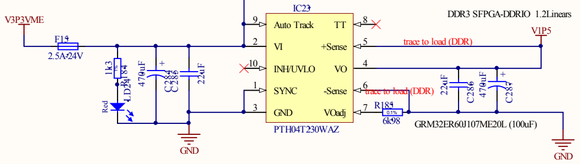


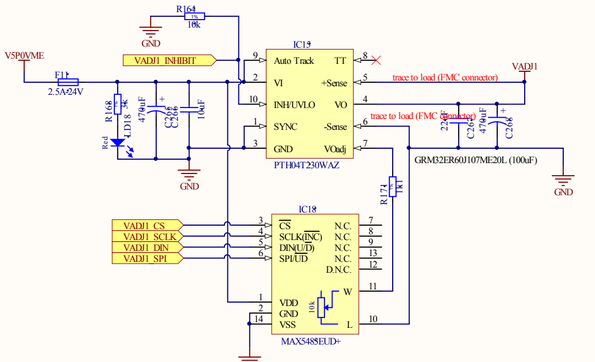


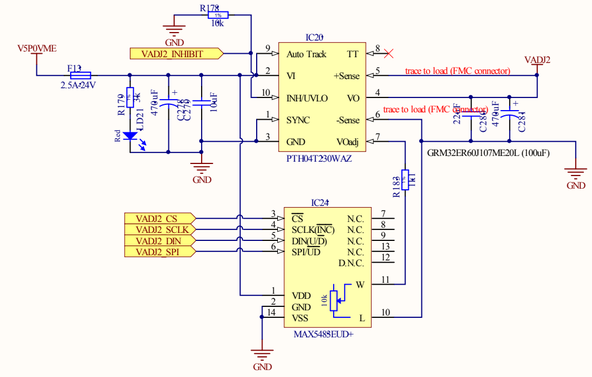


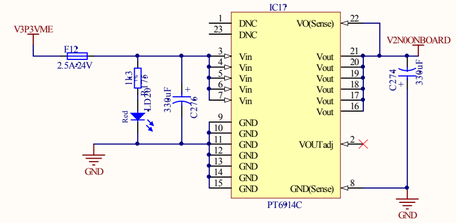


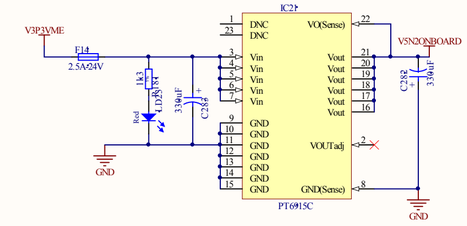












Project/Equipment	-		
Document	*VME FMC Carrier Power Supplies*	Designer Andrea Boccardi	
AB-BI		Drawn by Andrea Boccardi	XX/XX/XXXX
		Check by -	-
		Last Mod. -	4/1/2010
		File PowerSupplies.SchDoc	
		Print Date 4/1/2010 9:43:29 AM	Sheet - of -
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A2	Rev -

Add some TP (just vias) if there are spare pins

change package for the vertical one
FCI 10074141-001LF

Project/Equipment	-		
Document	VME FMC Carrier System FPGA	Designer	Andrea Boccardi
		Drawn by	Andrea Boccardi XX/XX/XXXX
		Check by	- -
		Last Mod.	- 3/30/2010
		File	SFPGA.SchDoc
		Print Date	4/1/2010 9:43:29 AM Sheet - of -
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size	A2 Rev -

ADDRESS[24..0] ADDRESS[24..0]

DATA[35..0] DATA[35..0]

Replace with the 3V3 version (same pinout)

*IC29A
*CY7C1470BV33-167BZXC

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ADDRESS1	P6	A1	DQa	J11	DATA1
ADDRESS2	A2	A	DQa	K10	DATA2
ADDRESS3	A9	A	DQa	K11	DATA3
ADDRESS4	A10	A	DQa	L10	DATA4
ADDRESS5	B2	A	DQa	L11	DATA5
ADDRESS6	B9	A	DQa	M10	DATA6
ADDRESS7	B10	A	DQa	M11	DATA7
ADDRESS8	P2	A			
ADDRESS9	P3	A		D10	DATA8
ADDRESS10	P4	A	DQb	D11	DATA9
ADDRESS11	P5	A	DQb	E10	DATA10
ADDRESS12	P9	A	DQb	E11	DATA11
ADDRESS13	P10	A	DQb	G10	DATA12
ADDRESS14	R2	A	DQb	G11	DATA13
ADDRESS15	R3	A	DQb	H10	DATA14
ADDRESS16	R4	A	DQb	H11	DATA15
ADDRESS17	R5	A			
ADDRESS18	R9	A		D1	DATA16
ADDRESS19	R10	A	DQc	D2	DATA17
ADDRESS20	R11	A	DQc	E1	DATA18
			DQc	E2	DATA19
R2GND	R1	MODE	DQc	F1	DATA20
CLOCK	B6	CLK	DQc	F2	DATA21
R2GND	A7	CEN	DQc	G1	DATA22
R2GND	A6	ADV/LD	DQc	G2	DATA23
WE_N	B7	WE			
OE_N	B8	OE		J1	DATA24
R2GND	A5	CE1	DQd	J2	DATA25
R2V3P3	B3	CE2	DQd	K1	DATA26
R2GND	A8	CE3	DQd	K2	DATA27
R2GND	H11	ZZ	DQd	L1	DATA28
			DQd	L2	DATA29
BWA_N	B5	BWa	DQd	M1	DATA30
BWB_N	A3	BWb	DQd	M2	DATA31
BWC_N	A4	BWc			
BWD_N	B4	BWd		N1	DATA32
			DQPa	C11	DATA33
TDI	P5	TDI	DQPb	C1	DATA34
TDO	P7	TDO	DQPc	N1	DATA35
TMS	R7	TMS	DQPd		
TCK	R8	TCK			

V3P3APP

R2V3P3

R2GND

GND

*IC29B
*CY7C1470BV33-167BZXC

D4	VDD	VSS	C4		
D5	VDD	VSS	C5		
E4	VDD	VSS	C6		
E5	VDD	VSS	C7		
F4	VDD	VSS	C8		
F5	VDD	VSS	D5		
G4	VDD	VSS	D6		
G5	VDD	VSS	D7		
H4	VDD	VSS	E5		
H5	VDD	VSS	E6		
J4	VDD	VSS	E7		
J5	VDD	VSS	F5		
K4	VDD	VSS	F6		
K5	VDD	VSS	F7		
L4	VDD	VSS	G5		
L5	VDD	VSS	G6		
M4	VDD	VSS	G7		
M5	VDD	VSS	H5		
		VSS	H6		
C3	VDDQ	VSS	H7		
C9	VDDQ	VSS	J5		
D3	VDDQ	VSS	J6		
D9	VDDQ	VSS	J7		
E3	VDDQ	VSS	K5		
E9	VDDQ	VSS	K6		
F3	VDDQ	VSS	L6		
F9	VDDQ	VSS	L7		
G3	VDDQ	VSS	M5		
G9	VDDQ	VSS	M6		
J3	VDDQ	VSS	M7		
J9	VDDQ	VSS	N4		
K3	VDDQ	VSS	N8		
K9	VDDQ				
L3	VDDQ	NC	H1		
L9	VDDQ	NC	H9		
M3	VDDQ	NC	H10		
M9	VDDQ	NC	J9		
N3	VDDQ	NC	K7		
N9	VDDQ	NC	K8		
		NC	L8		
A1	NC/576M	NC/144M	P11	ADDRESS21	
A11	NC	NC/288M	L9	ADDRESS22	
B1	NC/1G	NC	H8		
B11	NC	NC	H11		
C2	NC	NC	L10		
	NC	NC			

ADDRESS23

ADDRESS24

GND

V3P3APP

C400	100nF	C401	100nF	C402	100nF	C403	100nF	C404	100nF
C405	100nF	C406	100nF	C407	100nF	C408	100nF	C409	100nF

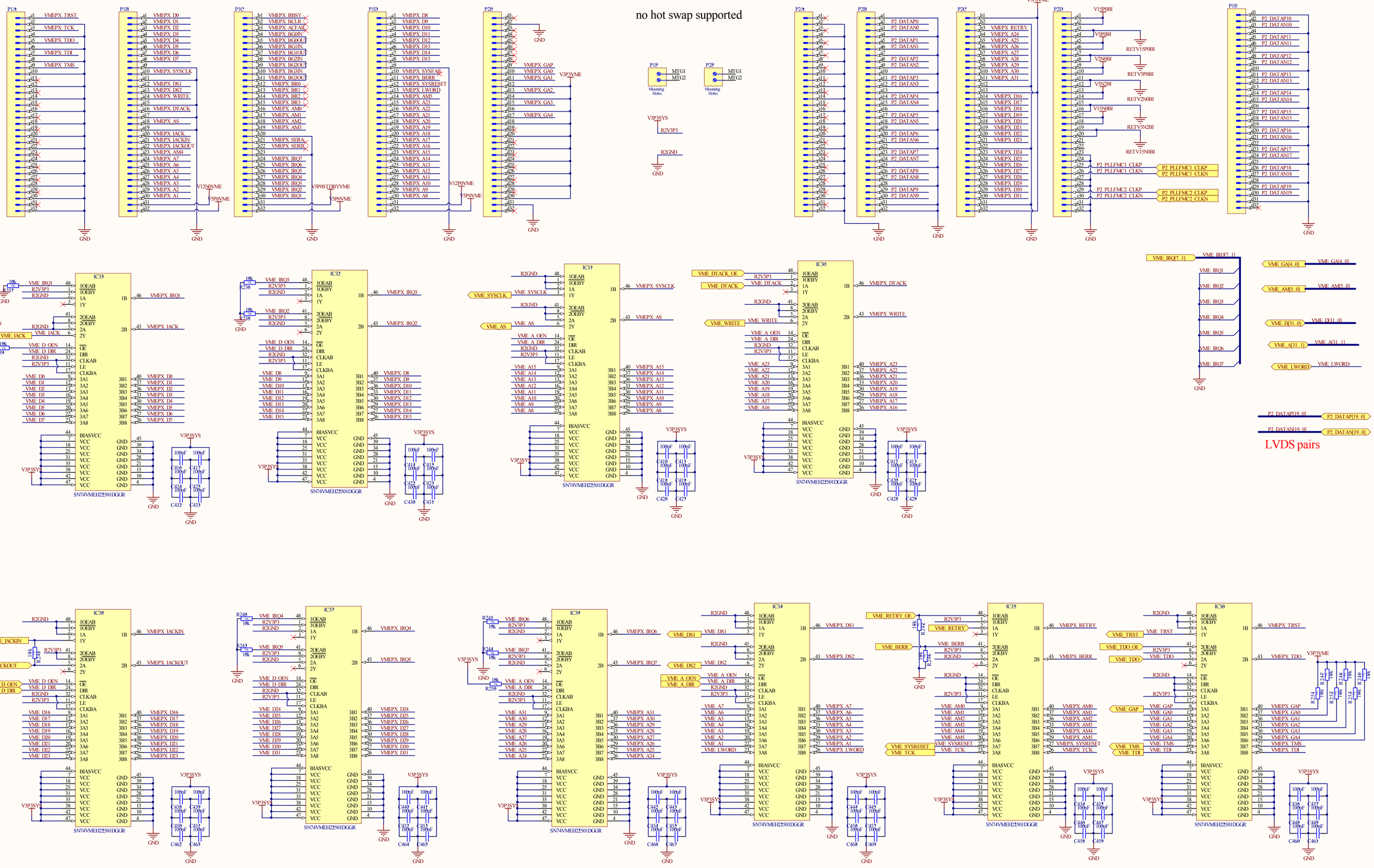
GND

Project/Equipment	-		
Document	*VME FMC Carrier* *SRAM*	Designer	Andrea Boccardi
		Drawn by	Andrea Boccardi
		Check by	-
		Last Mod.	-
		File	SRAM.SchDoc
		Print Date	4/1/2010 9:43:30 AM
		Sheet	- of -
European Organization for Nuclear Research *CH-1211 Genève 23 - Switzerland*	EDA-XXXXX-VX-X	Size	A2
		Rev	-

AB-BI

XX/XX/XXXX

3/30/2010


P1A
P1B
P1C
P1D
P2F
VMEPX_TRST
VMEPX_TCK
VMEPX_TDO
VMEPX_TDI
VMEPX_TMS
VMEPX_SYSCLK
VMEPX_IACKIN
VMEPX_IACKOUT
VMEPX_AS
VMEPX_DTACK
VMEPX_WRITE
VMEPX_IRQ1
VMEPX_IRQ2
VMEPX_IRQ3
VMEPX_IRQ4
VMEPX_IRQ5
VMEPX_IRQ6
VMEPX_IRQ7
VMEPX_SYSFAIL
VMEPX_BERR
VMEPX_SYSRESET
VMEPX_LWORD
VMEPX_AM5
VMEPX_A24
VMEPX_A25
VMEPX_A26
VMEPX_A27
VMEPX_A28
VMEPX_A29
VMEPX_A30
VMEPX_A31
VMEPX_D16
VMEPX_D17
VMEPX_D18
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VMEPX_D29
VMEPX_D30
VMEPX_D31
VMEPX_GAP
VMEPX_GA0
VMEPX_GA1
VMEPX_GA2
VMEPX_GA3
VMEPX_GA4
VMEPX_AM0
VMEPX_AM1
VMEPX_AM2
VMEPX_AM3
VMEPX_AM4
VMEPX_A7
VMEPX_A6
VMEPX_A5
VMEPX_A4
VMEPX_A3
VMEPX_A2
VMEPX_A1
VMEPX_A0
VMEPX_D0
VMEPX_D1
VMEPX_D2
VMEPX_D3
VMEPX_D4
VMEPX_D5
VMEPX_D6
VMEPX_D7
VMEPX_D8
VMEPX_D9
VMEPX_D10
VMEPX_D11
VMEPX_D12
VMEPX_D13
VMEPX_D14
VMEPX_D15
VMEPX_A15
VMEPX_A14
VMEPX_A13
VMEPX_A12
VMEPX_A11
VMEPX_A10
VMEPX_A9
VMEPX_A8
V12N0VME
V5P0STDBYVME
V5P0VME
V3P3VME
V5P0VME
V5P0BI
V2N0BI
V5N2BI
V15N0BI
RETV15P0BI
RETV2P5P0BI
RETV2N0BI
RETV5N2BI
RETV15N0BI
P2_PLLFMC1_CLKP
P2_PLLFMC1_CLKN
P2_PLLFMC2_CLKP
P2_PLLFMC2_CLKN
P2_DATAP0
P2_DATAN0
P2_DATAP1
P2_DATAN1
P2_DATAP2
P2_DATAN2
P2_DATAP3
P2_DATAN3
P2_DATAP4
P2_DATAN4
P2_DATAP5
P2_DATAN5
P2_DATAP6
P2_DATAN6
P2_DATAP7
P2_DATAN7
P2_DATAP8
P2_DATAN8
P2_DATAP9
P2_DATAN9
P2_DATAP10
P2_DATAN10
P2_DATAP11
P2_DATAN11
P2_DATAP12
P2_DATAN12
P2_DATAP13
P2_DATAN13
P2_DATAP14
P2_DATAN14
P2_DATAP15
P2_DATAN15
P2_DATAP16
P2_DATAN16
P2_DATAP17
P2_DATAN17
P2_DATAP18
P2_DATAN18
P2_DATAP19
P2_DATAN19
no hot swap supported
MTG1
MTG2
Mounting Holes
V3P3SYS
R2V3P3
R2GND
GND
IC33
IC32
IC31
IC30
SN74VMEH22501DGGR
VME_IRQ[7..1]
VME_GA[4..0]
VME_AM[5..0]
VME_D[31..0]
VME_A[31..1]
LVDS pairs
IC38
IC37
IC39
IC34
IC35
IC36
VME_IACKOUT
VME_D_OEN
VME_D_DIR
VME_RETRY_OE
VME_RETRY
VME_TRST
VME_TDO_OE
VME_TDO
VME_GAP
VME_TMS
VME_TDI
VME_SYSRESET
VME_TCK
VME_BERR
VME_DS1
VME_DS2
VME_A_OEN
VME_A_DIR
Project/Equipment -
Document
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VME FMC Carrier
VME P1 & P2
Designer Andrea Boccardi
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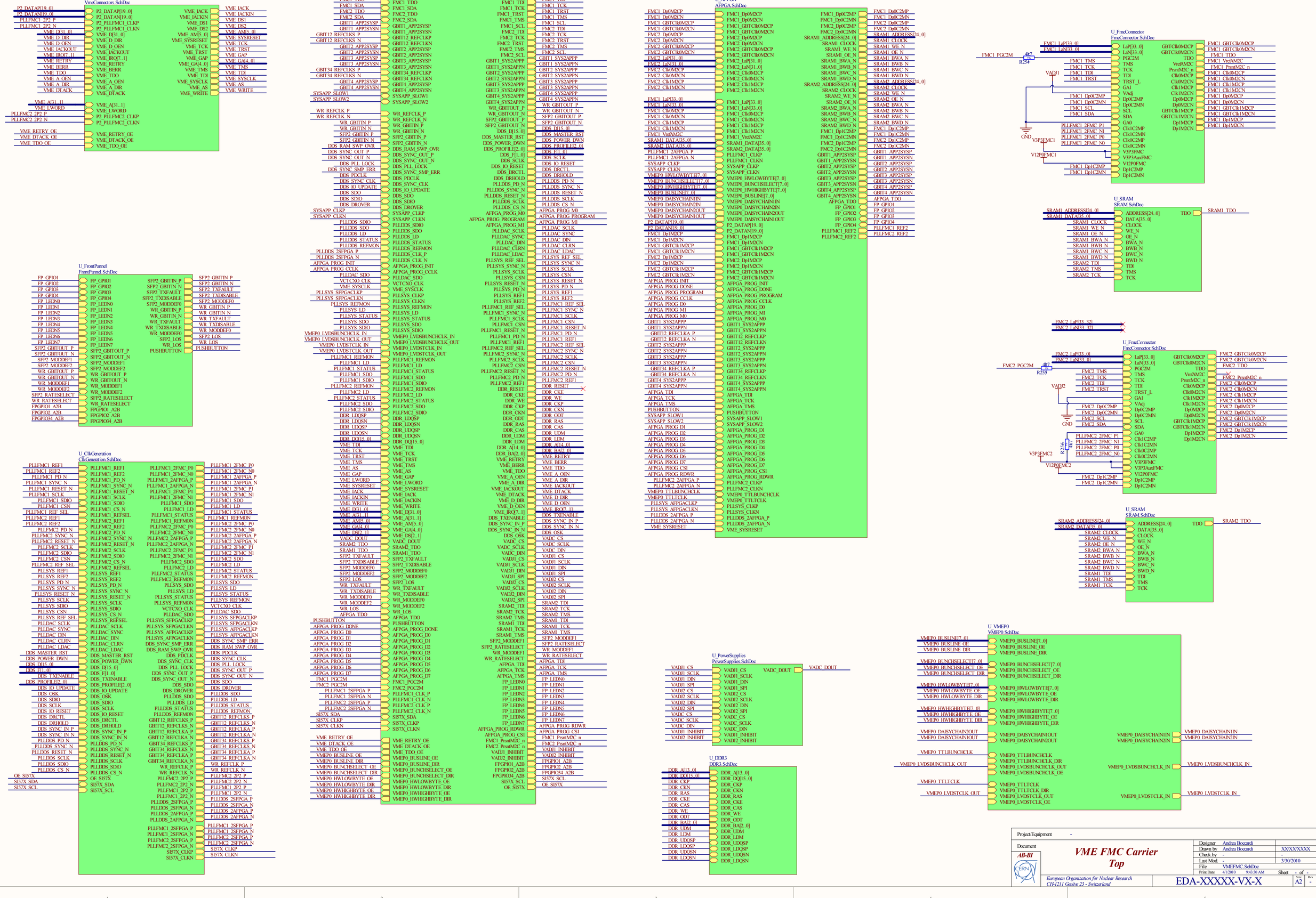
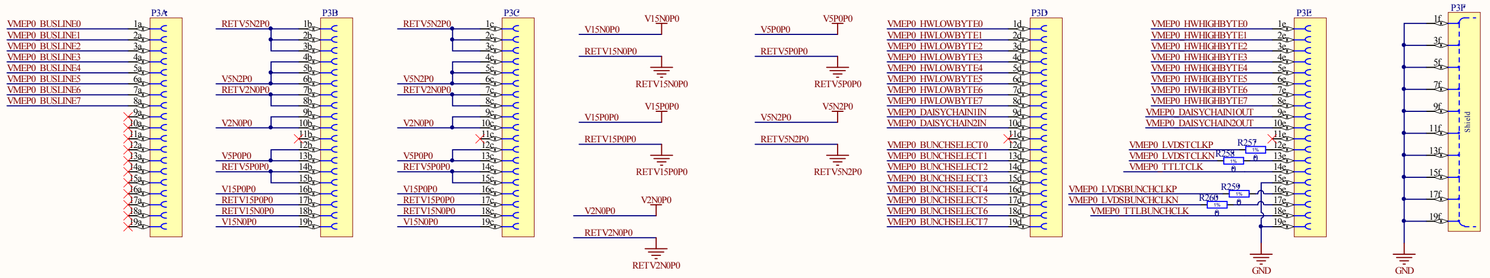
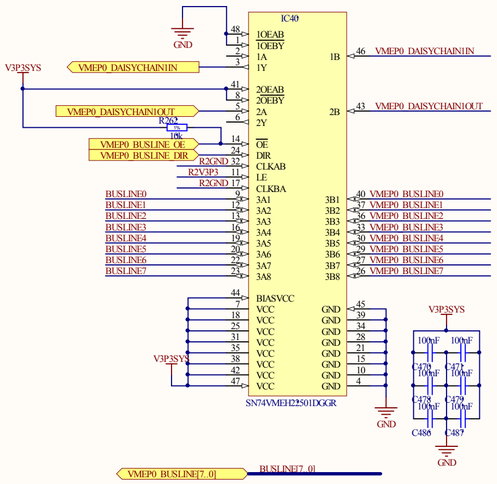
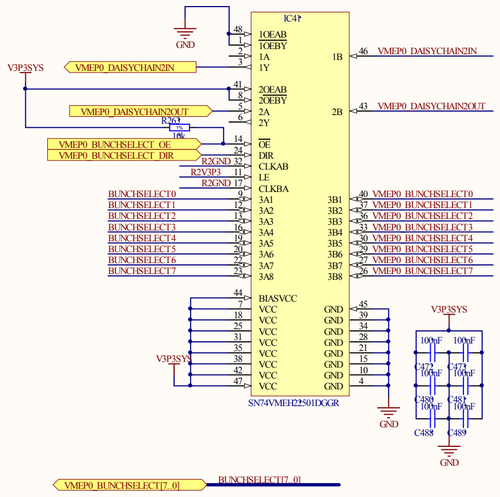
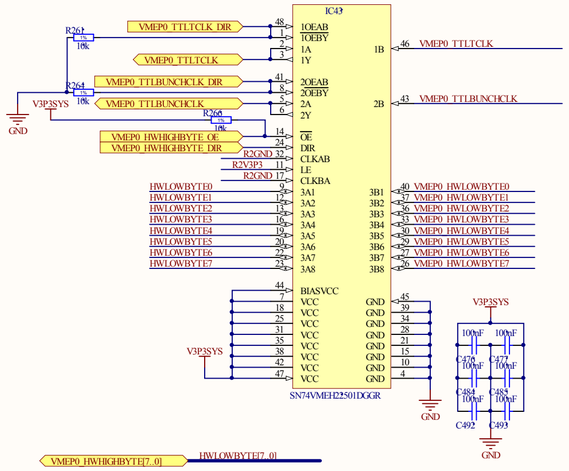
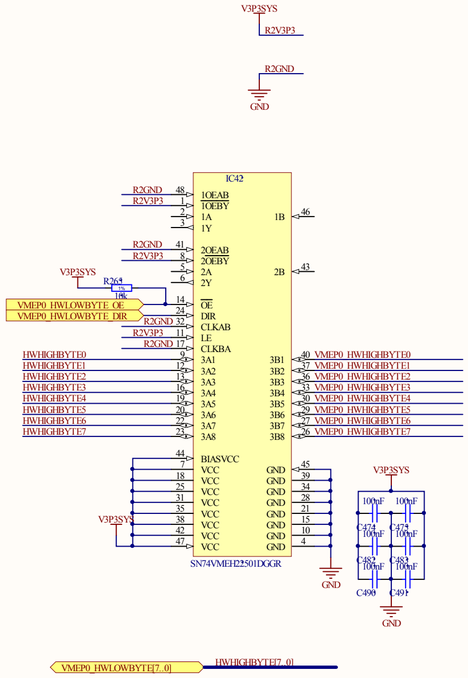

U_VmeConnectors
VmeConnectors.SchDoc
P2_DATAP[19..0]
P2_DATAN[19..0]
PLLFMC1_2P2_P
PLLFMC1_2P2_N
VME_D[31..0]
VME_D_DIR
VME_D_OEN
VME_IACKOUT
VME_IRQ7_1[1..7]
VME_RETRY
VME_BERR
VME_TDO
VME_A_OEN
VME_A_DIR
VME_DTACK
VME_A[31..1]
VME_LWORD
PLLFMC2_2P2_P
PLLFMC2_2P2_N
VME_RETRY_OE
VME_DTACK_OE
VME_TDO_OE
VME_IACK
VME_IACKIN
VME_DS1
VME_DS2
VME_AM[5..0]
VME_SYSRESET
VME_TCK
VME_TRST
VME_GAP
VME_GA[4..0]
VME_TMS
VME_TDI
VME_SYSCLK
VME_AS
VME_WRITE
U_SFPGA
SFPGA.SchDoc
FMC1_TDO
FMC1_SDA
FMC2_TDO
FMC2_SDA
GBIT1_APP2SYSP
GBIT1_APP2SYSN
GBIT12_REFCLKP
GBIT12_REFCLKN
GBIT2_APP2SYSP
GBIT2_APP2SYSN
GBIT3_APP2SYSP
GBIT3_APP2SYSN
GBIT34_REFCLKP
GBIT34_REFCLKN
GBIT4_APP2SYSP
GBIT4_APP2SYSN
SYSAPP_SLOW1
SYSAPP_SLOW2
WR_REFCLK_P
WR_REFCLK_N
WR_GBITIN_P
WR_GBITIN_N
SFP2_GBITIN_P
SFP2_GBITIN_N
DDS_RAM_SWP_OVR
DDS_SYNC_OUT_P
DDS_SYNC_OUT_N
DDS_PLL_LOCK
DDS_SYNC_SMP_ERR
DDS_PDCLK
DDS_SYNC_CLK
DDS_IO_UPDATE
DDS_SDO
DDS_SDIO
DDS_DROVER
SYSAPP_CLKP
SYSAPP_CLKN
PLLDDS_SDIO
PLLDDS_SDO
PLLDDS_LD
PLLDDS_STATUS
PLLDDS_REFMON
PLLDDS_2SFPGA_P
PLLDDS_2SFPGA_N
AFPGA_PROG_INIT
AFPGA_PROG_CCLK
PLLDAC_SDO
VCTCXO_CLK
VME_SYSCLK
PLLSYS_SFPGACLKP
PLLSYS_SFPGACLKN
PLLSYS_AFPGACLKP
PLLSYS_AFPGACLKN
PLLSYS_CLKP
PLLSYS_CLKN
PLLSYS_REFMON
PLLSYS_LD
PLLSYS_SDO
PLLSYS_SDIO
VME_RETRY_OE
VME_DTACK_OE
VME_TDO_OE
VMEP0_BUSLINE_OE
VMEP0_BUSLINE_DIR
VMEP0_BUNCHSELECT_OE
VMEP0_BUNCHSELECT_DIR
VMEP0_HWLOWBYTE_OE
VMEP0_HWLOWBYTE_DIR
VMEP0_HWHIGHBYTE_OE
VMEP0_HWHIGHBYTE_DIR
VMEP0_LVDSBUNCHCLK_IN
VMEP0_LVDSBUNCHCLK_OUT
VMEP0_LVDSTCLK_IN
VMEP0_LVDSTCLK_OUT
FMC1_TDI
FMC1_TCK
FMC1_TRST
FMC1_TMS
FMC1_SCL
FMC2_TDI
FMC2_TCK
FMC2_TRST
FMC2_TMS
FMC2_SCL
GBIT1_SYS2APPP
GBIT1_SYS2APPN
GBIT2_SYS2APPP
GBIT2_SYS2APPN
GBIT3_SYS2APPP
GBIT3_SYS2APPN
GBIT4_SYS2APPP
GBIT4_SYS2APPN
WR_GBITOUT_P
WR_GBITOUT_N
SFP2_GBITOUT_P
SFP2_GBITOUT_N
DDS_D[15..0]
DDS_MASTER_RST
DDS_POWER_DWN
DDS_PROFILE[2..0]
DDS_F[1..0]
DDS_SCLK
DDS_IO_RESET
DDS_DRCTL
DDS_DRHOLD
PLLDDS_PD_N
PLLDDS_SYNC_N
PLLDDS_RESET_N
PLLDDS_SCLK
PLLDDS_CS_N
AFPGA_PROG_M0
AFPGA_PROG_PROGRAM
AFPGA_PROG_M1
PLLDAC_SCLK
PLLDAC_SYNC
PLLDAC_DIN
PLLDAC_CLRN
PLLDAC_LDAC
PLLSYS_REF_SEL
PLLSYS_SYNC_N
PLLSYS_SCLK
PLLSYS_CSN
PLLSYS_RESET_N
PLLSYS_PD_N
PLLSYS_REF1
PLLSYS_REF2
PLLFMC1_REF_SEL
PLLFMC1_SYNC_N
PLLFMC1_SCLK
PLLFMC1_CSN
PLLFMC1_RESET_N
PLLFMC1_PD_N
PLLFMC1_REF1
PLLFMC1_REF2
PLLFMC2_REF_SEL
PLLFMC2_SYNC_N
PLLFMC2_SCLK
PLLFMC2_CSN
PLLFMC2_RESET_N
PLLFMC2_PD_N
PLLFMC2_REF1
DDR_RESET
DDR_CKE
DDR_WE
DDR_CKP
DDR_CKN
DDR_ODT
DDR_RAS
DDR_CAS
DDR_UDM
DDR_LDM
DDR_A[14..0]
DDR_BA[2..0]
VME_RETRY
VME_BERR
VME_TDO
VME_A_OEN
VME_A_DIR
VME_IACKOUT
VME_DTACK
VME_D_DIR
VME_D_OEN
VME_IRQ7_1[1..7]
DDS_TXENABLE
DDS_SYNC_IN_P
DDS_SYNC_IN_N
DDS_OSK
VADC_CS
VADC_SCLK
VADC_DIN
VADJ1_CS
VADJ1_SCLK
VADJ1_DIN
VADJ1_SPI
VADJ2_CS
VADJ2_SCLK
VADJ2_DIN
VADJ2_SPI
SRAM2_TDI
SRAM2_TCK
SRAM2_TMS
SRAM1_TDI
SRAM1_TCK
SRAM1_TMS
SFP2_MODDEF1
SFP2_RATESELECT
WR_MODDEF1
WR_RATESELECT
AFPGA_TDI
AFPGA_TCK
AFPGA_TMS
FP_LEDN0
FP_LEDN1
FP_LEDN2
FP_LEDN3
FP_LEDN4
FP_LEDN5
FP_LEDN6
FP_LEDN7
AFPGA_PROG_RDWR
AFPGA_PROG_CSI
FMC1_PrsntM2C_n
FMC2_PrsntM2C_n
VADJ1_INHIBIT
VADJ2_INHIBIT
FPGPIO1_A2B
FPGPIO2_A2B
FPGPIO34_A2B
SI57X_SCL
OE_SI57X
U_AFPGA
AFPGA.SchDoc
FMC1_Dp0M2CP
FMC1_Dp0M2CN
FMC1_GBTClk0M2CP
FMC1_GBTClk0M2CN
FMC2_Dp0M2CP
FMC2_Dp0M2CN
FMC2_GBTClk0M2CP
FMC2_GBTClk0M2CN
FMC2_LaP[31..0]
FMC2_LaN[31..0]
FMC2_Clk0M2CP
FMC2_Clk0M2CN
FMC2_Clk1M2CP
FMC2_Clk1M2CN
FMC1_LaP[33..0]
FMC1_LaN[33..0]
FMC1_Clk0M2CP
FMC1_Clk0M2CN
FMC1_Clk1M2CP
FMC1_Clk1M2CN
FMC1_VrefAM2C
SRAM1_DATA[35..0]
SRAM2_DATA[35..0]
PLLFMC1_2AFPGA_P
PLLFMC1_CLKP
PLLFMC1_CLKN
SYSAPP_CLKP
SYSAPP_CLKN
VMEP0_HWLOWBYTE[7..0]
VMEP0_BUNCHSELECT[7..0]
VMEP0_HWHIGHBYTE[7..0]
VMEP0_BUSLINE[7..0]
VMEP0_DAISYCHAININ
VMEP0_DAISYCHAIN2IN
VMEP0_DAISYCHAIN2OUT
VMEP0_DAISYCHAIN1OUT
P2_DATAP[19..0]
P2_DATAN[19..0]
FMC1_Dp1M2CP
FMC1_Dp1M2CN
FMC1_GBTClk1M2CP
FMC1_GBTClk1M2CN
FMC2_Dp1M2CP
FMC2_Dp1M2CN
FMC2_GBTClk1M2CP
FMC2_GBTClk1M2CN
AFPGA_PROG_INIT
AFPGA_PROG_DONE
AFPGA_PROG_PROGRAM
AFPGA_PROG_CCLK
AFPGA_PROG_D0
AFPGA_PROG_M1
AFPGA_PROG_M0
GBIT1_SYS2APPP
GBIT1_SYS2APPN
GBIT12_REFCLKP
GBIT12_REFCLKN
GBIT2_SYS2APPP
GBIT2_SYS2APPN
GBIT3_SYS2APPP
GBIT3_SYS2APPN
GBIT34_REFCLKP
GBIT34_REFCLKN
GBIT4_SYS2APPP
GBIT4_SYS2APPN
AFPGA_TDI
AFPGA_TCK
AFPGA_TMS
PUSHBUTTON
SYSAPP_SLOW1
SYSAPP_SLOW2
AFPGA_PROG_D1
AFPGA_PROG_D2
AFPGA_PROG_D3
AFPGA_PROG_D4
AFPGA_PROG_D5
AFPGA_PROG_D6
AFPGA_PROG_D7
AFPGA_PROG_CSI
AFPGA_PROG_RDWR
PLLFMC2_2AFPGA_P
PLLFMC2_2AFPGA_N
PLLFMC2_CLKP
PLLFMC2_CLKN
VMEP0_TTLBUNCHCLK
VMEP0_TTLTCLK
PLLSYS_AFPGACLKP
PLLSYS_AFPGACLKN
PLLDDS_2AFPGA_P
PLLDDS_2AFPGA_N
VME_SYSRESET
SRAM1_ADDRESS[24..0]
SRAM1_CLOCK
SRAM1_WE_N
SRAM1_OE_N
SRAM1_BWA_N
SRAM1_BWB_N
SRAM1_BWC_N
SRAM1_BWD_N
SRAM2_ADDRESS[24..0]
SRAM2_CLOCK
SRAM2_WE_N
SRAM2_OE_N
SRAM2_BWA_N
SRAM2_BWB_N
SRAM2_BWC_N
SRAM2_BWD_N
AFPGA_TDO
FP_GPIO1
FP_GPIO2
FP_GPIO3
FP_GPIO4
PLLFMC1_REF2
PLLFMC2_REF2
U_FmcConnector
FmcConnector.SchDoc
FMC1_PGC2M
4k7
R254
VADJ1
V3P3FMC1
V12P0FMC1
GND
LaP[33..0]
LaN[33..0]
PGC2M
TMS
TCK
TDI
TRST_L
GA1
VAdj
Dp0C2MP
Dp0C2MN
SCL
SDA
GA0
Clk1C2MP
Clk1C2MN
Clk0C2MP
Clk0C2MN
V3P3FMC
V3P3AuxFMC
V12P0FMC
Dp1C2MP
Dp1C2MN
FMC1_GBTClk0M2CP
FMC1_GBTClk0M2CN
FMC1_TDO
FMC1_VrefAM2C
FMC1_PrsntM2C_n
FMC1_Clk0M2CP
FMC1_Clk0M2CN
FMC1_Clk1M2CP
FMC1_Clk1M2CN
FMC1_Dp0M2CP
FMC1_Dp0M2CN
FMC1_GBTClk1M2CP
FMC1_GBTClk1M2CN
FMC1_Dp1M2CP
FMC1_Dp1M2CN
FMC1_LaP[33..0]
FMC1_LaN[33..0]
FMC1_TMS
FMC1_TCK
FMC1_TDI
FMC1_TRST
FMC1_Dp0C2MP
FMC1_Dp0C2MN
FMC1_SCL
FMC1_SDA
FMC1_Dp1C2MP
FMC1_Dp1C2MN
FMC2_Dp0C2MP
FMC2_Dp0C2MN
FMC2_Dp1C2MP
FMC2_Dp1C2MN
SRAM1_ADDRESS[24..0]
SRAM1_CLOCK
SRAM1_WE_N
SRAM1_OE_N
SRAM1_BWA_N
SRAM1_BWB_N
SRAM1_BWC_N
SRAM1_BWD_N
SRAM2_ADDRESS[24..0]
SRAM2_CLOCK
SRAM2_WE_N
SRAM2_OE_N
SRAM2_BWA_N
SRAM2_BWB_N
SRAM2_BWC_N
SRAM2_BWD_N
FMC1_Dp1C2MP
FMC1_Dp1C2MN
FMC2_Dp1C2MP
FMC2_Dp1C2MN
GBIT1_APP2SYSP
GBIT1_APP2SYSN
GBIT2_APP2SYSP
GBIT2_APP2SYSN
GBIT3_APP2SYSP
GBIT3_APP2SYSN
GBIT4_APP2SYSP
GBIT4_APP2SYSN
AFPGA_TDO
FP_GPIO1
FP_GPIO2
FP_GPIO3
FP_GPIO4
PLLFMC1_REF2
PLLFMC2_REF2
U_SRAM
SRAM.SchDoc
SRAM1_ADDRESS[24..0]
SRAM1_DATA[35..0]
SRAM1_CLOCK
SRAM1_WE_N
SRAM1_OE_N
SRAM1_BWA_N
SRAM1_BWB_N
SRAM1_BWC_N
SRAM1_BWD_N
SRAM2_TDI
SRAM2_TMS
SRAM2_TCK
ADDRESS[24..0]
DATA[35..0]
CLOCK
WE_N
OE_N
BWA_N
BWB_N
BWC_N
BWD_N
TDI
TMS
TCK
TDO
SRAM1_TDO
SRAM2_TDO
U_FrontPannel
FrontPannel.SchDoc
FP_GPIO1
FP_GPIO2
FP_GPIO3
FP_GPIO4
FP_LEDN0
FP_LEDN1
FP_LEDN2
FP_LEDN3
FP_LEDN4
FP_LEDN5
FP_LEDN6
FP_LEDN7
SFP2_GBITOUT_P
SFP2_GBITOUT_N
SFP2_MODDEF1
SFP2_MODDEF2
WR_GBITOUT_P
WR_GBITOUT_N
WR_MODDEF1
WR_MODDEF2
SFP2_RATESELECT
WR_RATESELECT
FPGPIO1_A2B
FPGPIO2_A2B
FPGPIO34_A2B
SFP2_GBITIN_P
SFP2_GBITIN_N
SFP2_TXFAULT
SFP2_TXDISABLE
SFP2_MODDEF0
WR_GBITIN_P
WR_GBITIN_N
WR_TXFAULT
WR_TXDISABLE
WR_MODDEF0
SFP2_LOS
WR_LOS
PUSHBUTTON
U_ClkGeneration
ClkGeneration.SchDoc
PLLFMC1_REF1
PLLFMC1_REF2
PLLFMC1_PD_N
PLLFMC1_SYNC_N
PLLFMC1_RESET_N
PLLFMC1_SCLK
PLLFMC1_SDIO
PLLFMC1_CSN
PLLFMC1_CS_N
PLLFMC1_REFSEL
PLLFMC2_REF1
PLLFMC2_REF2
PLLFMC2_PD_N
PLLFMC2_SYNC_N
PLLFMC2_RESET_N
PLLFMC2_SCLK
PLLFMC2_SDIO
PLLFMC2_CSN
PLLFMC2_CS_N
PLLFMC2_REFSEL
PLLSYS_REF1
PLLSYS_REF2
PLLSYS_PD_N
PLLSYS_SYNC_N
PLLSYS_RESET_N
PLLSYS_SCLK
PLLSYS_SDIO
PLLSYS_CSN
PLLSYS_CS_N
PLLSYS_REF_SEL
PLLDAC_SCLK
PLLDAC_SYNC
PLLDAC_DIN
PLLDAC_CLRN
PLLDAC_LDAC
DDS_MASTER_RST
DDS_POWER_DWN
DDS_D[15..0]
DDS_F[1..0]
DDS_TXENABLE
DDS_PROFILE[2..0]
DDS_IO_UPDATE
DDS_OSK
DDS_SDO
DDS_SCLK
DDS_IO_RESET
DDS_DRCTL
DDS_DRHOLD
DDS_SYNC_IN_P
DDS_SYNC_IN_N
PLLDDS_PD_N
PLLDDS_SYNC_N
PLLDDS_RESET_N
PLLDDS_SCLK
PLLDDS_SDIO
PLLDDS_CS_N
OE_SI57X
SI57X_SDA
SI57X_SCL
PLLFMC1_2FMC_P0
PLLFMC1_2FMC_N0
PLLFMC1_2AFPGA_P
PLLFMC1_2AFPGA_N
PLLFMC1_2FMC_P1
PLLFMC1_2FMC_N1
PLLFMC1_SDO
PLLFMC1_LD
PLLFMC1_STATUS
PLLFMC1_REFMON
PLLFMC2_2FMC_P0
PLLFMC2_2FMC_N0
PLLFMC2_2AFPGA_P
PLLFMC2_2AFPGA_N
PLLFMC2_2FMC_P1
PLLFMC2_2FMC_N1
PLLFMC2_SDO
PLLFMC2_LD
PLLFMC2_STATUS
PLLFMC2_REFMON
PLLSYS_SDO
PLLSYS_LD
PLLSYS_STATUS
PLLSYS_REFMON
VCTCXO_CLK
PLLDAC_SDO
PLLSYS_SFPGACLKP
PLLSYS_SFPGACLKN
PLLSYS_AFPGACLKP
PLLSYS_AFPGACLKN
DDS_SYNC_SMP_ERR
DDS_RAM_SWP_OVR
DDS_PDCLK
DDS_SYNC_CLK
DDS_PLL_LOCK
DDS_SYNC_OUT_P
DDS_SYNC_OUT_N
DDS_SDO
DDS_DROVER
PLLDDS_SDO
PLLDDS_LD
PLLDDS_STATUS
PLLDDS_REFMON
GBIT12_REFCLKS_P
GBIT12_REFCLKS_N
GBIT12_REFCLKA_P
GBIT12_REFCLKA_N
GBIT34_REFCLKS_P
GBIT34_REFCLKS_N
GBIT34_REFCLKA_P
GBIT34_REFCLKA_N
WR_REFCLK_P
WR_REFCLK_N
PLLFMC2_2P2_P
PLLFMC2_2P2_N
PLLFMC1_2P2_P
PLLFMC1_2P2_N
PLLDDS_2SFPGA_P
PLLDDS_2SFPGA_N
PLLDDS_2AFPGA_P
PLLDDS_2AFPGA_N
PLLFMC1_2SFPGA_P
PLLFMC1_2SFPGA_N
PLLFMC2_2SFPGA_P
PLLFMC2_2SFPGA_N
SI57X_CLKP
SI57X_CLKN
U_PowerSupplies
PowerSupplies.SchDoc
VADJ1_CS
VADJ1_SCLK
VADJ1_DIN
VADJ1_SPI
VADJ2_CS
VADJ2_SCLK
VADJ2_DIN
VADJ2_SPI
VADC_CS
VADC_SCLK
VADC_DIN
VADJ1_INHIBIT
VADJ2_INHIBIT
VADC_DOUT
U_DDR3
DDR3.SchDoc
DDR_A[13..0]
DDR_DQ[15..0]
DDR_CKP
DDR_CKN
DDR_RAS
DDR_CKE
DDR_CAS
DDR_WE
DDR_ODT
DDR_BA[2..0]
DDR_UDM
DDR_LDM
DDR_UDQSP
DDR_LDQSP
DDR_UDQSN
DDR_LDQSN
U_VMEP0
VMEP0.SchDoc
VMEP0_BUSLINE[7..0]
VMEP0_BUSLINE_OE
VMEP0_BUSLINE_DIR
VMEP0_BUNCHSELECT[7..0]
VMEP0_BUNCHSELECT_OE
VMEP0_BUNCHSELECT_DIR
VMEP0_HWLOWBYTE[7..0]
VMEP0_HWLOWBYTE_OE
VMEP0_HWLOWBYTE_DIR
VMEP0_HWHIGHBYTE[7..0]
VMEP0_HWHIGHBYTE_OE
VMEP0_HWHIGHBYTE_DIR
VMEP0_DAISYCHAIN2OUT
VMEP0_DAISYCHAIN1OUT
VMEP0_TTLBUNCHCLK
VMEP0_LVDSBUNCHCLK_OUT
VMEP0_TTLTCLK
VMEP0_LVDSTCLK_OUT
VMEP0_TTLBUNCHCLK
VMEP0_TTLBUNCHCLK_DIR
VMEP0_LVDSBUNCHCLK_OUT
VMEP0_LVDSBUNCHCLK_OE
VMEP0_TTLTCLK
VMEP0_TTLTCLK_DIR
VMEP0_LVDSTCLK_OUT
VMEP0_LVDSTCLK_OE
VMEP0_DAISYCHAININ
VMEP0_DAISYCHAIN2IN
VMEP0_LVDSBUNCHCLK_IN
VMEP0_LVDSTCLK_IN
Project/Equipment -
Document
AB-BI
VME FMC Carrier
Top
European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland
Designer Andrea Boccardi
Drawn by Andrea Boccardi
Check_by -
Last Mod. -
File VMEFMC.SchDoc
Print Date 4/1/2010 9:43:30 AM
Sheet - of -
XX/XX/XXXX
3/30/2010
EDA-XXXXX-VX-X
Size A2
Rev -

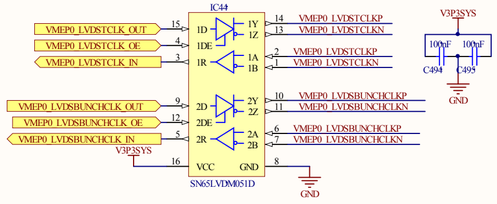












Project/Equipment	-		
Document	VME FMC Carrier	Designer	Andrea Boccardi
	Title2	Drawn by	Andrea Boccardi
AB-BI		Check by	-
		Last Mod	-
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		Print Date	4/1/2010 9:43:30 AM
European Organization for Nuclear Research, CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Sheet	- of -
		Size	A2
		Rev	-

Bill of Materials

Bill of Materials For Project [VmeFmcCarrier.PrjPCB] [No PCB Document Sel

Source Data From: VmeFmcCarrier.PrjPCB
Project: VmeFmcCarrier.PrjPCB
Variant: None

Creation Date: 4/1/2010 9:46:19 AM
Print Date: 4/2009 40560

Footprint	#Column Name	LibRef	#Column Name Error/Designator	Description	Quantity
CAPC1005X5		EC0402_100N		Non-polarised capacitor	200
CAPMP7343		CTS7343-1_470UF_6.3V_10%		Polarised capacitor	23
CAPC2012X1		EC0805_22UF		Non-polarised capacitor	1
CAPC2012X1		EC0805_22NF		Non-polarised capacitor	1
CAPC2012X1		EC0805_1NF_2		Non-polarised capacitor	2
CAPC2012X1		EC0805_220NF		Non-polarised capacitor	1
CAPC2012X1		EC0805_47NF_		Non-polarised capacitor	20
CAPC1608X0		EC0603_100NF		Non-polarised capacitor	1
CAPC1005X5		EC0402_33NF_		Non-polarised capacitor	1
CAPC3216X1		EC1206_10UF_		Non-polarised capacitor	4
CAPAE1030X		CAE630-1000UF_6.3V_20%		Polarised capacitor	4
CAPC3225X2		EC1210_10UF_		Non-polarised capacitor	6
CAPC2012X1		EC0805_22UF		Non-polarised capacitor	3
CAPC3216X1		EC1206_22UF_		Non-polarised capacitor	4
CAPC1608X0		EC0603_4.7UF_6.3V_10%		Non-polarised capacitor	1
CAPAE830X		CAE830-1000UF_6.3V_20%		Polarised capacitor	4
TYCO_63673		TYCO_6367309		SFP: Cage Bottom (Small Form-factor Pluggable)	2
TYCO_63673		TYCO_6367310		SFP: Cage Top (Small Form-factor Pluggable)	2
FUSC1608X		FUSC0603_8CU		Fuse	13
FUSC1608X		0603F350-2		Fuse	2
BGA676C110		0603F360-2		SPARTAN-6, FPGA, 676-Ball BGA, Commercial Grade, Pb-Free	2
CLOCK_ICS5		ADI9516-4BCPZ		14-Output Clock Generator with Integrated 1.6 GHz VCO	1
SOP65P640		ADI5668BRUZ		Quad 16-Bit DAC with6 ppm/°C On-Chip Reference	1
QFP50P160		ADI9918BSVZ		5 GSPS, 14-Bit, 3.3 V CMOS Direct Digital Synthesizer	1
BGA96C80P		MT41J128M16		16 Meg x 16 x 8 Banks DDR3 SDRAM	1
SOP65P610		SN74VMEH22		8-Bit Universal Bus Transceiver and Two	10
TEXAS_BCR		PTH04T230WA		8A, 2.2 V to 5.5 V Input, Non-Isolated, V Output Adjustable Power Module With PMBus	4
QFN65P900		TPS74401RGW		Single Output LDO, 3.0A, Adj,0.8 to 3.3V, Fast Transient Response, Programmable Soft-Start	3
SOIC127P6		AD7688AR		2.7 V to 5.25 V, Micro Power, 8-Channel, 525 kSPS, 16-Bit ADC	1
SOIC65P350		TPS51200DRC		Sink/Source DDR Termination Regulator	1
TEXAS_ELC		PT6914C		12 Watt SV/3.3V Input Plus to Minus Volt Converter	1
SOP65P610		MAX5483ZUD+		75-Bit, Nonvolatile Linear-Taper Digital Potentiometer	2
TEXAS_ELC		PT6916C		12 Watt SV/3.3V Input Plus to Minus Volt Converter	1
SOP65P490		DS18B20+		Programmable Resolution 1-Wire Digital Thermometer	1
SOIC127P1		MSP12B-MFIEG		128 Mbit (Multilevel), low-voltage, Serial Flash memory with 80-MHz SPI bus interface	2
BGA165C10		CY7C1470BV3		72-Mbit (2M x 36) Pipelined 3.3V SRAM	2
SOIC127P6		SN65LVDM6SV		High-Speed Differential Line Drivers And Receivers	1
SMTSO-63-		HIROSE_U-FL-R-SMT-1(10)			2
		Connector 160absbot Male (6x32), Connector 160absbot Male (6x32), Connector HAR-BUS 6E Female (abcdef) + Shield (f), Connector VITA 57 400 Female (abcdefghijk)		Connector 160absbot Male (6x32), Connector HAR-BUS 6E Female (abcdef) + Shield (f), Connector VITA 57 400 Female (abcdefghijk)	5
LEMO_EPY		LEMO_EPY.00		Dual Female Coax 1-2 Common Shield 3	2
TYCO_13670		TYCO_1367072		20 Position SFP Connector (Small Form-factor Pluggable)	2
MOLEX_470		MOLEX_470400		7 Pin + 1 Shield SATA Receptacle	1
MOLEX_878		MOLEX_878330		Connector 14 Male	1
INDC2012X1		INDC2012_4.7UH		Inductor With Magnetic core	2
INDC2014X1		INDC1812_10UH_20%_ASMT_DWI		Inductor With Magnetic core	4
LEDC1608X		LED_RCHM_0		LED Red 1C 2A	23
LED_BIVAR		LED_BIVAR_4		LED x4 Red 1C2A-WOT_3C4A_3C4A_7C	2
OSC_RAKON		OSC_2594HZ_0		Oscillator 4 pins 1=Voltage Control 2=GN 3=OUT 4=VCC	1
OSC_SILICO		OSC_10-MHMHZ_SILICON		Any-Rate I2C Programmable XO Oscillator SI570 Serie	1
PB_TYCO_A		PB_TYCO_ALC		Push-Button Switch SPDT	1
RESC1005X		RD402_49R9_0		Resistor - 0.1%	24
RESC1005X		RD402_1K3_1%		Resistor - 1%	23
RESC1005X		RD402_10K_1%		Resistor - 1%	45
RESC2012X		RD805_100R_1		Resistor - 1%	6
RESC2012X		RD805_4K7_1%		Resistor - 1%	20
RESC2012X		RD805_2K1_1%		Resistor - 1%	4
RESC2012X		RD805_4K12_0		Resistor - 0.1%	4
RESC2012X		RD805_1R5_1%		Resistor - 1%	1
RESC2012X		RD805_200R_1		Resistor - 1%	23
RESC1608X		RD603_10K_0.1		Resistor - 0.1%	3
RESC1005X		RD402_30R_1%		Resistor - 1%	1
RESC2012X		RD805_51R_1%		Resistor - 1%	2
RESC1005X		RD402_100R_1		Resistor - 1%	1
RESC1005X		RD402_24R9_1		Resistor - 0.1%	1
RESC2012X		RD805_5R_1%		Resistor - 1%	40
RESC1005X		RD402_150R_1		Resistor - 1%	14
RESC1005X		RD402_51R_1%		Resistor - 1%	4
RESC1005X		RD402_10K_0.1		Resistor - 0.1%	2
RESC1005X		RD402_3K_1%		Resistor - 1%	4
RESC1608X		RD603_931R_0		Resistor - 0.1%	3
RESC1608X		RD603_2K07_0		Resistor - 0.1%	2
RESC1608X		RD603_1K13_0		Resistor - 0.1%	1
RESC1005X		RD402_1K1_1%		Resistor - 1%	12
RESC1005X		RD402_5K6_1%		Resistor - 1%	2
RESC1608X		RD603_2K87_0		Resistor - 0.1%	1
RESC1608X		RD603_2K49_0		Resistor - 0.1%	2
RESC1608X		RD603_49R9_0		Resistor - 0.1%	1
RESC1608X		RD603_845R_0		Resistor - 0.1%	1
RESC1608X		RD603_5R_JUM		Resistor - 1%	4
RESC2012X		RD805_2K4_1%		Resistor - 1%	2
RESC1005X		RD402_5R_JUM		Resistor - 1%	4
SW_DMRC1		SW_DMRC06_		6 Ways SPST DIP Switch	1
SOT95P230		MSH103		N-CHANNEL MOSFET WITH DIODE	6
					302

Approved **Notes**