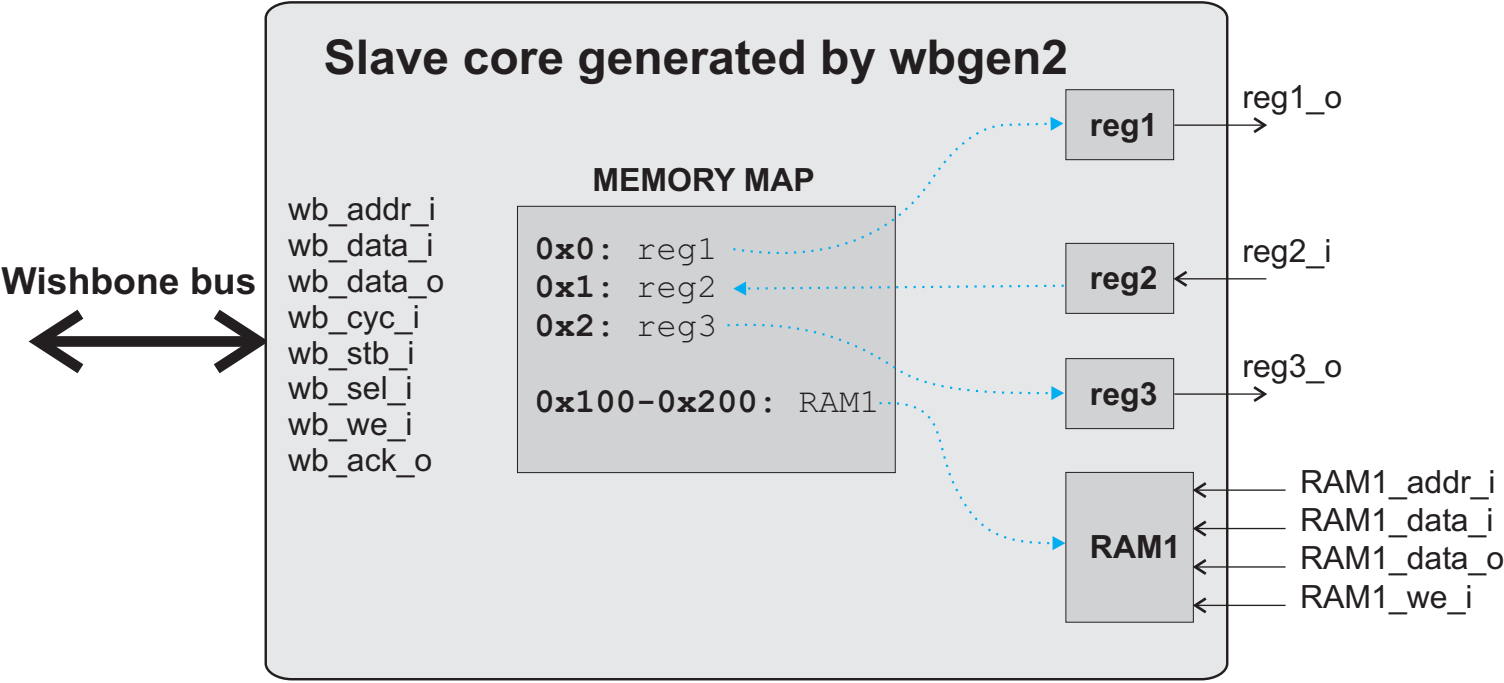
Slave core generated by wbgen2
Wishbone bus
wb_addr_i
wb_data_i
wb_data_o
wb_cyc_i
wb_stb_i
wb_sel_i
wb_we_i
wb_ack_o
MEMORY MAP
0x0: reg1
0x1: reg2
0x2: reg3
0x100-0x200: RAM1
reg1
reg2
reg3
RAM1
reg1_o
reg2_i
reg3_o
RAM1_addr_i
RAM1_data_i
RAM1_data_o
RAM1_we_i