MAROC

FPGA CONNECTIONS

PAGE 2

CLOCK GENERATOR

AND CONTROL DACS

PAGE 5

CTEST DAC
LEDS
SWITCHES

PAGE 8

DC-DC CONVERTERS

3.5V (MAROC)
3.3V

PAGE 10

LVDS I/O CONNECTIONS

( DIN 41612 )

FPGA CONNECTIONS

PAGE 3

SFP CAGES

ESATA CONNECTORS

FPGA CONNECTIONS

PAGE 6

DC-DC CONVERTERS

1.2V (VCCINT)
2.5V

PAGE 9

POWER CONNECTIONS
VCCINT=1.2V
VCCAUX=2.5V
VCCO(LVDS)=2.5V
VCCO(MAROC)=3.3V

DECOUPLING

PAGE 11

BUSSED LINES -

CLOCKS, TRIGGERS

PAGE 4

SPI FLASH

JTAG CONNECTIONS

M0,M1 CONNECTIONS

PAGE 7

| | | | | | | |
|---|---|---|---|---|---|---|
| | Tue Jun | 3 10:41:38 | 2014 | | | |
| | | | DAVID CUSSANS | | | |
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TITLE uob_hep_pc049a_lib

MODULE: pc049a_toplevel

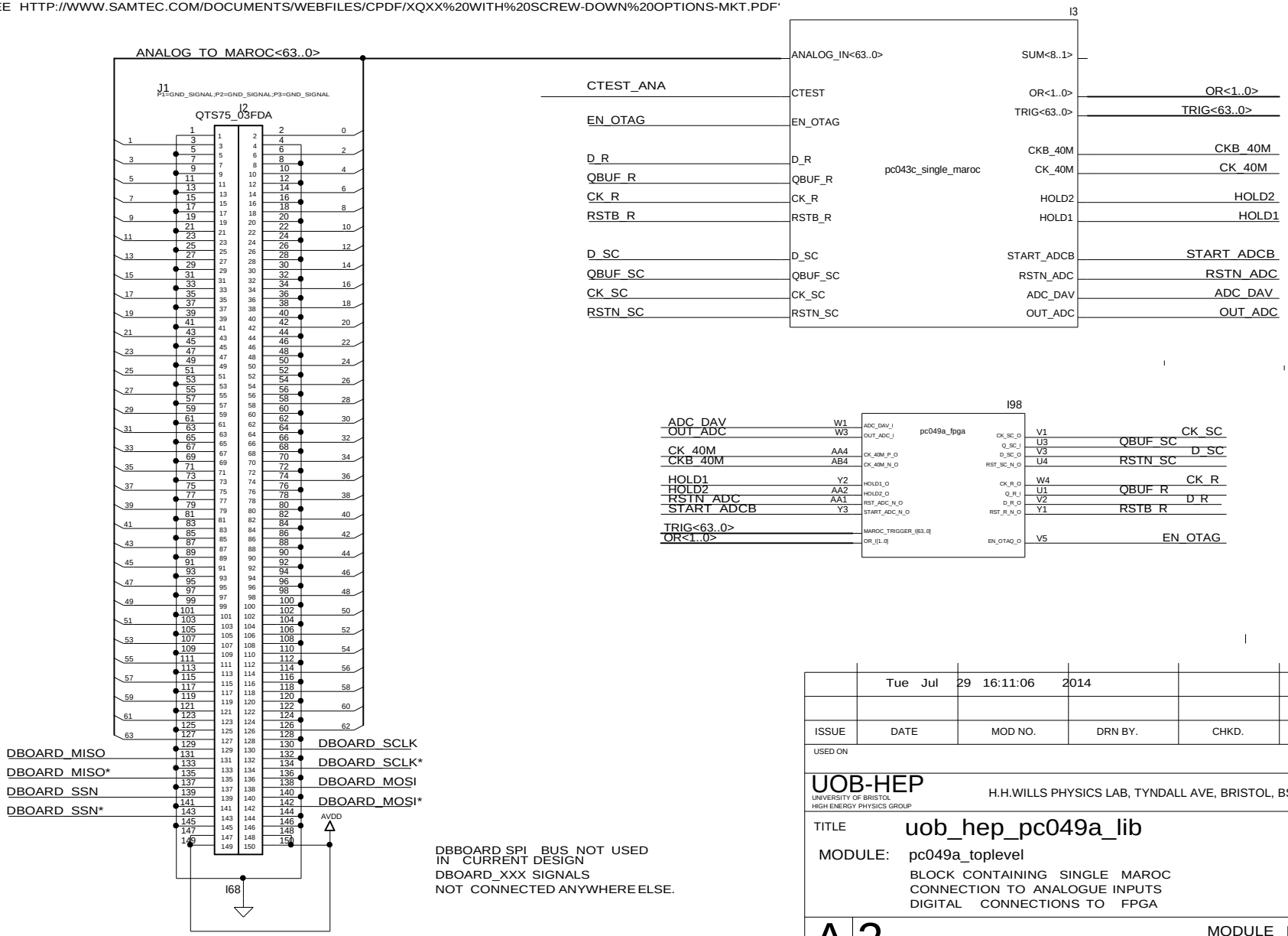
OVERALL LAYOUT

A2

MODULE PAGE: 1 OF 11
OVERALL PAGE: 1 OF 14

TOTAL NO. OF SHEETS

ADD HOLES TO ALLOW QTS CONNECTORTO MATE TO SQCD CABLE
SEE HTTP://WWW.SAMTEC.COM/DOCUMENTS/WEBFILES/CPDF/XQXX%20WITH%20SCREW-DOWN%20OPTIONS-MKT.PDF'




DBBOARD SPI BUS NOT USED
IN CURRENT DESIGN
DBOARD_XXX SIGNALS
NOT CONNECTED ANYWHERE ELSE.

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TITLE uob_hep_pc049a_lib

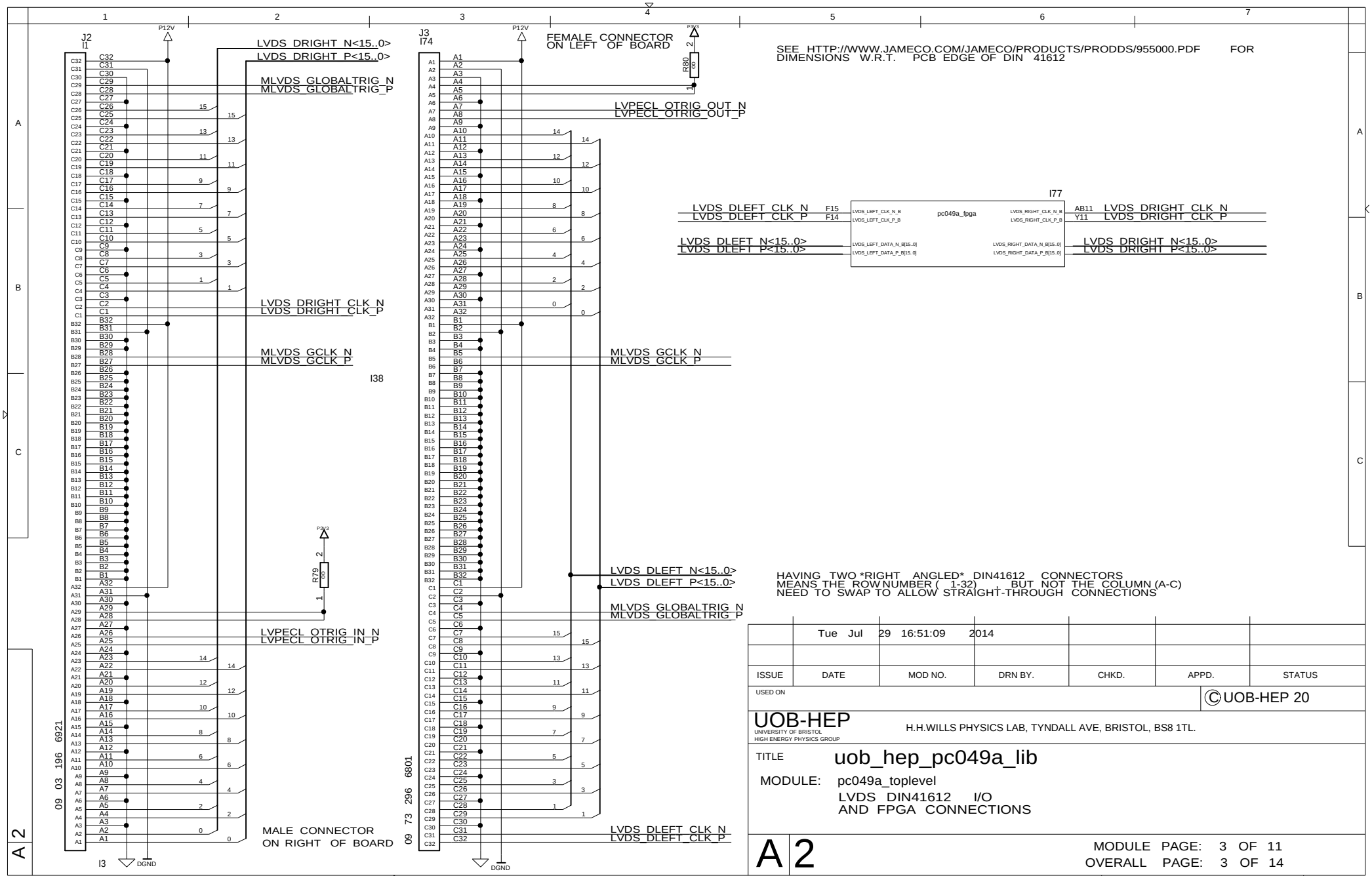
MODULE: pc049a_toplevel

BLOCK CONTAINING SINGLE MAROC
CONNECTION TO ANALOGUE INPUTS
DIGITAL CONNECTIONS TO FPGA

A2

MODULE PAGE: 2 OF 11
OVERALL PAGE: 2 OF 14

TOTAL NO. OF SHEETS


J2
I1
P12V
LVDS_DRIGHT_N<15..0>
LVDS_DRIGHT_P<15..0>
MLVDS_GLOBALTRIG_N
MLVDS_GLOBALTRIG_P
LVDS_DRIGHT_CLK_N
LVDS_DRIGHT_CLK_P
MLVDS_GCLK_N
MLVDS_GCLK_P
I38
LVPECL_OTRIG_IN_N
LVPECL_OTRIG_IN_P
R79
P3V3
MALE CONNECTOR
ON RIGHT OF BOARD
I3
DGND
J3
I74
FEMALE CONNECTOR
ON LEFT OF BOARD
R80
LVPECL_OTRIG_OUT_N
LVPECL_OTRIG_OUT_P
LVDS_DLEFT_N<15..0>
LVDS_DLEFT_P<15..0>
LVDS_DLEFT_CLK_N
LVDS_DLEFT_CLK_P
SEE HTTP://WWW.JAMECO.COM/JAMECO/PRODUCTS/PRODDS/955000.PDF FOR
DIMENSIONS W.R.T. PCB EDGE OF DIN 41612
I77
pc049a_fpga
LVDS_DLEFT_CLK_N F15
LVDS_DLEFT_CLK_P F14
LVDS_DLEFT_N<15..0>
LVDS_DLEFT_P<15..0>
AB11 LVDS_DRIGHT_CLK_N
Y11 LVDS_DRIGHT_CLK_P
LVDS_DRIGHT_N<15..0>
LVDS_DRIGHT_P<15..0>
HAVING TWO *RIGHT ANGLED* DIN41612 CONNECTORS
MEANS THE ROW NUMBER ( 1-32) , BUT NOT THE COLUMN (A-C)
NEED TO SWAP TO ALLOW STRAIGHT-THROUGH CONNECTIONS
09 03 196 6921
09 73 296 6801
Tue Jul 29 16:51:09 2014
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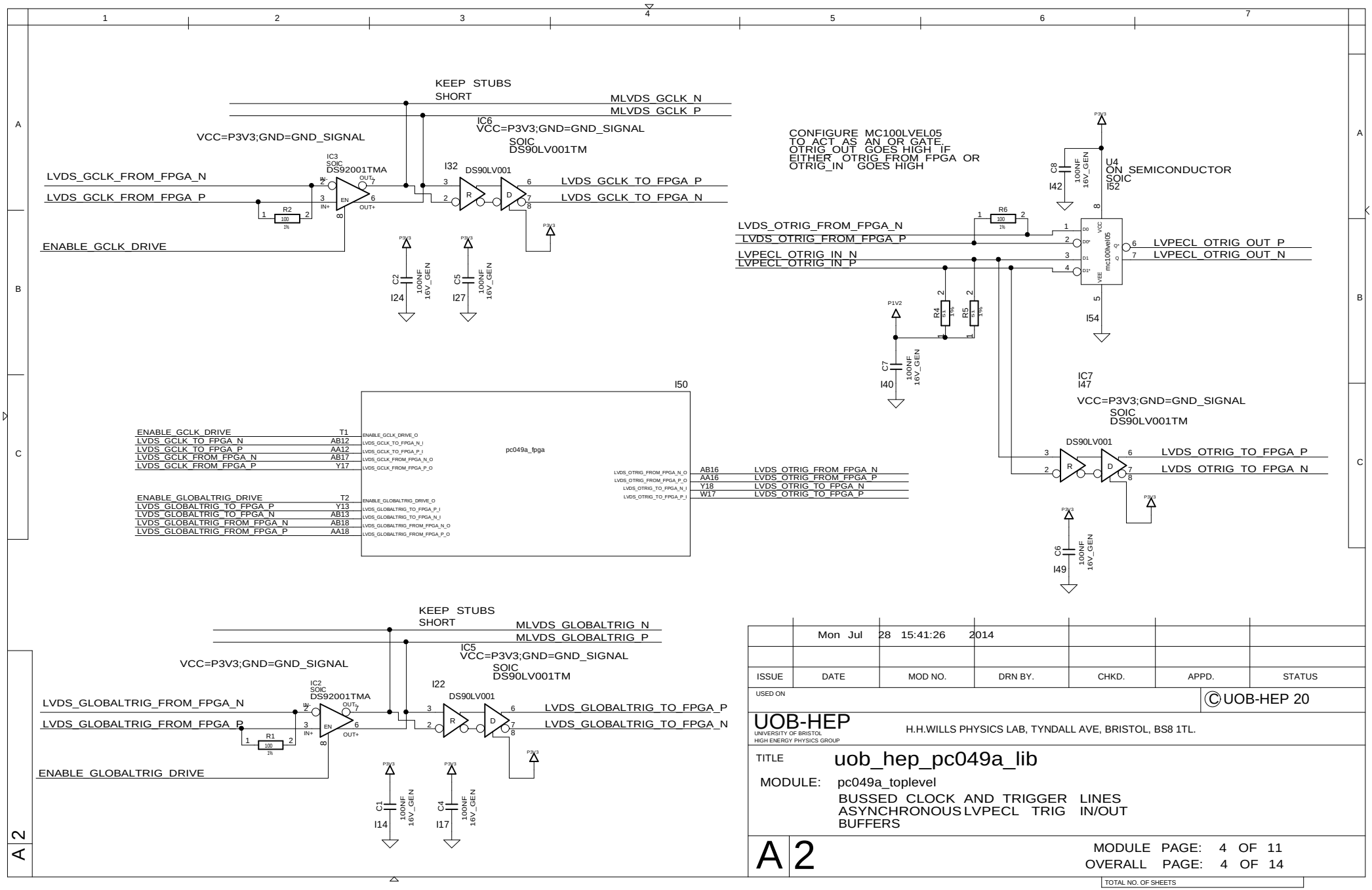
TITLE uob_hep_pc049a_lib
MODULE: pc049a_toplevel
LVDS DIN41612 I/O
AND FPGA CONNECTIONS
A2
MODULE PAGE: 3 OF 11
OVERALL PAGE: 3 OF 14
TOTAL NO. OF SHEETS

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TITLE uob_hep_pc049a_lib

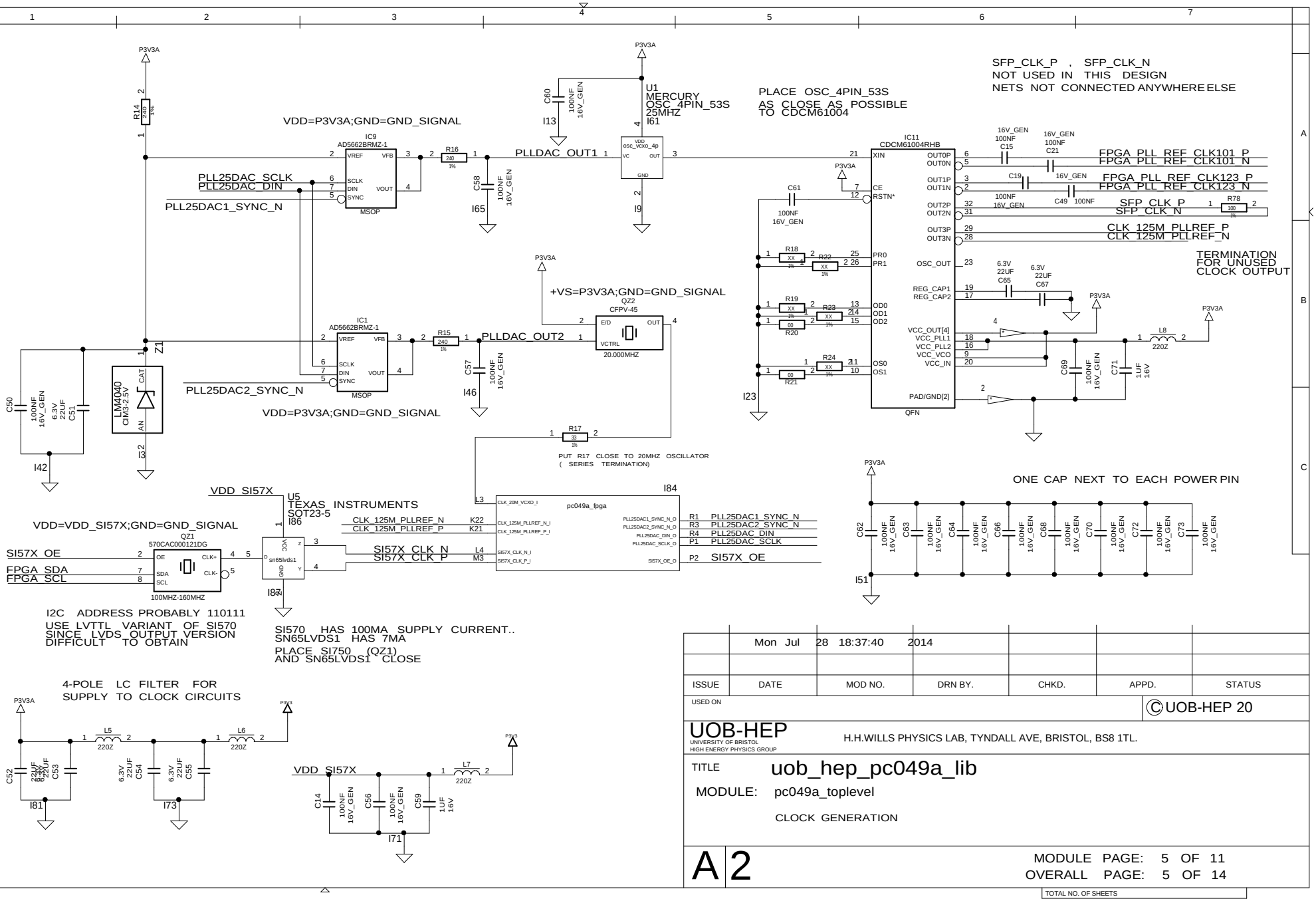
MODULE: pc049a_toplevel

BUSSED CLOCK AND TRIGGER LINES
ASYNCHRONOUS LVPECL TRIG IN/OUT
BUFFERS

A2

MODULE PAGE: 4 OF 11
OVERALL PAGE: 4 OF 14

TOTAL NO. OF SHEETS

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TITLE uob_hep_pc049a_lib

MODULE: pc049a_toplevel

CLOCK GENERATION

A2

MODULE PAGE: 5 OF 11
OVERALL PAGE: 5 OF 14

TOTAL NO. OF SHEETS

SFP POWER CONSUMPTION UP TO 1W
TRY TO LIMIT DROP OVER FILTER TO < 0.1V
SO DC RESISTANCE < 0.3 OHMS

ORIENT CONNECTOR WITH
PINS 1-10 TOWARDS BEZEL
USE WITH A TYCO SFP CAGE
6367035-1

J6
1367073-1

SFP0_RX_P
SFP0_RX_N
SFP0_MOD_DEF0
SFP0_MOD_DEF1
SFP0_MOD_DEF2
SFP0_RATE_SELECT
SFP0_TX_P
SFP0_TX_N
SFP0_TX_DISABLE
SFP0_TX_FAULT
SFP0_LOS

RD+ RD- MOD_DEF0 MOD_DEF1 MOD_DEF2 RATE_SELECT VCCR VEER TD+ TD- TX_DISABLE TX_FAULT LOS VCCT VEET

SFP Connector

P3V3
LI0805H121R-10
L1 L2
C9 1UF 16V
C10 1UF 16V
C11 100NF 16V_GEN
C12 1UF 16V
C13 22UF 4V
C22 100NF 16V_GEN
C23 22UF 4V

I13

J7
1367073-1

SFP1_RX_P
SFP1_RX_N
SFP1_MOD_DEF0
SFP1_MOD_DEF1
SFP1_MOD_DEF2
SFP1_RATE_SELECT
SFP1_TX_P
SFP1_TX_N
SFP1_TX_DISABLE
SFP1_TX_FAULT
SFP1_LOS

SFP Connector

L3 L4
C24 1UF 16V
C25 1UF 16V
C26 100NF 16V_GEN
C27 1UF 16V
C28 22UF 4V
C29 100NF 16V_GEN
C30 22UF 4V

I30

SFP1 SFP2 SFP3 SFP4
6367034-1 6367035-1

SFP CAGES IN TWO PARTS
SEPARATE FROM SFP CONNECTOR

GND=GND_SIGNAL GND=GND_SIGNAL
GND=GND_SIGNAL GND=GND_SIGNAL
SATA CONNECTORS

ONE NORMAL CONNECTIONS (MASTER)
OTHER WITH RX/TX SWAPPED (SLAVE)

NORMAL CONNECTIONS
(MASTER) J4
MOLEX
SMD_STR
I8

SATA_MRX_P
SATA_MRX_N
SATA_MTX_N
SATA_MTX_P
C18 100NF 16V_GEN
C16 100NF 16V_GEN

I90

TX/RX SWAPPED
(SLAVE) J5
MOLEX
SMD_STR
I4

SATA_STX_P
SATA_STX_N
SATA_SRX_N
SATA_SRX_P
C17 100NF 16V_GEN
C20 100NF 16V_GEN

I89

CROSS-OVER MEANS
CAN PLUG MASTER INTO SLAVE
WITH NORMAL ESATA CABLE

FPGA_PLL_REF_CLK101_N
FPGA_PLL_REF_CLK101_P
FPGA_PLL_REF_CLK123_N
FPGA_PLL_REF_CLK123_P

TRACE LENGTH FROM MGTAVTTRCAL TO
RESISTOR SAME LENGTH AS FROM
RESISTOR TO MGTRREF

MGT_AVCC_A

R53 1K0

I38

pc049a_fpga

SFP_LOS<1..0>
SFP_RATE_SELECT<1..0>
SFP_MOD_DEF0<1..0>
SFP_MOD_DEF1<1..0>
SFP_MODE_DEF2<1..0>
SFP_TX_FAULT<1..0>
SFP_TX_DISABLE<1..0>

SFP_RXN<1..0>
SFP_RXP<1..0>
SFP_TXN<1..0>
SFP_TXP<1..0>
SATA_RXN<1..0>
SATA_RXP<1..0>
SATA_TXN<1..0>
SATA_TXP<1..0>

SFP1_RX_N SFP0_RX_N SFP1_RX_P SFP0_RX_P SFP1_TX_N SFP0_TX_N SFP1_TX_P SFP0_TX_P
SATA_MRX_N SATA_SRX_N SATA_MRX_P SATA_SRX_P SATA_MTX_N SATA_STX_N SATA_MTX_P SATA_STX_P

MGT_AVCC_A
L9 LI0805H121R-10
C104 22UF 6.3V
C107 1UF 16V
C110 1UF 16V
C105 C108 C111 C113 100NF 16V_GEN
C106 C109 C112 C114 100NF 16V_GEN

I82

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TITLE uob_hep_pc049a_lib

MODULE: pc049a_toplevel
GIGABIT SERIAL LINKS

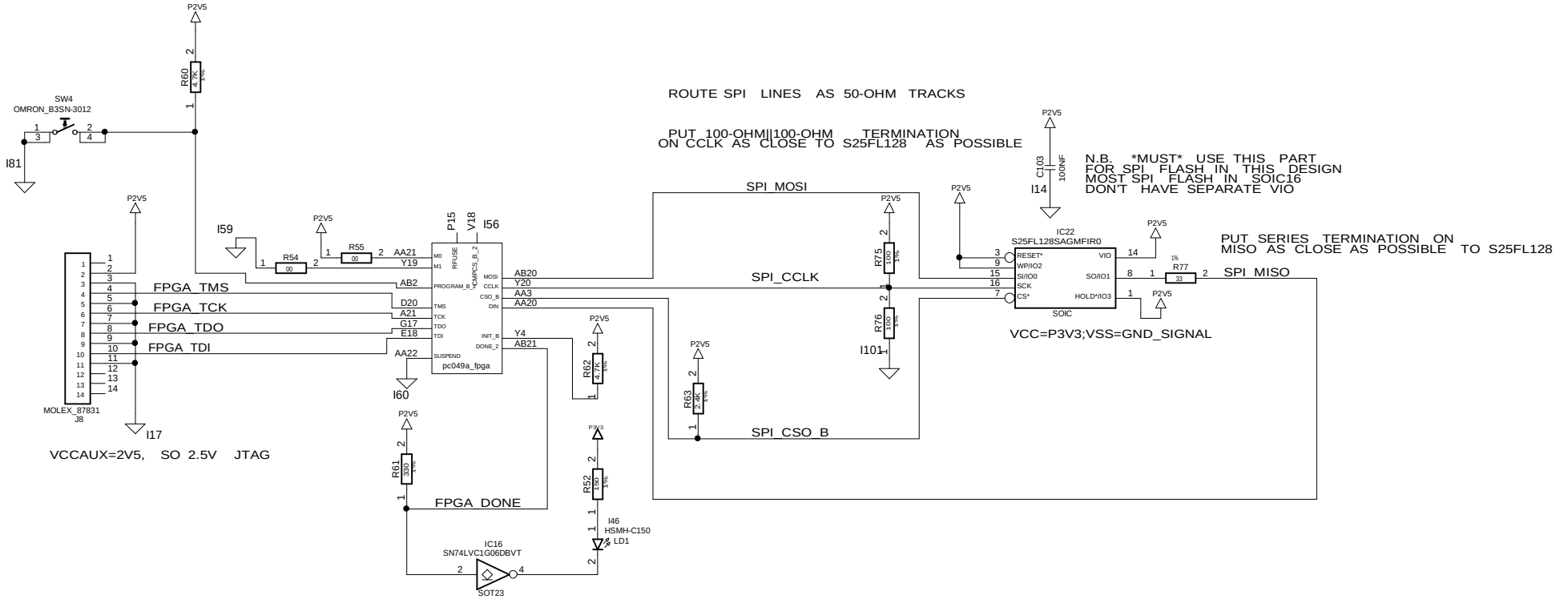
TWO SFP , TWO ESATA

A2

MODULE PAGE: 6 OF 11
OVERALL PAGE: 6 OF 14

TOTAL NO. OF SHEETS

FPGA CONFIGURES AT POWER-ON
PRESS BUTTON TO RE-CONFIGURE




ROUTE SPI LINES AS 50-OHM TRACKS

PUT 100-OHM||100-OHM TERMINATION
ON CCLK AS CLOSE TO S25FL128 AS POSSIBLE

N.B. *MUST* USE THIS PART
FOR SPI FLASH IN THIS DESIGN
MOST SPI FLASH IN SOIC16
DON'T HAVE SEPARATE VIO

PUT SERIES TERMINATION ON
MISO AS CLOSE AS POSSIBLE TO S25FL128

SEE FIGURE 2-12 IN XILINX UG380
FOR DIAGRAM OF CONFIGURATION CIRCUIT

AVOID ATTACHING LARGE, CAPACITIVE LOAD OF LED
FROM DONE PIN BY USING BUFFER
DONE GOES HIGH AND LED LIGHTS
AT END OF CONFIGURATION

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TITLE uob_hep_pc049a_lib

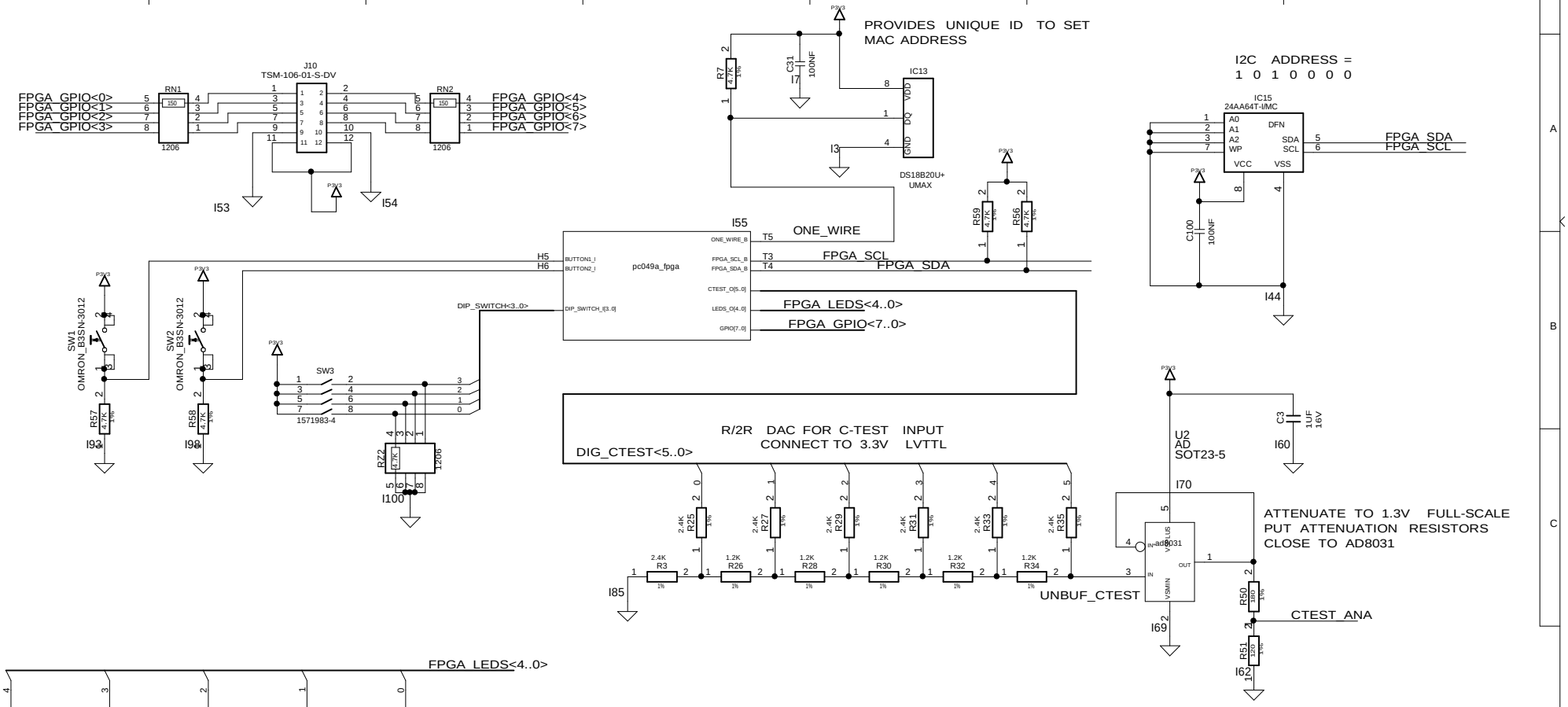
MODULE: pc049a_toplevel

SPI FLASH AND JTAG CONFIGURATION

A2

MODULE PAGE: 7 OF 11
OVERALL PAGE: 7 OF 14

TOTAL NO. OF SHEETS

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TITLE: uob_hep_pc049a_lib

MODULE: pc049a_toplevel

I2C-EEPROM , R/2R DAC FOR CTEST

1-WIRE THERMOMETER/UNIQUE ID CHIP , GPIO , LEDS , DIP-SWITCHES

A2

MODULE PAGE: 8 OF 11

OVERALL PAGE: 8 OF 14

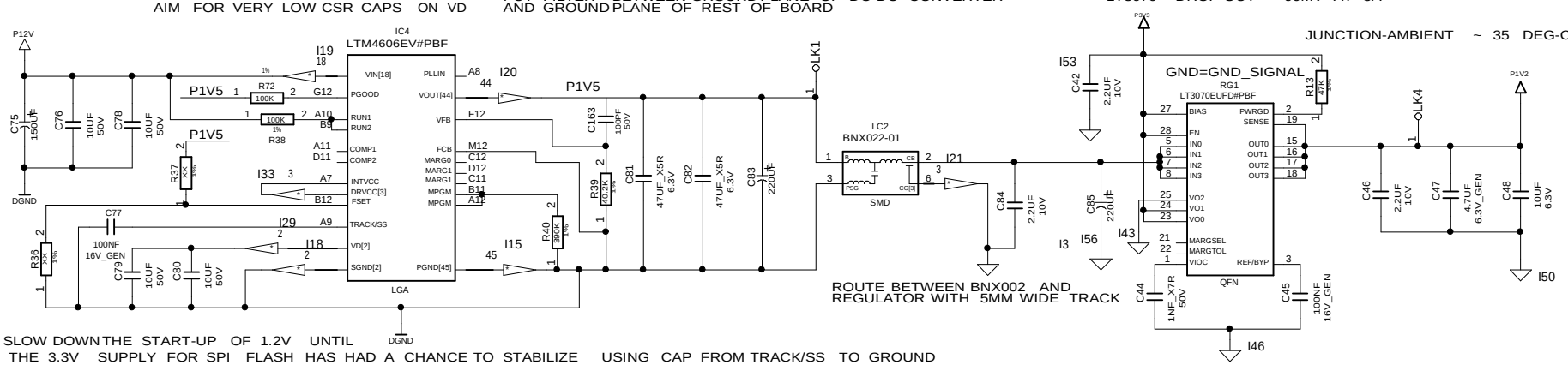
TOTAL NO. OF SHEETS

WANT TO KEEP GROUND AND POWER-PLANE NOISE AWAY FROM MAROC
PUT FILTER BETWEEN GROUND PLANE OF DC-DC CONVERTER
AND GROUND PLANE OF REST OF BOARD

AIM FOR VERY LOW CSR CAPS ON VD

PUT LINEAR REGULATOR NEAR FPGA
LT3070 DROP-OUT = 90MV AT 5A

JUNCTION-AMBIENT ~ 35 DEG-C/W

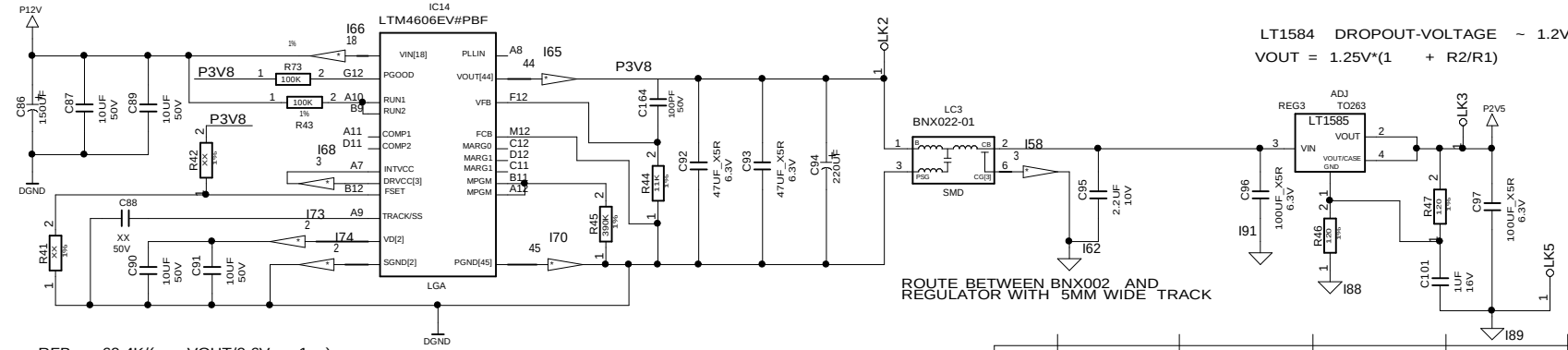



ROUTE BETWEEN BNX002 AND REGULATOR WITH 5MM WIDE TRACK

SLOW DOWN THE START-UP OF 1.2V UNTIL THE 3.3V SUPPLY FOR SPI FLASH HAS HAD A CHANCE TO STABILIZE USING CAP FROM TRACK/SS TO GROUND

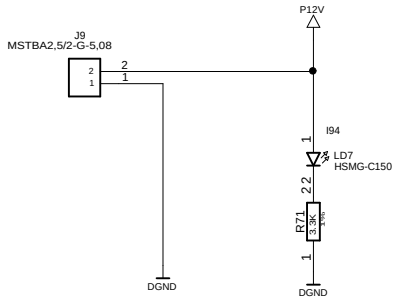
LT1584 DROPOUT-VOLTAGE ~ 1.2V @ 4.5A , 25 DEG-C/W

VOUT = 1.25V*(1 + R2/R1)




ROUTE BETWEEN BNX002 AND REGULATOR WITH 5MM WIDE TRACK

RFB = 60.4K/( VOUT/0.6V -1 )

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TITLE uob_hep_pc049a_lib

MODULE: pc049a_toplevel
DC-DC CONVERTERS
( 1.2V , 2.5V FOR FPGA )

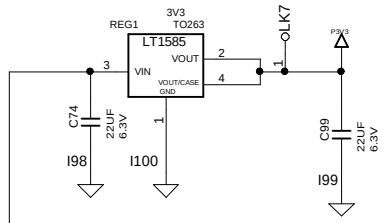
A2

MODULE PAGE: 9 OF 11
OVERALL PAGE: 9 OF 14

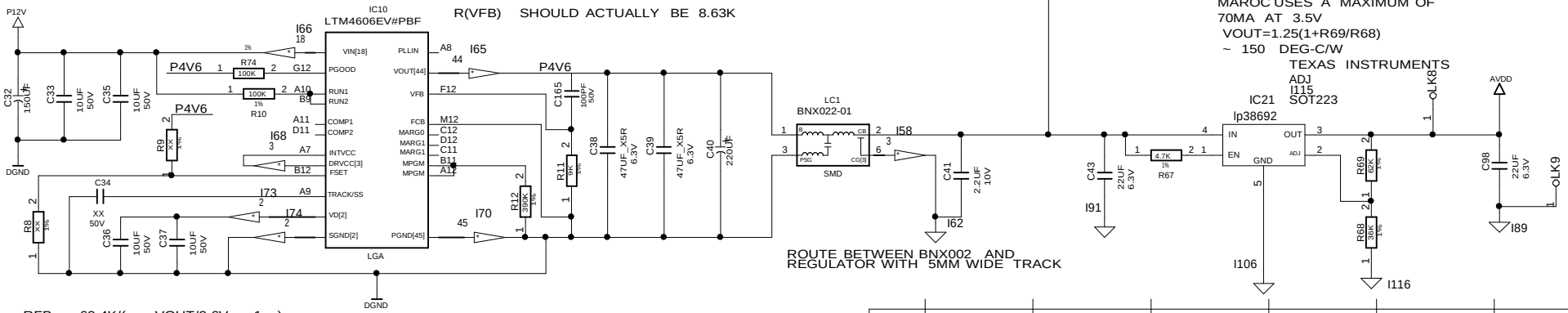
TOTAL NO. OF SHEETS

3.3V @ 4.6A
3.5V @ 0.4A ( THERMALLY LIMITED )

LT1585 DROPOUT-VOLTAGE ~ 1.2V @ 4.5A , 25-DEGC
VOUT = 1.25V*(1 + R2/R1)




PUT 3.5V REGULATOR (IC21)
CLOSE TO MAROC
0-OHMS < ESR < 100-OHMS
LP38692 DROP-OUT = 0.4V @ 0.8A
MAROC USES A MAXIMUM OF
70MA AT 3.5V
VOUT=1.25(1+R69/R68)
~ 150 DEG-C/W




RFB = 60.4K/( VOUT/0.6V -1 )

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TITLE uob_hep_pc049a_lib

MODULE: pc049a_toplevel
DC-DC CONVERTERS
( 3.3V FOR FPGA , 3.5V FOR MAROC )

A2

MODULE PAGE: 10 OF 11
OVERALL PAGE: 10 OF 14

TOTAL NO. OF SHEETS

REMEMBER:
RESISTORS FOR SSTL VT ( TRIGGER , DATA SIGNALS )
LOOKS LIKE RESITORS ARE *NOT* NEEDED IN SPARTAN6 TO SELECT DIFF TERM VALUE ( FOR LVDS INPUTS )
REFER TO XILINX UG393 FOR DECOUPLING CAPACITOR RECOMMENDATIONS

2.5V = VCCAUX , VCCO(0,1,2) =
(1+1+1+1)*100UF , (2+1+1+1)*4.7UF , (4+2+3+3)*100NF

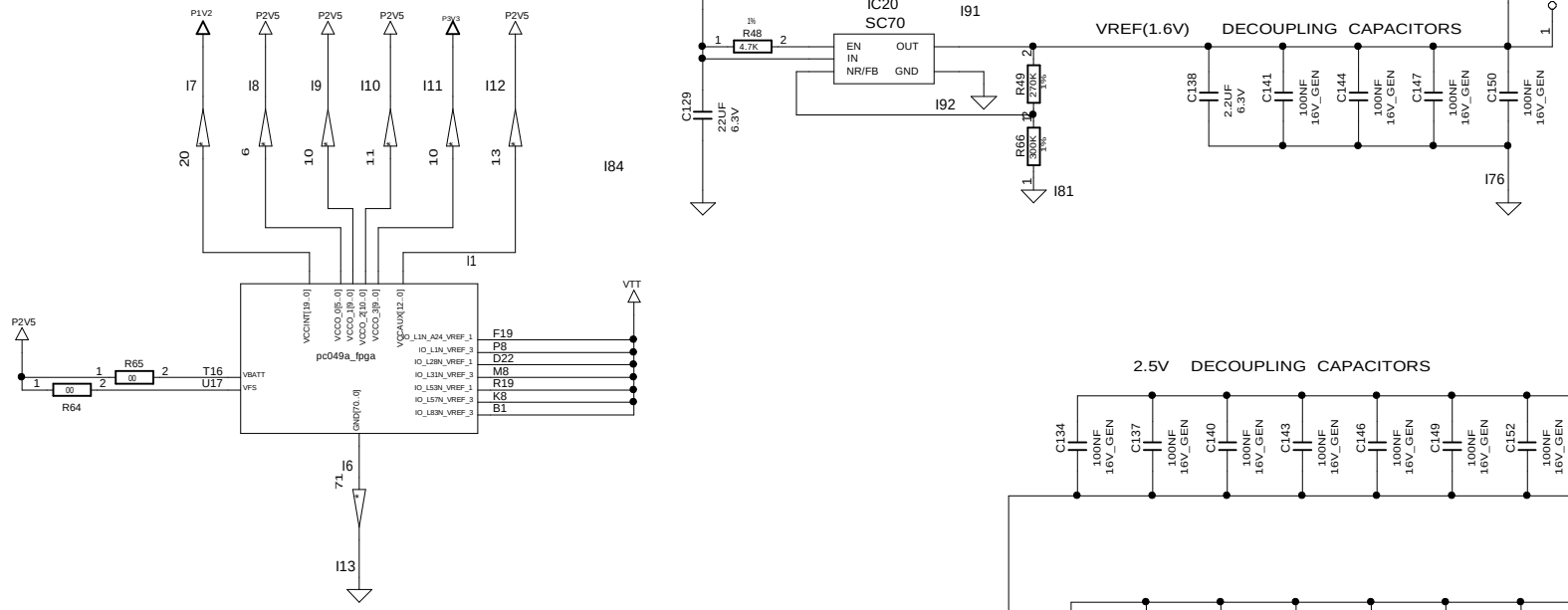
3.3V = VCCO(3) =
1*100UF , 1*4.7UF , 3*100NF

1.2V = VCCINT
2*100UF ,3*3.7UF , 6*100NF

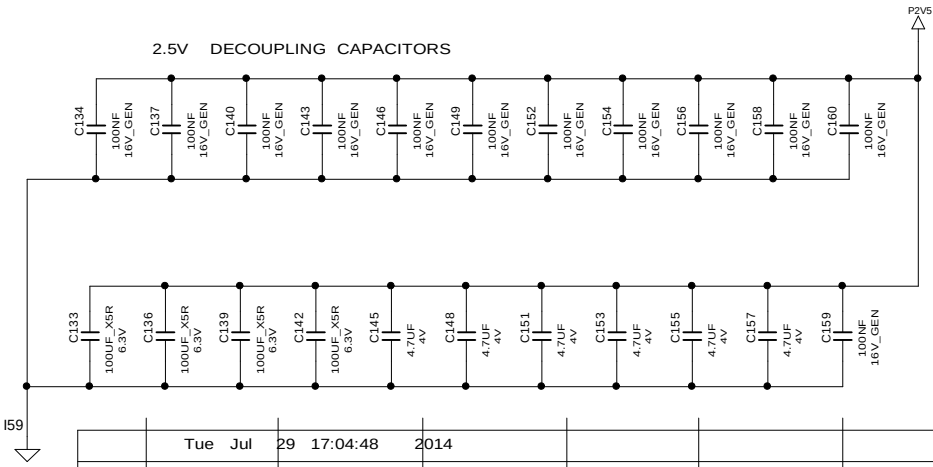
VOUT=0.8(R1+R2)/R2 , R2 ~ 320K
~ 150 DEG-C/W
TPS717XX DROP-OUT ~ 0.24V @ 0.15A
ESR < 1-OHM, COUT > 1UF

tps71701dckrg4
IC20
SC70
TEXAS INSTRUMENTS
I91

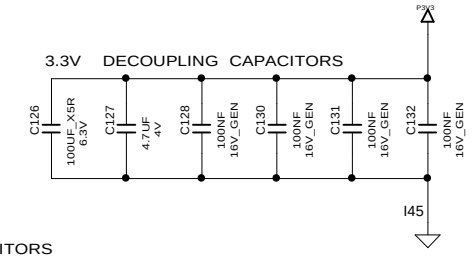
VREF(1.6V) DECOUPLING CAPACITORS



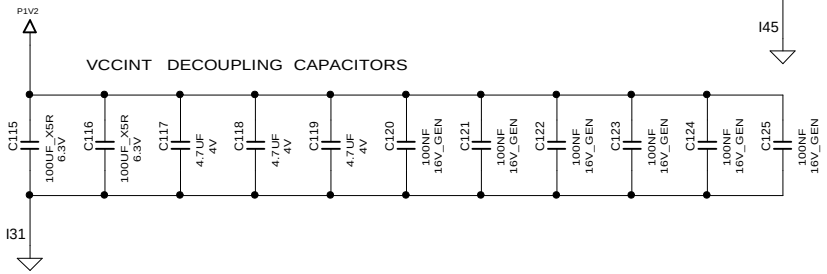

2.5V DECOUPLING CAPACITORS




3.3V DECOUPLING CAPACITORS




VCCINT DECOUPLING CAPACITORS

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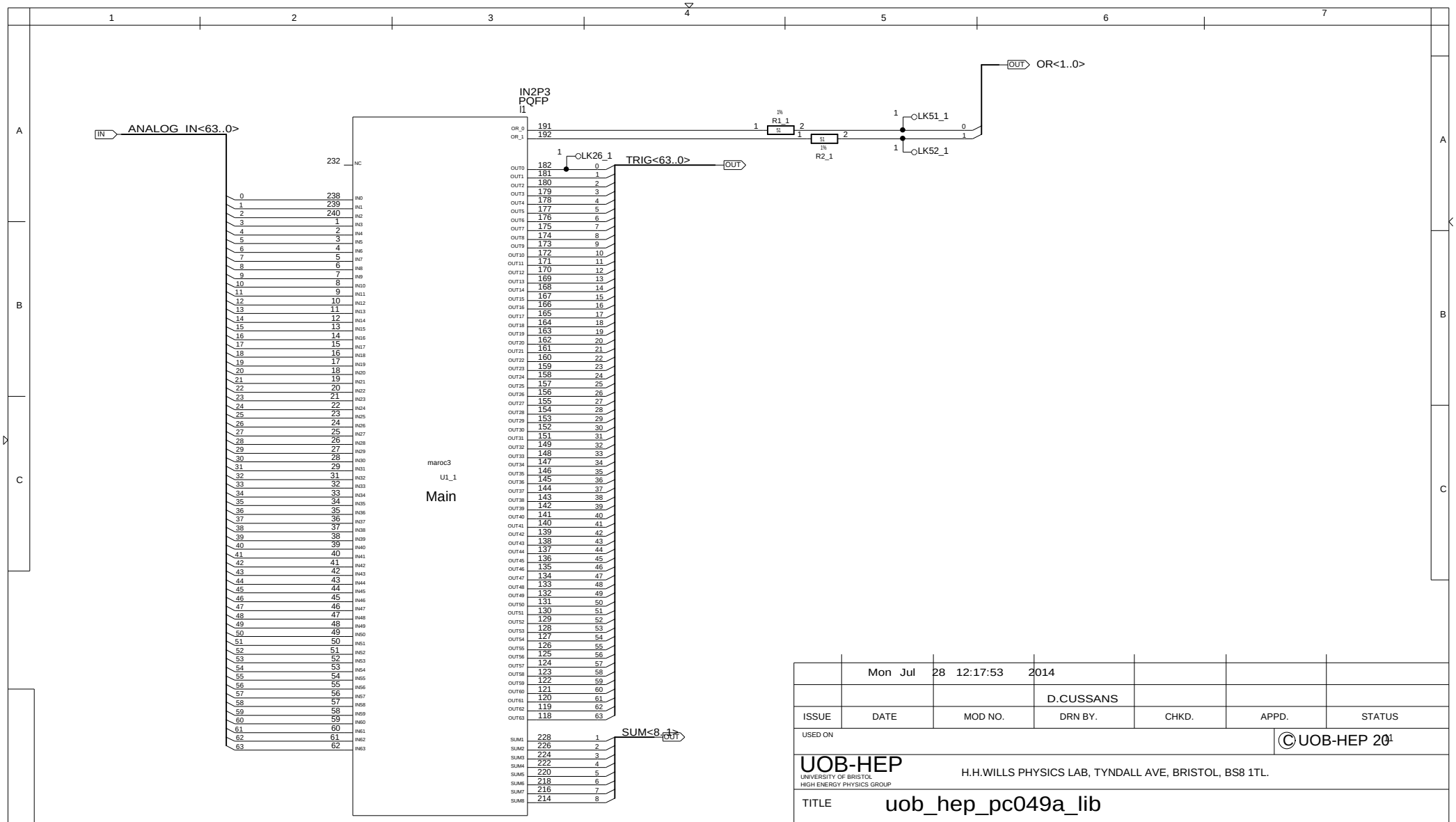
TITLE uob_hep_pc049a_lib

MODULE: pc049a_toplevel
CONNECTIONS TO FPGA POWER PINS
POWER DECOUPLING CAPACITORS

A2

MODULE PAGE: 11 OF 11
OVERALL PAGE: 11 OF 14

TOTAL NO. OF SHEETS




| | | | | | | |
|---|---|---|---|---|---|---|
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TITLE uob_hep_pc049a_lib

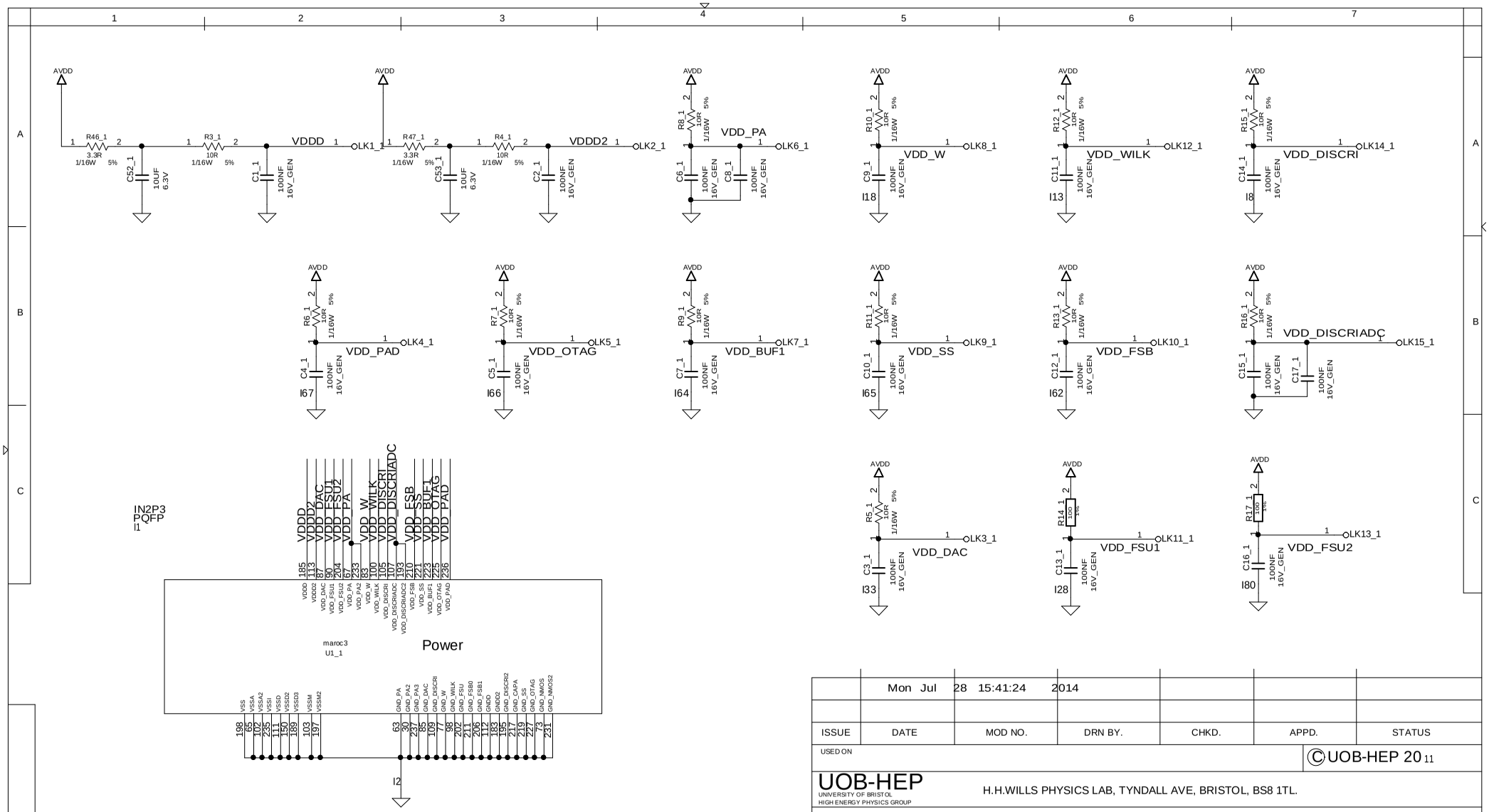
MODULE: pc043c_single_maroc

ANALOGUE INPUTS, TRIGGER OUTPUTS AND SUM OUTPUTS

A2

MODULE PAGE: 1 OF 3
OVERALL PAGE: 12 OF 14

TOTAL NO. OF SHEETS

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TITLE uob_hep_pc049a_lib

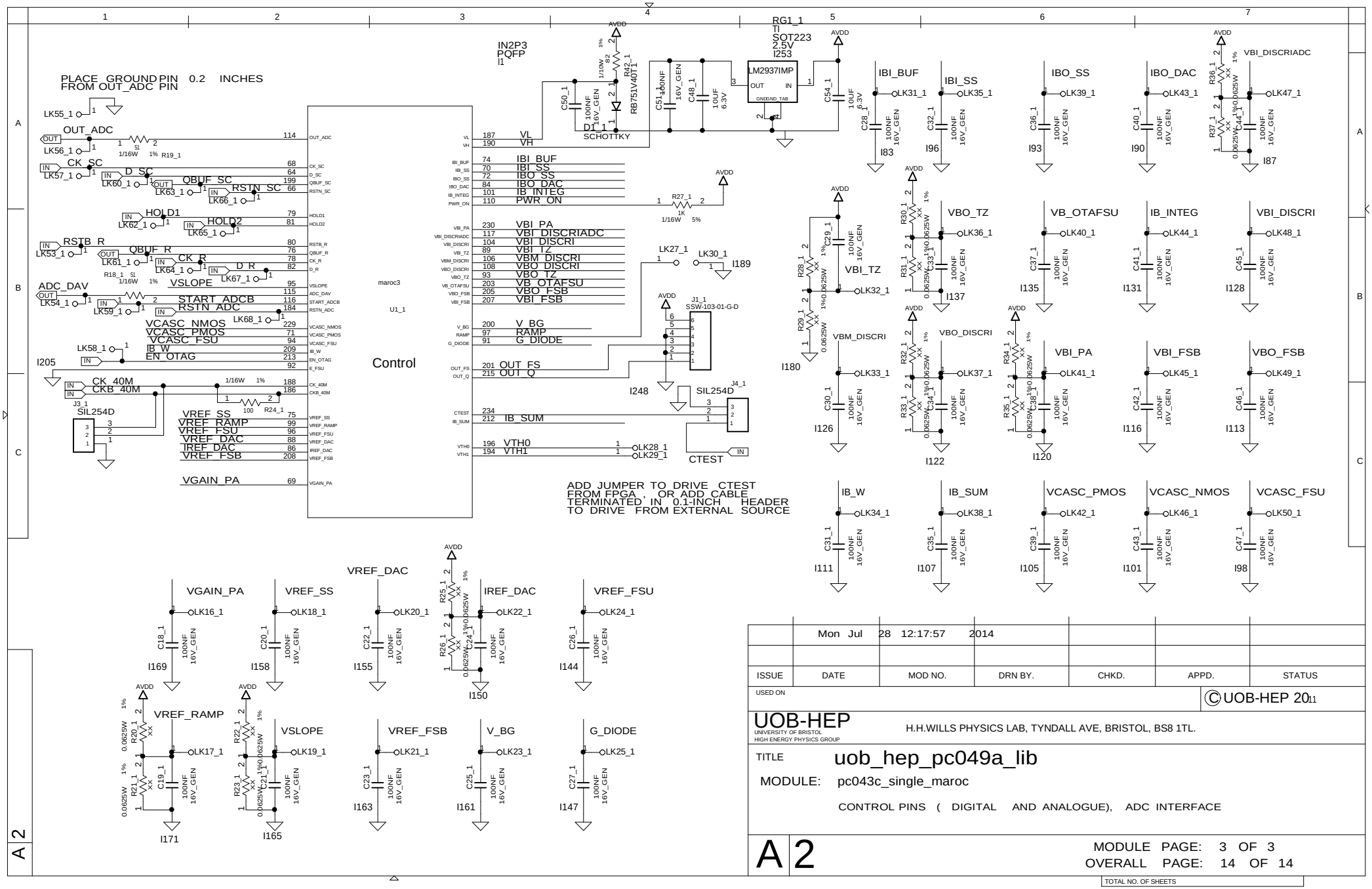
MODULE: pc043c_single_maroc

POWER SUPPLY PINS

A2

MODULE PAGE: 2 OF 3
OVERALL PAGE: 13 OF 14

TOTAL NO. OF SHEETS

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CONTROL PINS ( DIGITAL AND ANALOGUE), ADC INTERFACE

A2

MODULE PAGE: 3 OF 3
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TOTAL NO. OF SHEETS