

# ***NFTC v1.00***

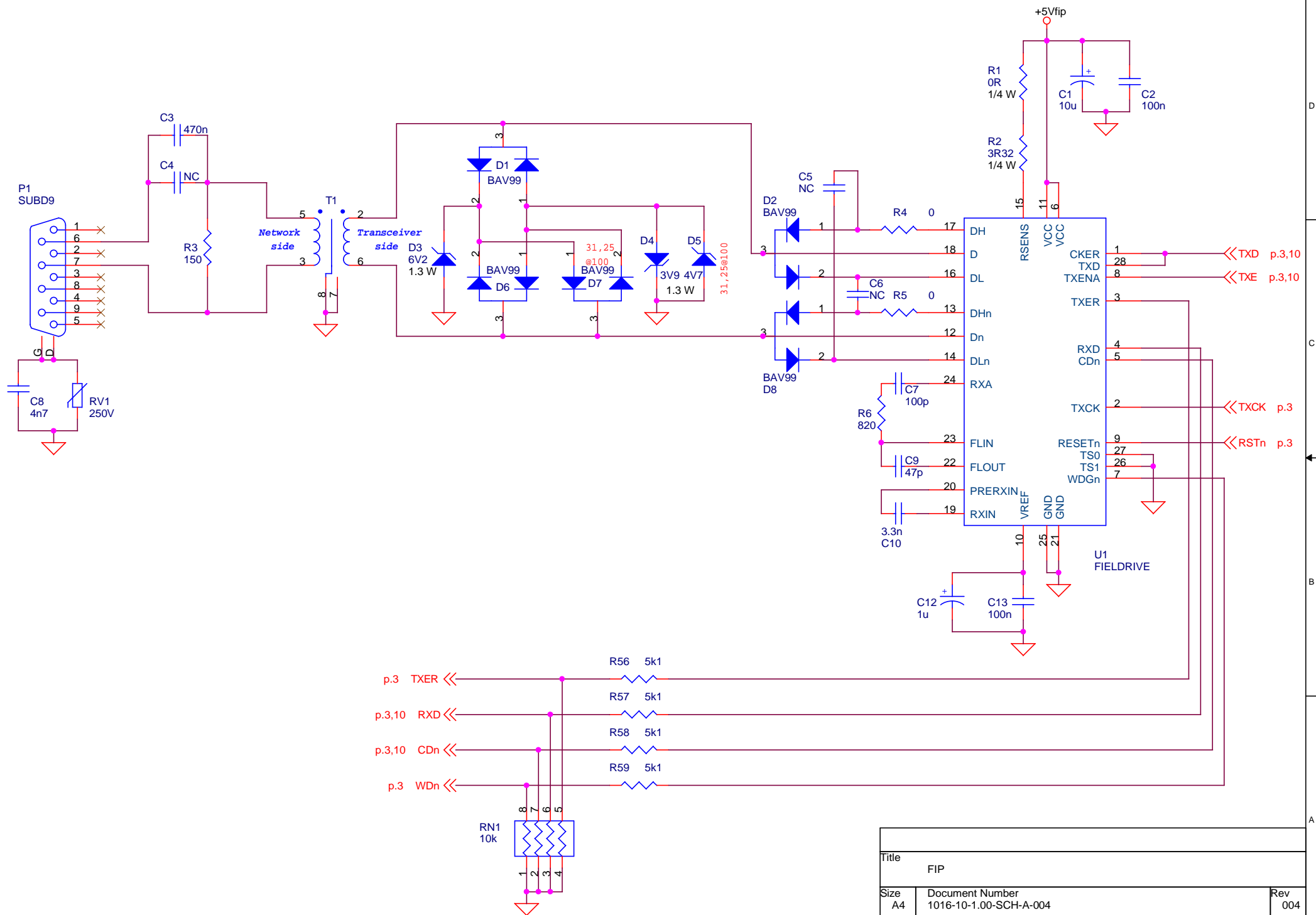
***NanoFIP test board***

**HLP Technologies**

35 rue Tournefort  
75005 Paris

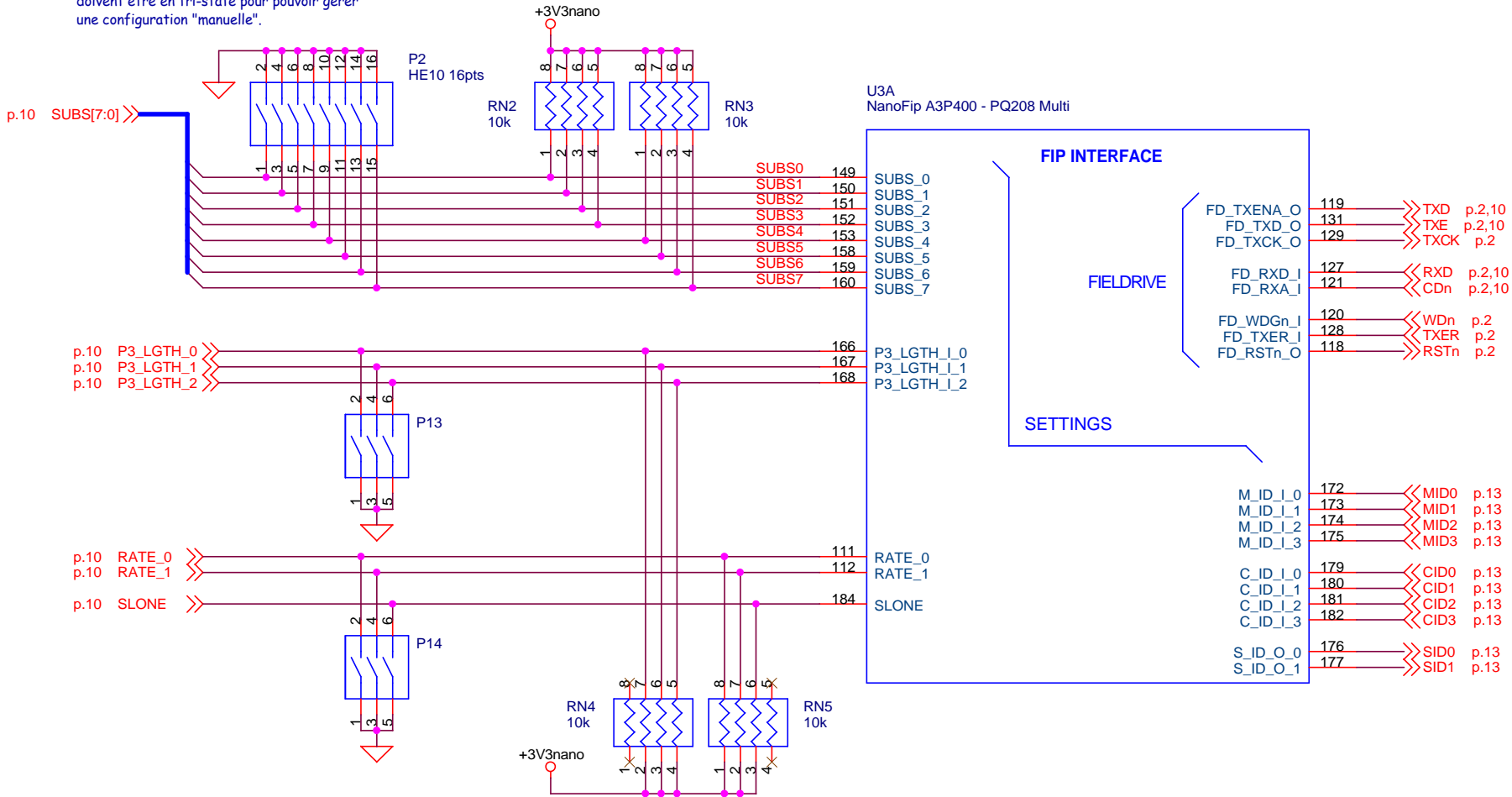
[www.hlp.fr](http://www.hlp.fr)

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Cover		
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FIP		
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Les sorties SUBS du FPGA de controle  
doivent être en tri-state pour pouvoir gérer  
une configuration "manuelle".

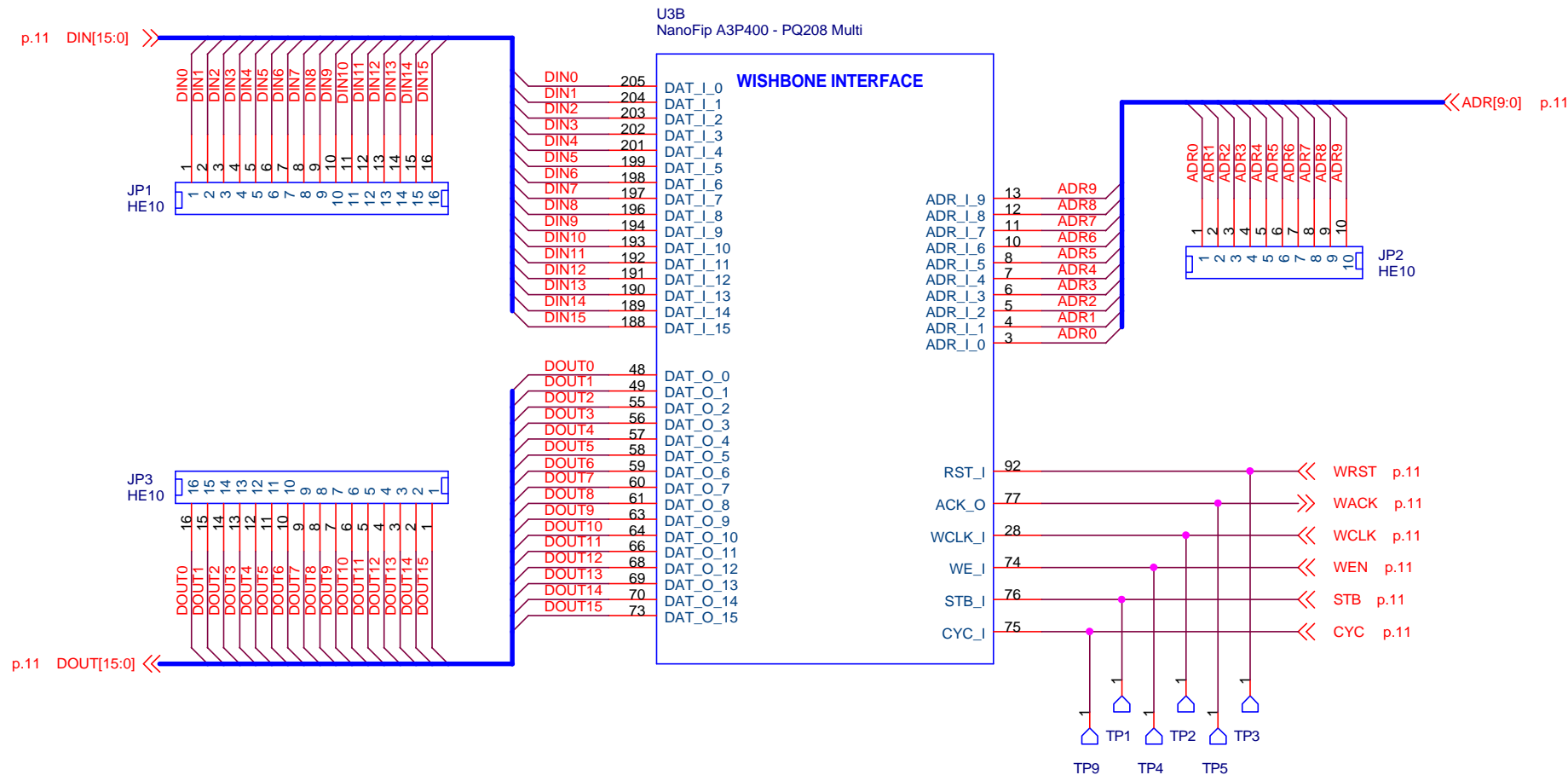


Si l'alimentation du NanoFip est coupée, les entrées  
doivent être à 0.  
Le FPGA de controle doit gérer des sorties tri-state

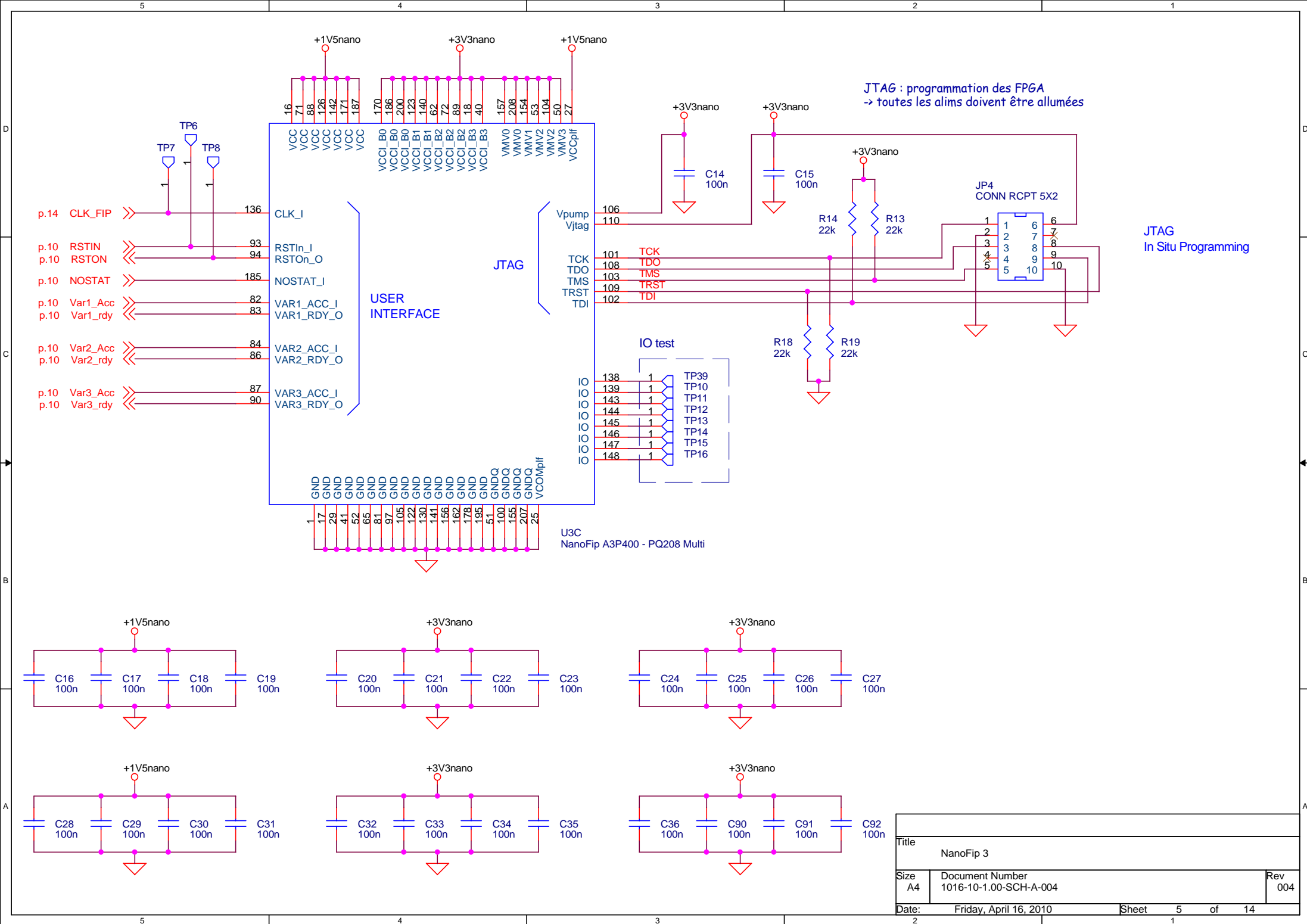
RATE_0	RATE_1	
0	0	31.25 kbps
0	1	1 Mbps
1	0	2.5 Mbps
1	1	reserved

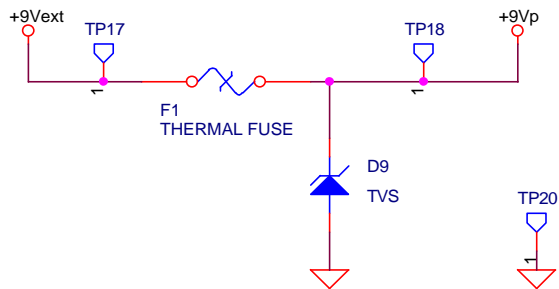
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NanoFip 1		
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Si l'alimentation du NanoFip est coupée, les entrées  
doivent être à 0.  
Le FPGA de controle doit forcer ses sorties à 0

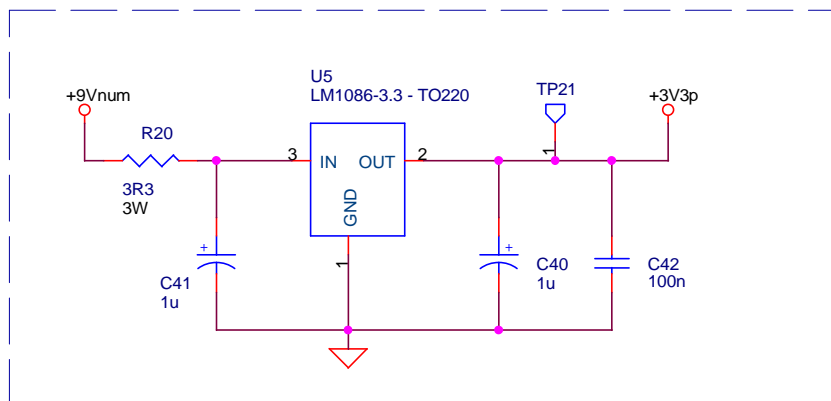


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NanoFip 2		
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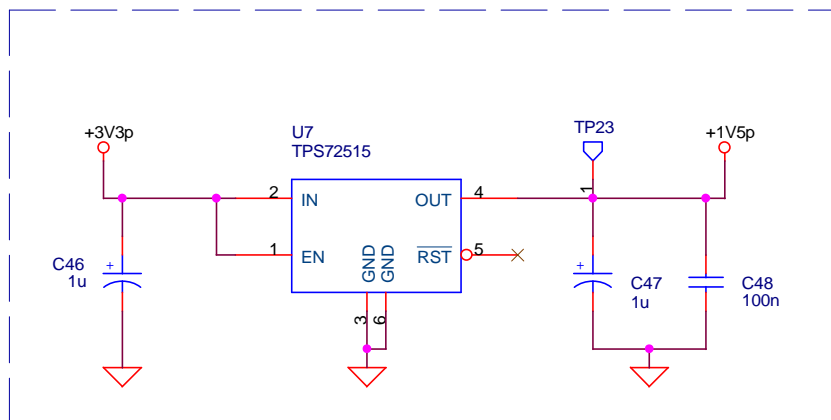




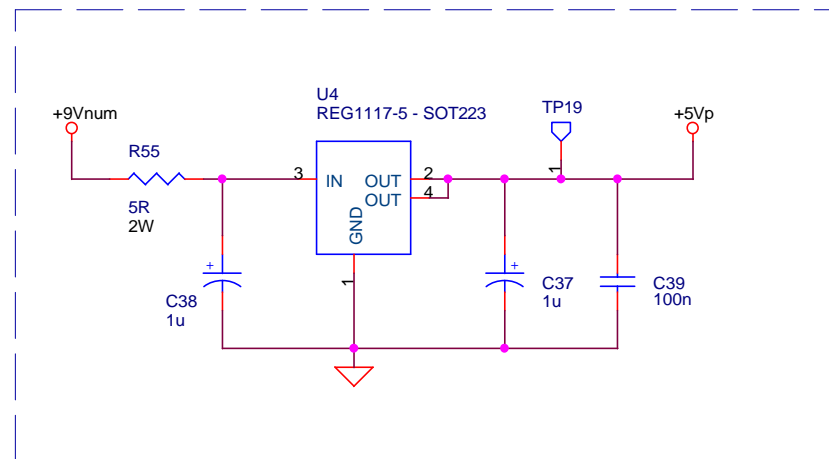
### ALIMENTATION 3V3



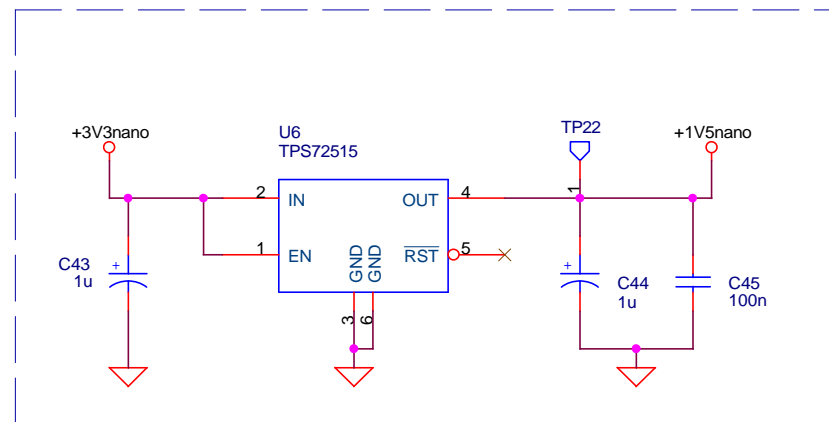
### ALIMENTATION 1V5



### ALIMENTATION 5V

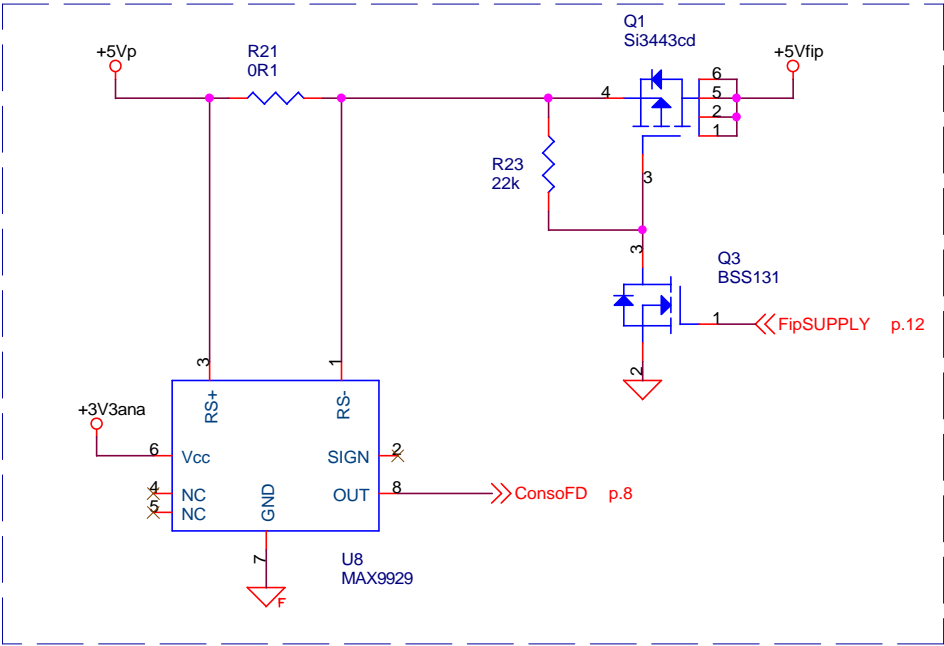


### ALIMENTATION 1V5 (NanoFip)

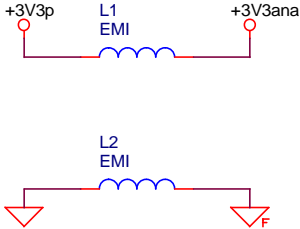
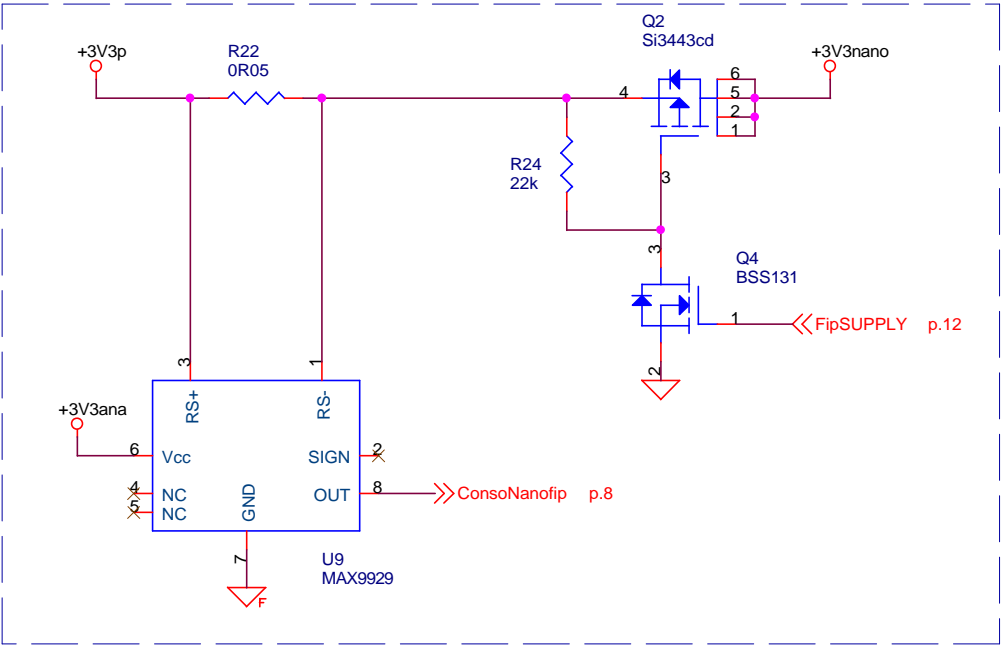


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Alimentation		
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Mesure consommation du Fieldrive



Mesure consommation du NanoFip



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Current sense		
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Q5 Si3443cd

+9Vp

R27 22k

Q7 BSS131

p.10 NF\_PWM

R29 56R

R60 56R

ces pistes font 2mm de large

sur le NanoFip

Q6  
Si3443cd

+9Vp

R28  
22k

Q8  
BSS131

p.10 FD\_PWM

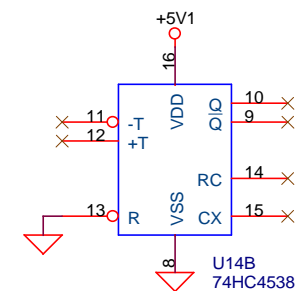
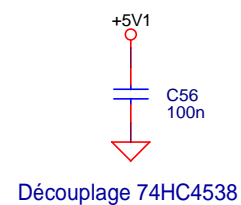
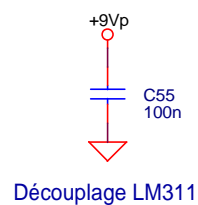
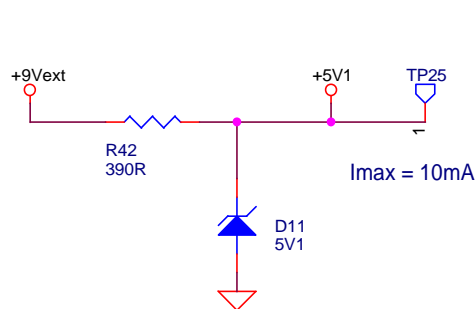
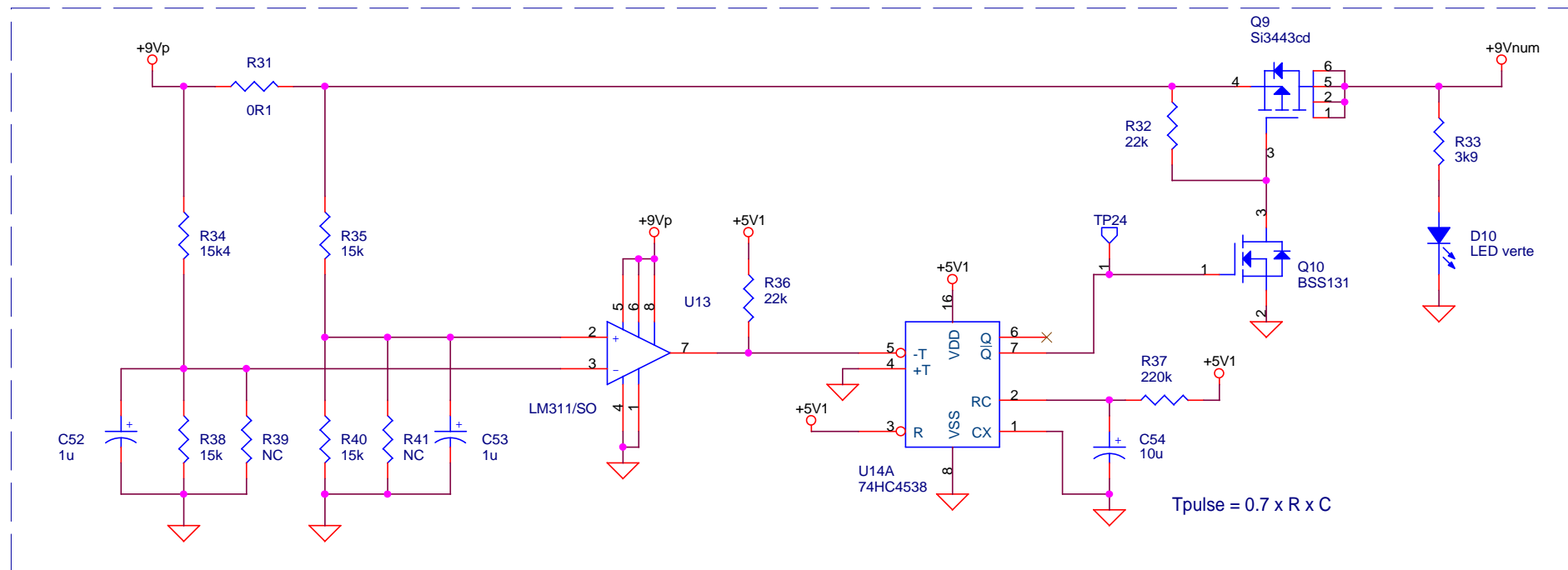
R30  
56R

sur le Fieldrive

Title Temperature management			
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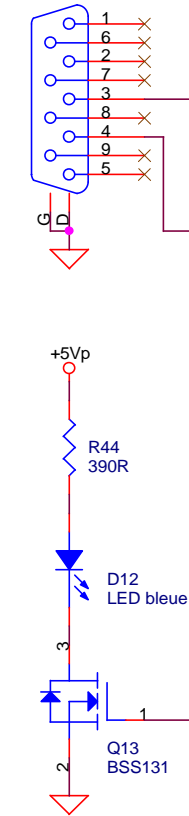
# Protection Latch-up



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Latch-up		
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Les sorties doivent être forcée à 0 si  
l'alimentation 3V3nano est coupée.

P3  
SUBD9

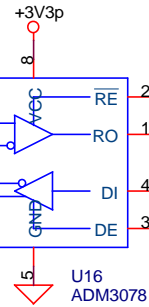


FIP\_activity

p.8,14 I2C\_SCL  
p.8,14 I2C\_SDA

p.5 RSTIN  
p.5 RSTON  
p.5 NOSTAT

p.8 NF\_PWM  
p.8 FD\_PWM

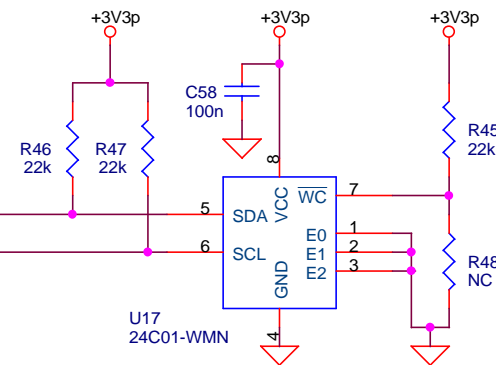


U16  
ADM3078

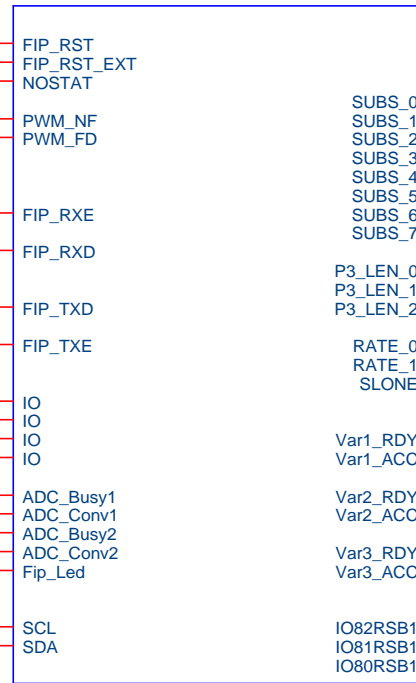
p.2,3 TXD  
p.2,3 TXE  
p.2,3 RXD  
p.2,3 CDn

p.8 Busy\_1  
p.8 Conv\_1  
p.14 Busy\_2  
p.14 Conv\_2

EEPROM serie I2C



U17  
24C01-WMN



SUBS\_0  
SUBS\_1  
SUBS\_2  
SUBS\_3  
SUBS\_4  
SUBS\_5  
SUBS\_6  
SUBS\_7

P3\_LEN\_0  
P3\_LEN\_1  
P3\_LEN\_2

RATE\_0  
RATE\_1  
SLONE

Var1\_RDY  
Var1\_ACC

Var2\_RDY  
Var2\_ACC

Var3\_RDY  
Var3\_ACC

IO82RSB1  
IO81RSB1  
IO80RSB1

U15A  
Actel A3P125 - TQ144 Multi

SUBS[7:0] p.3

SUBS0  
SUBS1  
SUBS2  
SUBS3  
SUBS4  
SUBS5  
SUBS6  
SUBS7

P3\_LGTH\_0 p.3  
P3\_LGTH\_1 p.3  
P3\_LGTH\_2 p.3

RATE\_0 p.3  
RATE\_1 p.3  
SLONE p.3

Var1\_rdy p.5  
Var1\_Acc p.5

Var2\_rdy p.5  
Var2\_Acc p.5

Var3\_rdy p.5  
Var3\_Acc p.5

TP30  
TP31  
TP32

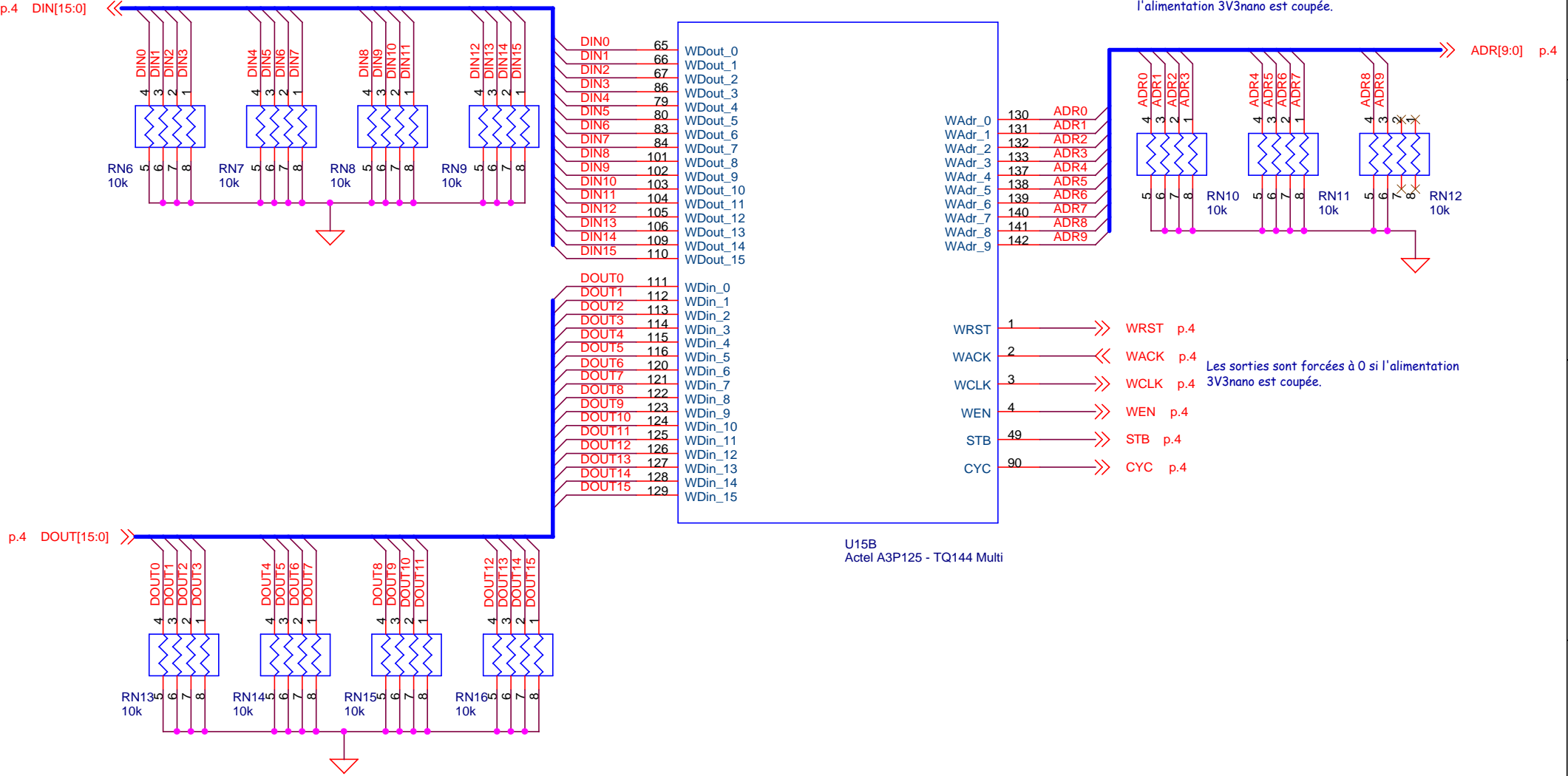
Les sorties doivent être forcée à 0 si  
l'alimentation 3V3nano est coupée.

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FPGA 1		
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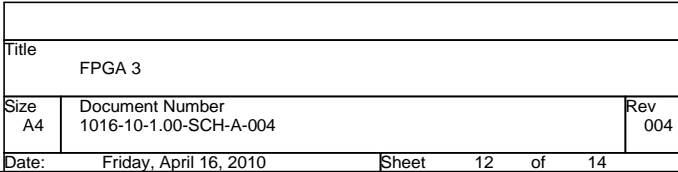
Controle WISHBONE

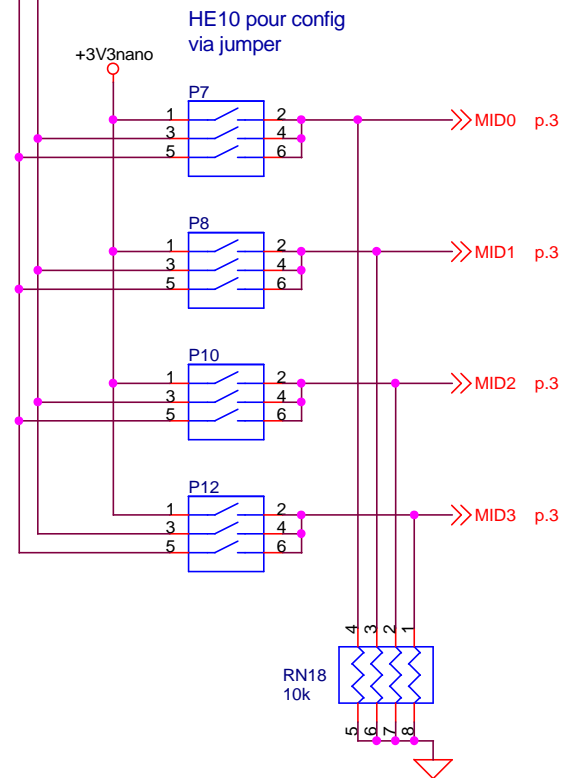
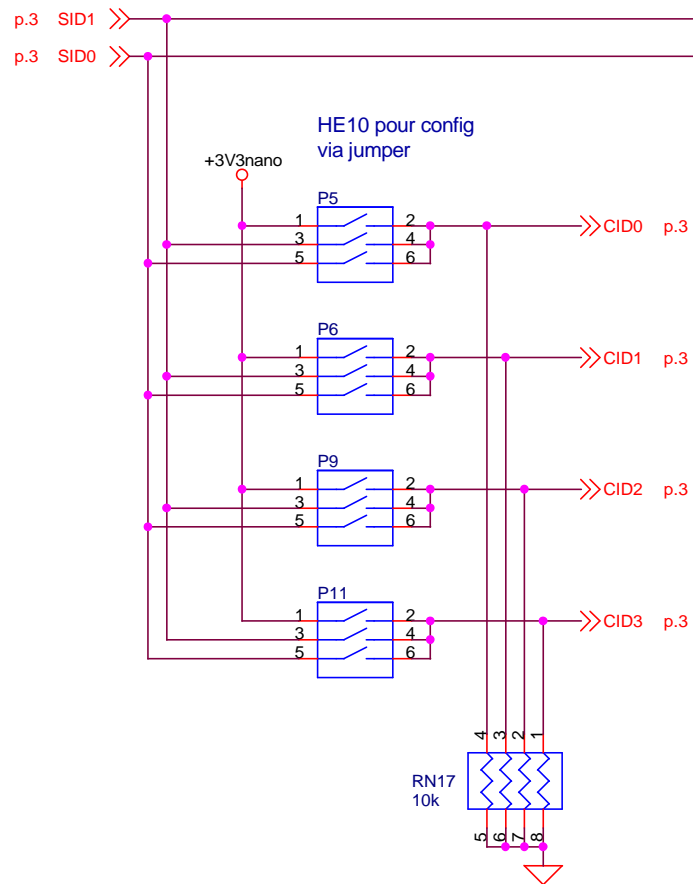
Le bus DIN doit être forcé à 0 si  
l'alimentation 3V3nano est  
coupée.

Le bus ADR doit être forcé à 0 si  
l'alimentation 3V3nano est coupée.



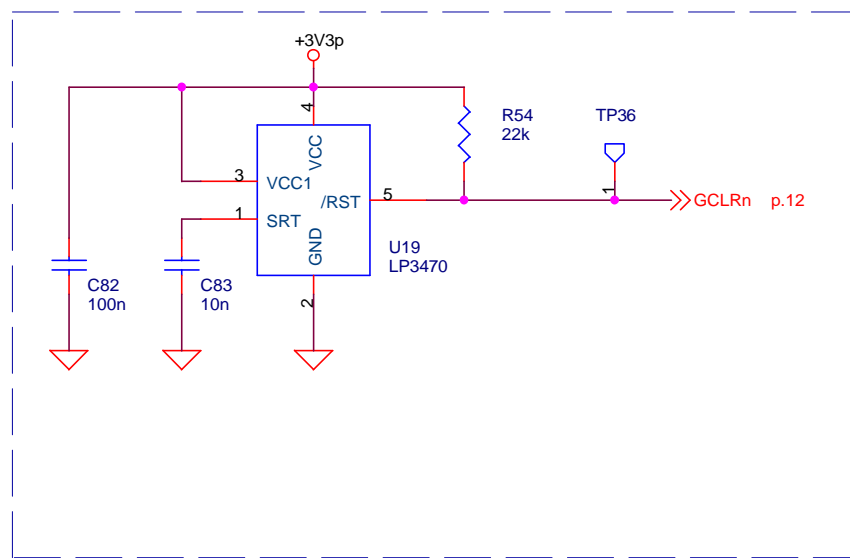
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FPGA 2		
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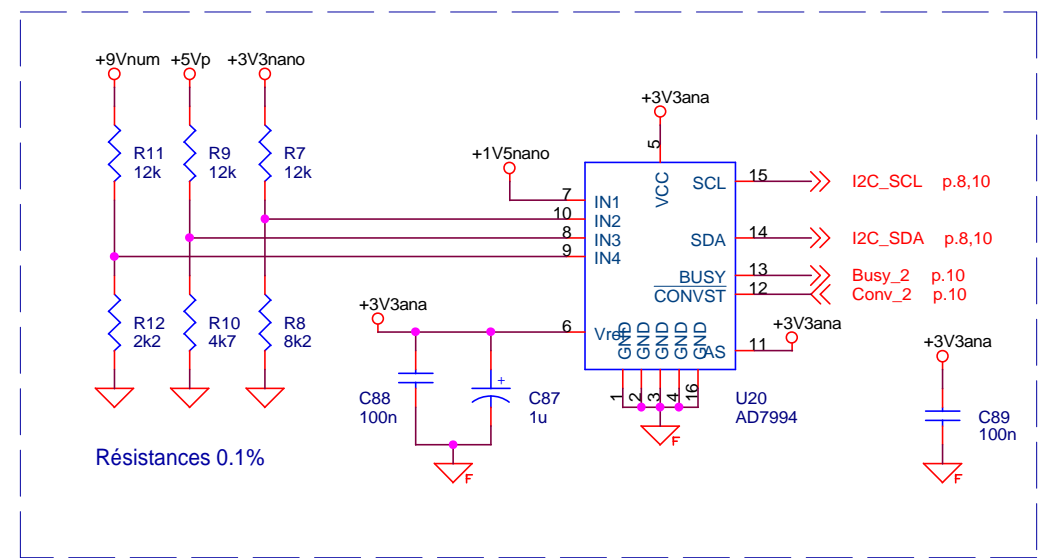


Title		
Configuration		
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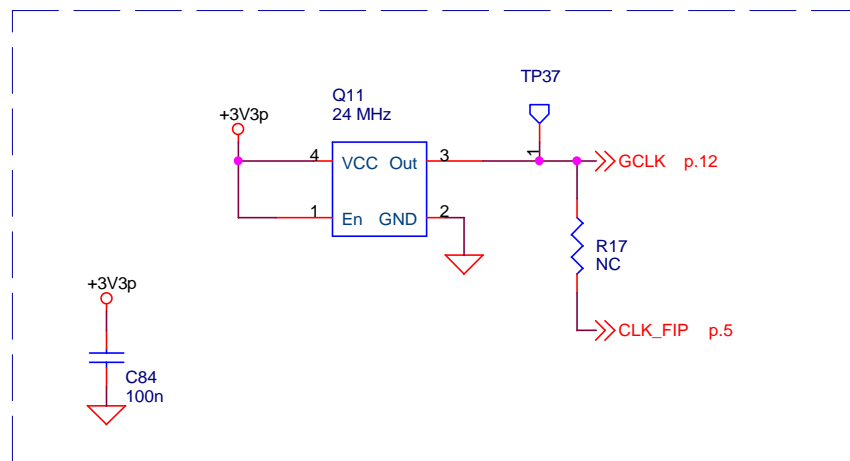
RESET



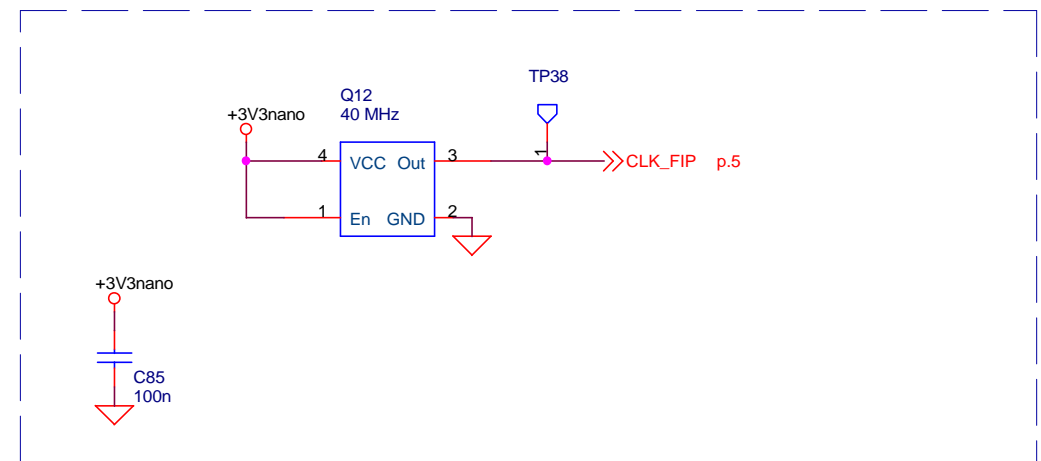
## Mesure des tensions d'alimentation



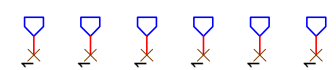
## Horloge FPGA



Horloge NanoFip (40 MHz)



FIX1    FIX2    FIX3    FIX4    FIX5    FIX6



## Percages de fixation

Title Divers			
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