Brandon Hamilton and Alan Langman.

Rhino

Reconfigurable Hardware Interface for computation and radio.
Overview.

- Who are we?
- Objectives and key requirements
- Rhino Hardware
- Rhino Embedded
- Rhino Applications
Acknowledgements.

- Simon Scott and Hayden So
- Students
- CASPER
- University of Cape Town
- MeerKAT project (SKA South Africa)
- SANDF Ledger Project
- OHWR
- Xilinx
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Cape Town, South Africa.
Objective.

To develop an accessible reconfigurable computing platform for software-defined radio teaching and research.
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Back to basics.
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Back to basics.
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Back to basics.
Requirements.

- Low cost hardware and open platform (TAPR/OHL)
- Open Source software (Tools/DSP)
- Easy to learn and use
- Compatible with existing hardware and software (GNU radio)
- Target software-defined radio apps
Reconfigurable devices can be configured to provide the best match for the computational requirements at that specific time, giving much better area – speed – power performance.
Open Hardware solution.
Rhino Architecture.

FPGA
Spartan-6
XC6SLX150T

FPGA Processor Bus

ARM Processor
ARM Core
Texas Instruments AM3517

Micron
Rhino Architecture.

- FPGA
- Spartan-6 XC6SLX150T

- Xilinx XC6SLX150T
  - 676-pin package
  - 150,000 logic cells
  - 180 DSP48A1 slices (up to 300MHz)
  - 8 GTP transceivers
  - 4 integrated DDR3 Memory Controller Blocks
Rhino Architecture.

- **Micron DDR3-1066**
  - 512MB capacity
  - 25.6Gbps total bandwidth
- **Spartan-6 XC6SLX150T**
- ARM Core
- Texas Instruments AM3517
Rhino Architecture.

FPGA

FPGA Processor Bus

ARM Processor
ARM Core
Texas Instruments AM3517

FMC connectors for ADC and DAC cards
Supports 2 cards
Rhino Architecture.

- FPGA: Spartan-6 XC6SLX150T
- Processor: ARM Core
- Texas Instruments AM3517
- Processor Bus
- 2 CX4 10Gbps Ethernet connectors
- Supports copper-to-fibre adaptors
Texas Instruments AM3517ZCN
491-pin package
600MHz ARM cortex-A8 core
Many integrated peripherals (USB, Ethernet, HD video output)
Rhino Architecture.

- **FPGA**
  - Spartan-6
  - XC6SLX150T

- **Processor Bus**

- **ARM Core**

- **Memory**
  - 256MB NAND flash memory

- **Storage**
  - Storage for bootloader and OS

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Rhino Architecture.

FPGA

Spartan-6
XC6SLX150T

ARM boots from USB drive or SD card
2 USB host ports
JTAG over USB

ARM core
Texas Instruments AM3517
Rhino Architecture.

FPGA

Spartan-6
XC6SLX150T

100Mbps Ethernet
Supports IEEE1588
Precision Time Protocol
Sync board within 10ns
Rhino Architecture.

FPGA
Spartan-6
XC6SLX150T

FPGA Processor Bus
16-bit data bus
1.3 Gbps

Texas Instruments AM3517
FMC.

- Well-specified standard
  - Electrical interfaces, mechanical and thermal requirements
- Dedicated I2C lines for control
- Lots of commercial off-the-shelf ADC/DAC
- FMC-to-ZDOK+ adaptor (CASPER cards)
- FMC-to-Ettus radio board controllers
Commercially Available.
CERN FMC ADC 100M 14b 4cha.

- 4 Channel ADC
- 100 MSPS
- OHWR
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Model.
Model (with Enclosure).

- FMC-to-ZDOK+ adaptor
- ZDOK ADC card
- FMC ADC/DAC card
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Manufactured.
Making Rhino Comfortable.
BORPH.

- Berkeley Operating system for ReProgrammable Hardware

OS for reconfigurable computers
- Treats reconfigurable hardware as computational resources

UNIX interface to HW designs
- Familiar to SW and HW engineers
- Design language independent
BORPH.

- Abstraction layer
  - Portability
  - Usability
- UNIX process model
  - HW becomes an active entity
- Focus on application, rather than low level implementation details
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BORPH.

SW Process
CPU

HW Process
FPGA

BORPH
Device configuration.

**BORPH Object File (BOF)**
- HW executable
- Analogous to SW ELF executable

```bash
1:bash$ ./my_design.bof
system("./my_design.bof")
```
Device I/O.

- Virtual File System (IOREG)
  - Interface to the running HW process
  - Access to device registers
  - Generic (Language independent)

```bash
1:bash$ cp /proc/1337/hw/ioreg/MYREG ~/
memfile = fopen("/proc/1337/hw/ioreg/MYREG", "r");
fread(buf, 4, 1, memfile);
```
Portability.

- Platform specific functions
  - Configuration
  - Unconfiguration
  - Read from device
  - Write to device

Linux Kernel (3.1)

BORPH

- BOF Binary format
- Proc filesystem extension
- Exec threads

Platform Specific

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Remote Development.
Gateware Infrastructure.

- Support open standards (wishbone)
- Common architecture with open hardware
- Support for
  - Etherbone (ethernet to wishbone)
  - ARMbone (GPMC to wishbone, ICAP)
  - Wishbone serializer core (CX4)
  - DSP Pipeline wishbone dataflow mode
Rhino Radar.
Rhino Radar Integrated.
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Radio Astronomy.
Conclusions.

- Motivation and history of Rhino
- Open Hardware!
- Approximately 1 year from concept to pre-production unit
- Available from Digicom ($2000)
- Easy to use interface for user
- Grow the user community
Thanks.

www.rhinoplatform.org