Open Hardware at CERN

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BE-CO Hardware and Timing section
CERN, Geneva, Switzerland

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Outline

1. Introduction
2. Open Hardware products
3. Gateware architecture
4. Tools and concepts
5. Future work & conclusions
## CERN Beams Controls group

### Responsible for
- Specification, design, procurement and operation of electronic modules
- Linux device drivers, C/C++ libraries, test programs

### Hardware kit
- Analog and digital I/O
- Level converters, repeaters
- Serial links, timing modules

### Currently, October 2013
- About 120 module types
- Most are custom designed: only 1 in 4 is commercial
Need for a new hardware kit

Motivations
- Obsolete components/modules → can’t build/buy
- Limited stock → no new installations
- Incomplete/nonexistent documentation

New approach
- Open and modular designs
- Compliant with existing standards

Carrier-mezzanine concept
- Only one complex design per platform (carrier)
- Reduce number of supported modules
Use of standards

Based on standards
- Platform bus: VME, PCI, PCIe, PXIe
- FMC (FPGA Mezzanine Card, ANSI/VITA 57.1)
- Wishbone FPGA internal bus
- Linux device drivers

Contribute to standards
- FMC bus Linux driver structure: in Linux v3.11
- ZIO Linux framework for DAQ and CTL hardware: RFC made to Linux Kernel list
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Open Hardware products

More than just a board
- Hardware board
- FPGA gateware
- Linux driver
- Production test system

Carriers
- Three fully supported (VME, PCIe, PXIe)
- Six other carriers (VXS, AMC, stand-alone)

Mezzanines
- Four fully supported (ADC-100M, TDC, DIO-5ch, Delay)
- About a dozen other mezzanines (ADC, DAC, DDS, DIO)
SVEC - Simple VME FMC Carrier
Commercialised in Germany
SPEC - Simple PCI Express FMC carrier
Commercialised in Spain, The Netherlands & Poland
SPEXI - Simple PXI Express FMC carrier
A modified SPEC board
FMC mezzanine: 5-channel 1ns TDC
A joint development by TE/ABT, TE/CRG & BE/CO
FMC mezzanine: 100 MSPS 14-bit 4-channel ADC
<table>
<thead>
<tr>
<th>Project</th>
<th>Producers</th>
<th>Users</th>
<th>Produced</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPEC carrier - PCIe</td>
<td>3</td>
<td>41</td>
<td>300</td>
</tr>
<tr>
<td>SVEC carrier - VME</td>
<td>2</td>
<td>4</td>
<td>105</td>
</tr>
<tr>
<td>SPEXI carrier - PXIe</td>
<td>1</td>
<td>2</td>
<td>(proto) 3</td>
</tr>
<tr>
<td>ADC 100M 14b 4ch</td>
<td>2</td>
<td>11</td>
<td>70</td>
</tr>
<tr>
<td>TDC 1ns 5cha</td>
<td>1</td>
<td>3</td>
<td>70</td>
</tr>
<tr>
<td>FMC DEL 1ns 4cha</td>
<td>3</td>
<td>4</td>
<td>108</td>
</tr>
<tr>
<td>FMC DIO 5ch</td>
<td>3</td>
<td>10</td>
<td>92</td>
</tr>
<tr>
<td>WR switch 18 ports</td>
<td>1</td>
<td>11</td>
<td>77</td>
</tr>
</tbody>
</table>

**Table:** eight CERN OH designs found producers and users
Gateware architecture

Wishbone for modularity

- Open standard
- Simple, uses few FPGA resources
- Collection of cores already available (OpenCores)

New cores developed

- At CERN: VME64x, PCIe, DDR3
- By collaborators: Wishbone crossbar (GSI)
Example: FMC-ADC gateware architecture
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## Gateware design tools

### hdlmake: Automating HDL design flow
- Generates Makefiles for synthesis and simulation.
- Project structure described in Manifest files.
- Solves dependencies (fetches remote ones).

### wbgen2: Wishbone slave generator
- Describes structure in a single text file.
- Automatically generates HDL source, C header and documentation.
- Generates registers, RAM, FIFO, interrupt controller.

Both FOSS tools available on ohwr.org
## wbgen2: HTML documentation example

**HW prefix:** example_csr

**HW address:** 0x0

**C prefix:** CSR

**C offset:** 0x0

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<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
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<td>LED_RED</td>
<td>LED_GREEN</td>
<td>SYS_PLL_LCK</td>
<td>FMC_PRES</td>
<td>PCB_REV[3:0]</td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

- **PCB_REV** [read-only]: PCB revision
  - Binary coded PCB layout revision.
- **FMC_PRES** [read-only]: FMC presence
  - 0: FMC slot is populated
  - 1: FMC slot is not populated.
- **SYS_PLL_LCK** [read-only]: System clock PLL status
  - 0: not locked
  - 1: locked.
- **LED_GREEN** [read/write]: Green LED
  - Manual control of the front panel green LED (unused in the fmc-adc application)
- **LED_RED** [read/write]: Red LED
  - Manual control of the front panel red LED (unused in the fmc-adc application)
- **RESERVED** [read-only]: Reserved register
  - Ignore on read, write with 0's.
- **TYPE** [read-only]: Carrier type
  - Carrier type identifier
  - 1 = SPEC
  - 2 = SVEC
  - 3 = VFC
  - 4 = SPAXI
Testing environment

Production test systems

- Automated production tests.
- Software framework to develop & run tests (Python).
New concepts

SDB: Self Describing Bus

- Allows software to know about gateware architecture
- Series of predefined structures
- Contains meta-data about HDL cores
  - Vendor & device ID, version, address range
Example: SDB record (VHDL)

```vhdl
constant c_ONEWIRE_SDB_DEVICE : t_sdb_device := (
    abi_class => x"0000",
    abi_ver_major => x"01",
    abi_ver_minor => x"01",
    wbd_endian => c_sdb_endian_big,
    wbd_width => x"4",
    sdb_component => (
        addr_first => x"0000000000000000",
        addr_last => x"0000000000000007",
        product => (
            vendor_id => x"000000000000CE42",
            device_id => x"00000602",
            version => x"00000001",
            date => x"20121116",
            name => "WB-OneWire.Control "))));
```
Example: SDB records in Wishbone crossbar
New concepts

SDB File System

- Based on SDB data structures
- Easy to parse (e.g. for embedded processor)
- Library and tools available (generate, parse)
- Used in an EEPROM on each mezzanine
  - Mezzanine identification (type, serial number)
  - Calibration data
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Future work

Consolidate our designs
- Consolidate documentation (starter guides, ...).
- Continue to transfer knowledge to companies.

Future platform
- Current platform limitations
- Ready for a new platform
  - Re-useable mezzanines set
  - HDL and software framework ready
Conclusions

CERN’s FMC kit is not only a set of hardware modules.
- Collection of HDL cores
- Linux device drivers, libraries and test programs
- Production test systems
- Tools and concepts

Using standards improves re-usability.

Eight CERN designs are already commercialized.

New users and collaborations are welcome.

Four years of experience show it works!
Open products are real products™

Want to know more? Take a tour on ohwr.org