Libre-FDATool Official Kickstart

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(presented by Tomasz Wlostowski)

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Outline

1 Motivation
2 Requirements
3 Dependencies
4 HDL Verification
5 Roadmap
6 Demo
7 Get Involved!
The Libre-FDATool inception

The idea of Libre-FDATool emerged at the CERN Open Hardware Repository. The program aims to help in design of DSP blocks used in many Open Hardware projects.

Libre-FDATool is a free/libre program for analysis and design of HDL digital filters from their high-level specifications.

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The Idea

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Definition

Libre-FDATool is a free/libre program for analysis and design of HDL digital filters from their high-level specifications.
Why Libre-FDATool?

Digital filters are ubiquitous in FPGAs and are the base for a multitude of applications, from telecommunications, through control and measurement systems, to sound/video processing.

Non-Recurring Engineering (NRE)
Coding a VHDL filter by hand is straightforward but a time-consuming task, which increases the cost of the project. Automated tools increase productivity.

No FOSS software
The only alternative with similar features is the proprietary FDATool (part of Matlab DSP toolbox).
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**Blueprint (I)**

<table>
<thead>
<tr>
<th>Motivation</th>
<th>Requirements</th>
<th>Dependencies</th>
<th>HDL Verification</th>
<th>Roadmap</th>
<th>Demo</th>
<th>Contact</th>
</tr>
</thead>
</table>

**Libre-FDATool**

 выпускается под лицензией GPLv3 (или более поздней версии).

Pythoн

Python становится фактическим открытым стандартом для научных расчетов и анализа данных в большинстве исследовательских институтов.

Libre-FDATool будет поддерживать версии Python 2 и 3 и соответственно связанные пакеты.

**User-friendly graphical interface**

Мы стремимся сделать Libre-FDATool простым для использования, поэтому разработка удобной и удобной GUI обязательна. Мы выбрали библиотеки QT/PyQt для этой цели.

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Free as in freedom

Libre-FDATool is released under the GPLv3 (or later).
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Written in Python
Python is becoming the de facto open standard for scientific calculations and data analysis in most research institutes. Libre-FDATool will support Python versions 2 and 3 and respective associated packages.
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User-friendly graphical interface
We aim to make Libre-FDATool easy to use, so developing a nice and handy GUI is a must. We chose the Qt/PyQt libraries for that purpose.
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Dependencies

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Blueprint (II)

We will support as many OSes as possible (at least: Linux, Windows, OSX)

Multiple HDL support

Verilog and VHDL code generation, with emphasis on readability of the generated code (including testbenches).

Multiple ways of describing filters

Multiple LTI system definitions (FIR and IIR) from high level specs, including cutoff frequencies and gains, ripple, windows, maximum order, etc.

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Blueprint (III)

Variety of filter structures

Easily expandable set of configurable structures for each filter (Direct/Transposed Forms, Linear Phase, Parallel, Cascade, CIC-Compensator, Distributed Arithmetic, etc.).

Simulation

The tool must be able to simulate a full DSP chain. This includes filtering a signal in floating point, Python-modeled hardware and using external simulators for verifying the generated HDL.

Analysis

Built in graphical analyzer of the theoretical and quantized filters (transmittance, poles-zeros, group delay).
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Signal stimulus wizards

The test signals are generated using wizards (chirp, sine, square, sawtooth, impulse, step, etc.).

Signal import/export

Importing stimulus signals from files (waveform, CSV) as well as exporting the filtered ones.

Advanced scope

Variety of methods for graphical analysis of stimulus and filtered signals, such as value vs time, power estimation, error, FFT, etc.
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- NumPy
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- NumPy
- SciPy
- matplotlib
Specific EDA Software

In order to verify the generated HDL, third-party Open EDA tools can be used. Currently supported tools include:

- Verilog and VHDL simulation
- VHDL simulation
- VCD waveform graphical viewer

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- **GHDL**
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  VCD waveform graphical viewer
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Motivation for testing

We can simulate the filters from inside Libre-FDATool, but this is not enough to fully validate the generated HDL code. We need to cross check expected vs. experimental outcomes.

Maximum relative speed for each of the filter structures

Explore the resources needed for different structures

All-programmable SoCs

The new generation of SoCs that puts together embedded processors with an integrated FPGA facilitates quick HW validation of HDL cores.

Run Libre-FDATool on the CPU in an embedded OS

Deploy the synthesized HDL Filter as an IP-Core in the FPGA

Stimulate the IP-Core input and capture the output signal
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Reference Hardware Platform

Xilinx’s Zynq powered Zedboard

- Dual Core ARM Cortex-A9
- Xilinx 7 Series FPGA
- Flexible ADC
- Multimedia interfaces
- It’s Open-Hardware!
Reference Embedded Operating System

Linaro: Linux on ARM

As the reference embedded Operating System, Linaro has been selected:

- Optimized for ARM architectures
- Ubuntu based Linux distribution
- Open Project
- Big community
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Currently we support only a limited set of filter structures. We want to cover as many as possible.

Export/Import capability

We are working on the import/export functionality for test signals, including PCM waveforms.

Report Generation

We plan to support extensive report generation, including speed and resource estimation.
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Roadmap (II): Planned Improvements

- Interface with proprietary tools
- Despite the fact that Libre-FDATool is a free tool, we are interested in integrating it with mainstream proprietary tools by:
  - Supporting proprietary simulators (Modelsim, Cadence, etc.)
  - IP block generation for Electronic System Level tools

- Target Optimization
- Platform-specific code optimizations targeted to efficiently use the resources that state-of-the-art FPGAs offer:
  - DSP slices
  - Embedded RAM Blocks
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Libre-FDATool in action

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Get involved in Libre-FDATool

Keep in touch

If you are interested in Libre-FDATool or want to join the development team, just take a look at the official Libre-FDATool project site:

Libre-FDATool on CERN’s Open Hardware Repository

http://www.ohwr.org/projects/libre-fdatool

Thank you!