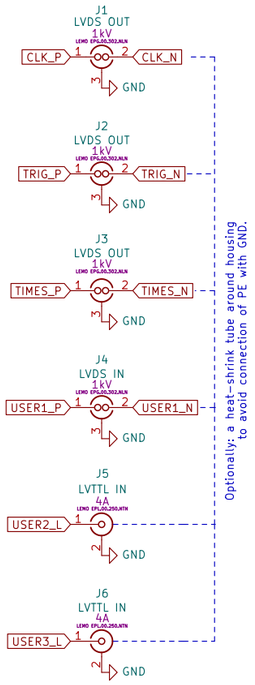
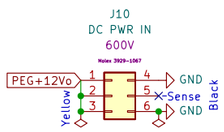
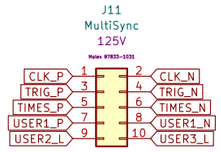
FRONT-END

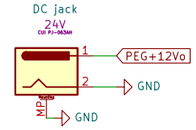


BACK-END



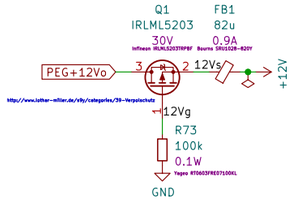


4xLVDS (1-2, 3-4, 5-6, 7-8)
2xLVTTL (9, 10)
Flat cable:
- Amphenol 191-2815-010
- 2x Molex 87568-1074

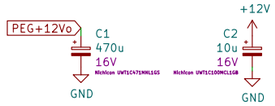


Alternative power supply connector

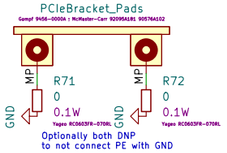
POWER MANAGEMENT



DECOUPLING



MOUNTING

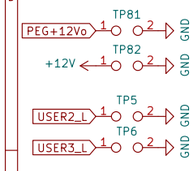


FID1
BoardOutline

FID2
Logo KiCAD

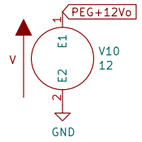
FID3
Logo Trash

TESTING



SPICE SIMULATION

```
.control
version
.endc
.tran 0.5n 1.7u
```



NOTES

Layer buildup is ML4-1mm. PCB thickness: 1mm
GND - LVDS isolation height: 0.232 mm
All LVDS are length and skew-matched to 100mm, but not the TTL.
Trace edge-coupled surface microstrip width: 0.25 mm, gap: 0.20 mm, height: 0.035mm
https://eu.beta-layout.com/pcb/technology/specifications/
https://www.multi-circuit-boards.eu/en/pcb-design-aid/impedance-calculation.html
This is needed so that the e.g. 100 MHz clock is not lost when routing

The board is supplied by PCI 6-pin PEG ATX power (J10) on the back end.
The J11 on the back end connects via flat cable to J70 of SIS1160.
The front end has 6 digital channels J1-J6 (non-isolated).
J1-J4 are LVDS from/into the J70 of SIS1160 (input/output configurable).
J5-J6 are LVTTL from/into the J70 of SIS1160 (input/output configurable).
Adapt SW70 on SIS1160 pull-up depending on wanted termination.

The direction of every pair/signal at J70 can be controlled individually.
J1 <=> J70-[1,2]: [CLK_P, CLK_N] LVDS Synchronous clock source distribution
J2 <=> J70-[3,4]: [TRIG_P, TRIG_N] LVDS (Suggestion) Global trigger distribution, firmware defined
J3 <=> J70-[5,6]: [TIMES_P, TIMES_N] LVDS (Suggestion) Global timestamp distribution, firmware defined
J4 <=> J70-[7,8]: [USER1_P, USER1_N] LVDS General purpose
J5 <=> J70-[9]: [USER2_L] LVTTL General purpose, single ended, open drain
J6 <=> J70-[10]: [USER3_L] LVTTL General purpose, single ended, open drain

SW70-1: When ON, enable 100Ω Termination for CLK_P/CLK_N
SW70-2: When ON, enable 100Ω Termination for TRIG_P/TRIG_N
SW70-3: When ON, enable 100Ω Termination for TIMES_P/TIMES_N
SW70-4: When ON, enable 100Ω Termination for USER1_P/USER1_N
SW70-5: When ON, enable 4.7kΩ Pullup to 3.3V on USER2_L
SW70-6: When ON, enable 4.7kΩ Pullup to 3.3V on USER3_L

Potential upgrade:
- Blinking LEDs on front panel
- Change to Gompf bracket 9456-0000C ?
- Galvanic Isolation of J5 and J6
- Add SVG logos
- LVTTL to LVDS converter for CLK to CLK_P, CLK_N

https://ohwr.org/project/sis1160-pci-io
Front-end PCI board with LEMO connectors
to interface with GPIO interconnect pins of the SIS1160 FMC carrier (Struck).
Funded by Generalitat Valenciana under grant number CDEIGENT/2019/11.
Fernando Hueso-González - IFIC (CSIC/UV)

Sheet: /
File: BoardIO.kicad_sch

Title: SIS1160 PCI-L I/O add on

Size: A3	Date: 2021-06-02	**Rev: V0-0**
KiCad E.D.A. kicad 6.0.3-a3aad9c10e~116~ubuntu18.04.1		Id: 1/1