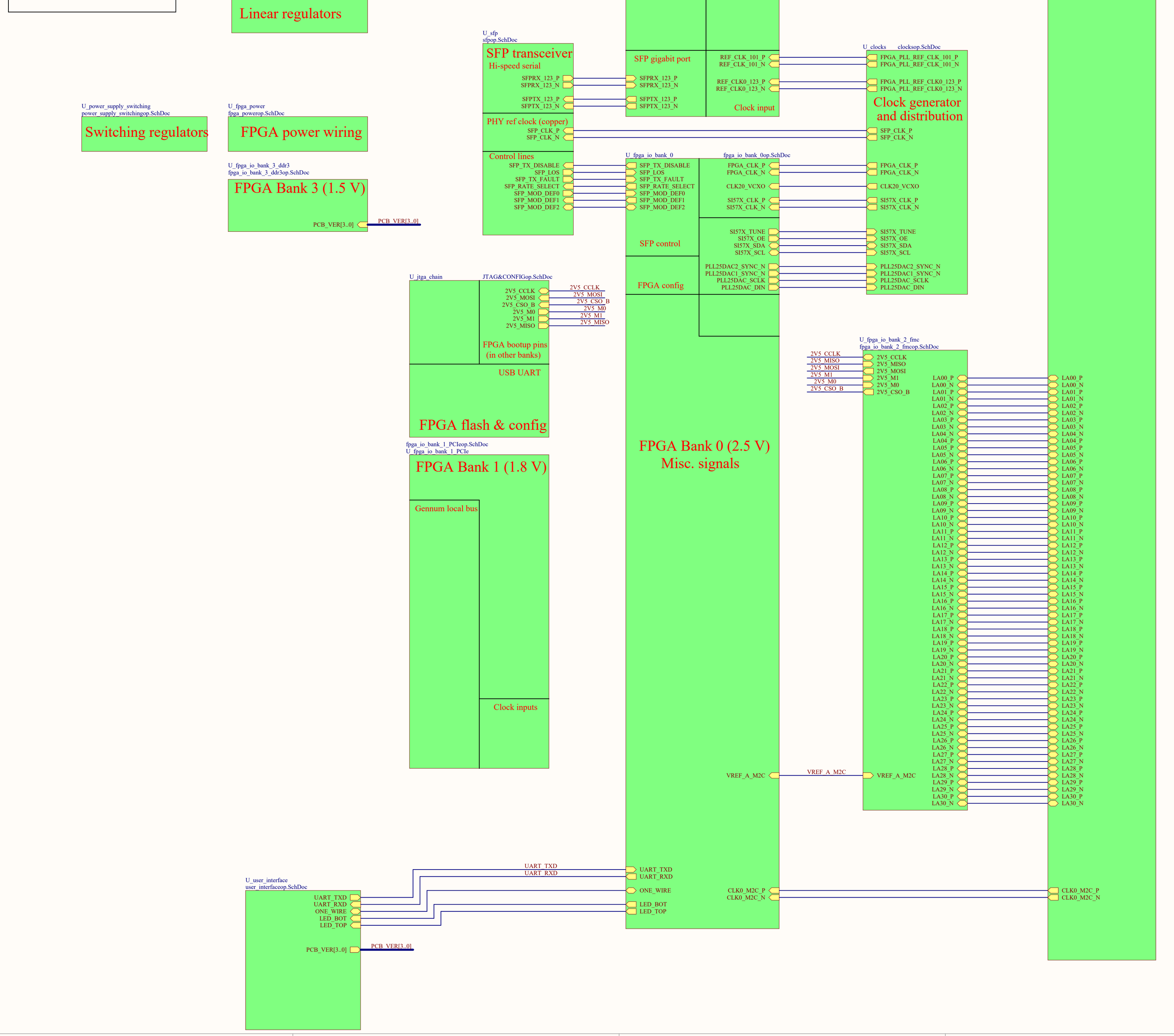

U_power_supply_linear
power_supply_linearop.SchDoc
Linear regulators
U_power_supply_switching
power_supply_switchingop.SchDoc
Switching regulators
U_fpga_power
fpga_powerop.SchDoc
FPGA power wiring
U_fpga_io_bank_3_ddr3
fpga_io_bank_3_ddr3op.SchDoc
FPGA Bank 3 (1.5 V)
PCB_VER[3..0]
U_sfp
sfpop.SchDoc
SFP transceiver
Hi-speed serial
SFPRX_123_P
SFPRX_123_N
SFPTX_123_P
SFPTX_123_N
PHY ref clock (copper)
SFP_CLK_P
SFP_CLK_N
Control lines
SFP_TX_DISABLE
SFP_LOS
SFP_TX_FAULT
SFP_RATE_SELECT
SFP_MOD_DEF0
SFP_MOD_DEF1
SFP_MOD_DEF2
fpga_gtpop.SchDocU_fpga_gtp
FPGA GTPs
SFP gigabit port
REF_CLK_101_P
REF_CLK_101_N
REF_CLK0_123_P
REF_CLK0_123_N
Clock input
U_clocks clocksop.SchDoc
FPGA_PLL_REF_CLK_101_P
FPGA_PLL_REF_CLK_101_N
FPGA_PLL_REF_CLK0_123_P
FPGA_PLL_REF_CLK0_123_N
Clock generator and distribution
U_fpga_io_bank_0 fpga_io_bank_0op.SchDoc
FPGA_CLK_P
FPGA_CLK_N
CLK20_VCXO
SI57X_CLK_P
SI57X_CLK_N
SI57X_TUNE
SI57X_OE
SI57X_SDA
SI57X_SCL
PLL25DAC2_SYNC_N
PLL25DAC1_SYNC_N
PLL25DAC_SCLK
PLL25DAC_DIN
SFP control
FPGA config
FPGA Bank 0 (2.5 V)
Misc. signals
U_jtga_chain JTAG&CONFIGop.SchDoc
2V5_CCLK
2V5_MOSI
2V5_CSO_B
2V5_M0
2V5_M1
2V5_MISO
FPGA bootup pins (in other banks)
USB UART
FPGA flash & config
FPGA Bank 1 (1.8 V)
U_fpga_io_bank_2_fmc
fpga_io_bank_2_fmcop.SchDoc
U_fmc_connector fmc_connectorop.SchDoc
LA00_P
LA00_N
LA01_P
LA01_N
LA02_P
LA02_N
LA03_P
LA03_N
LA04_N
LA04_P
LA05_P
LA05_N
LA06_P
LA06_N
LA07_P
LA07_N
LA08_P

Project/Equipment	TiCkS/ CTA		
Document	TiCkS	Designer	OR
		Drawn by	Ronan OGER 04/03/2019
		Check.by	04/03/2019
		Last Mod.	08/03/2019
		File	FMC_PCIe_Carrierop.SchDoc
		Print Date	13/11/2020 16:22:00 Sheet 1 of 17
CNRS-IN2P3 Laboratoire APC	MST-CAM-ED-0138-APC_ACTL-TIME/161201a	Size A2	Rev

Control voltage is +1.5V ±1V.
Min. pull range is ±10 ppm for ±1V.
Positive slope (Positive voltage for positive frequency shift).

CDCM61004 configuration:
LVDS outputs
PRESC DIV = 4
FB DIV = 20
OUT DIV = 4
All config inputs have internal pull-ups.

Input = 25 MHz
Output=125 MHz

DAC Vih = 2V so it accepts 2.5V CMOS signal

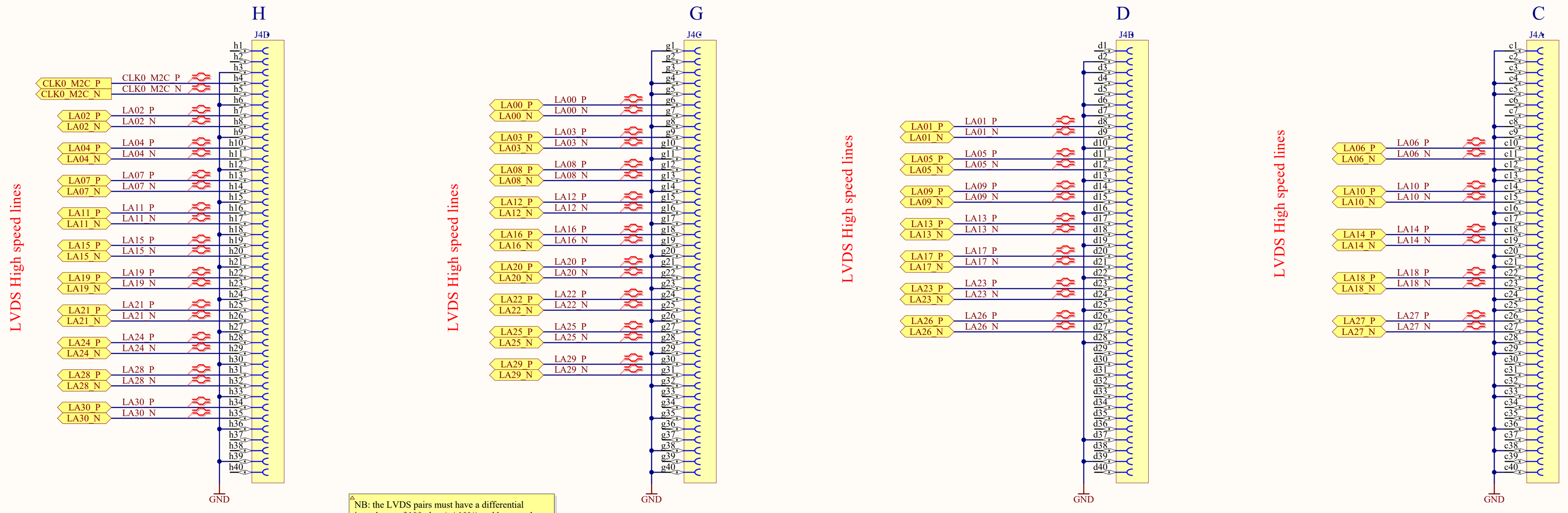
DAC ouput range: 0V to 2.5V

Optional RC filter for 1-bit DAC from FPGA output.
Can be used to fine tune Si571, which has a control voltage input.

Project/Equipment	CTA TiCkS board
Document	**Clocks Generation & distribution**
Designer	OR
Drawn by	OGER Ronan 10/02/2017
Check by	11/05/2017
Last Mod.	04/10/2018
File	clocksop.SchDoc
Print Date	13/11/2020 16:22:01 Sheet 2 of 17

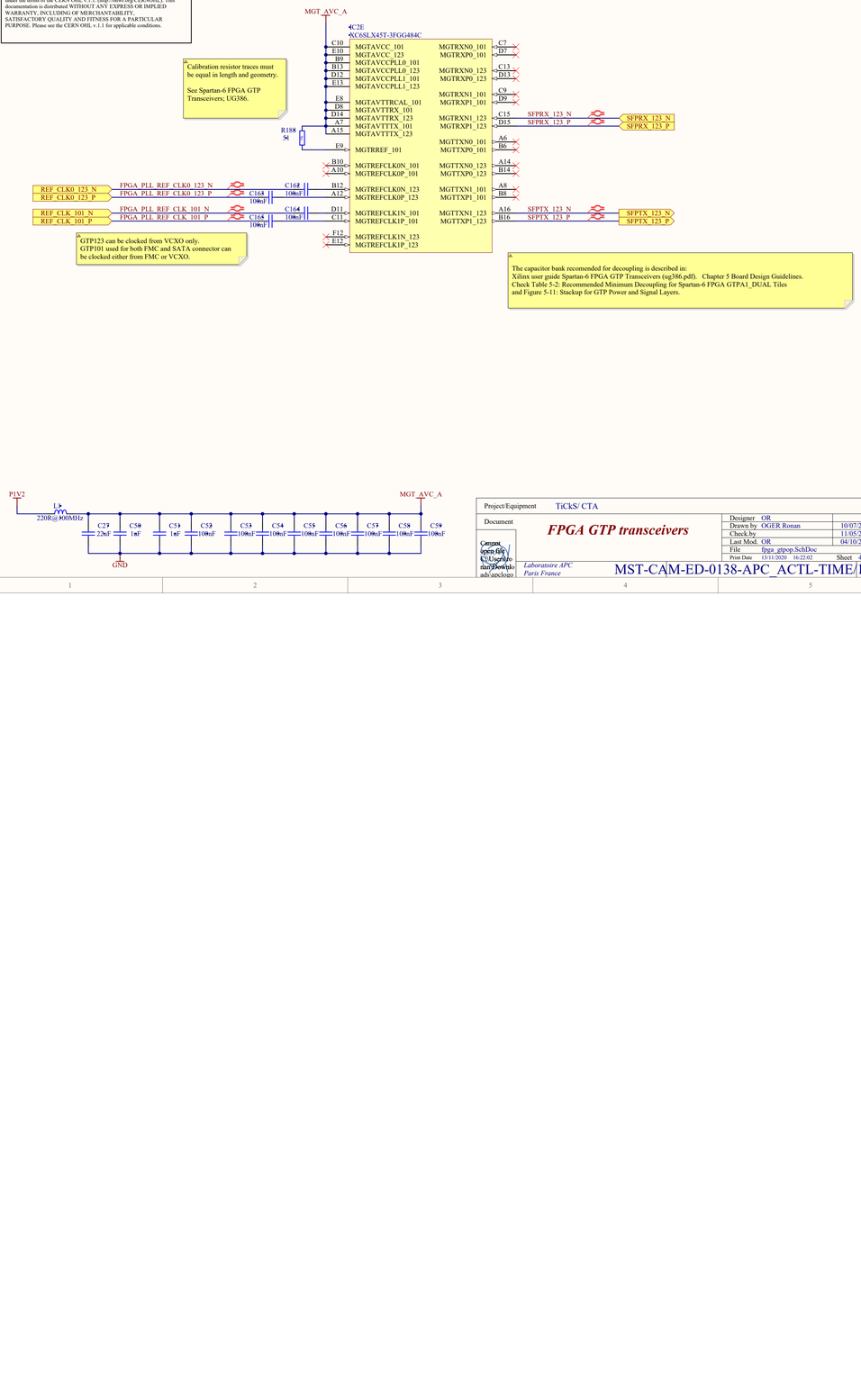
Laboratoire APC
Paris - france

MST-CAM-ED-0138-APC_ACTL-TIME-Fr1201a



NB: the LVDS pairs must have a differential impedance of 100 ohm (+/-10%) and be routed with no skew between the P and the N lines. The skew between the various LA pairs should be kept as low as possible (<200ps).

Project/Equipment	Simple PCIe Carrier Board		
Document	**FMC Connector**		
		Designer	GK, MC, TW, EB, PAS
		Drawn by	Greg Kasprowicz 10/07/2010
		Check.by	MC, TW, EB 11/05/2011
		Last Mod.	TW, MC 09/10/2018
		File	fmc_connectorop.SchDoc
		Print Date	13/11/2020 16:22:01 Sheet 3 of 17
BE-CO	*European Organization for Nuclear Research CH-1211 Geneve 23 - SwitzerLA_Pd*	EDA-02189-V4-0	Size A3 Rev -

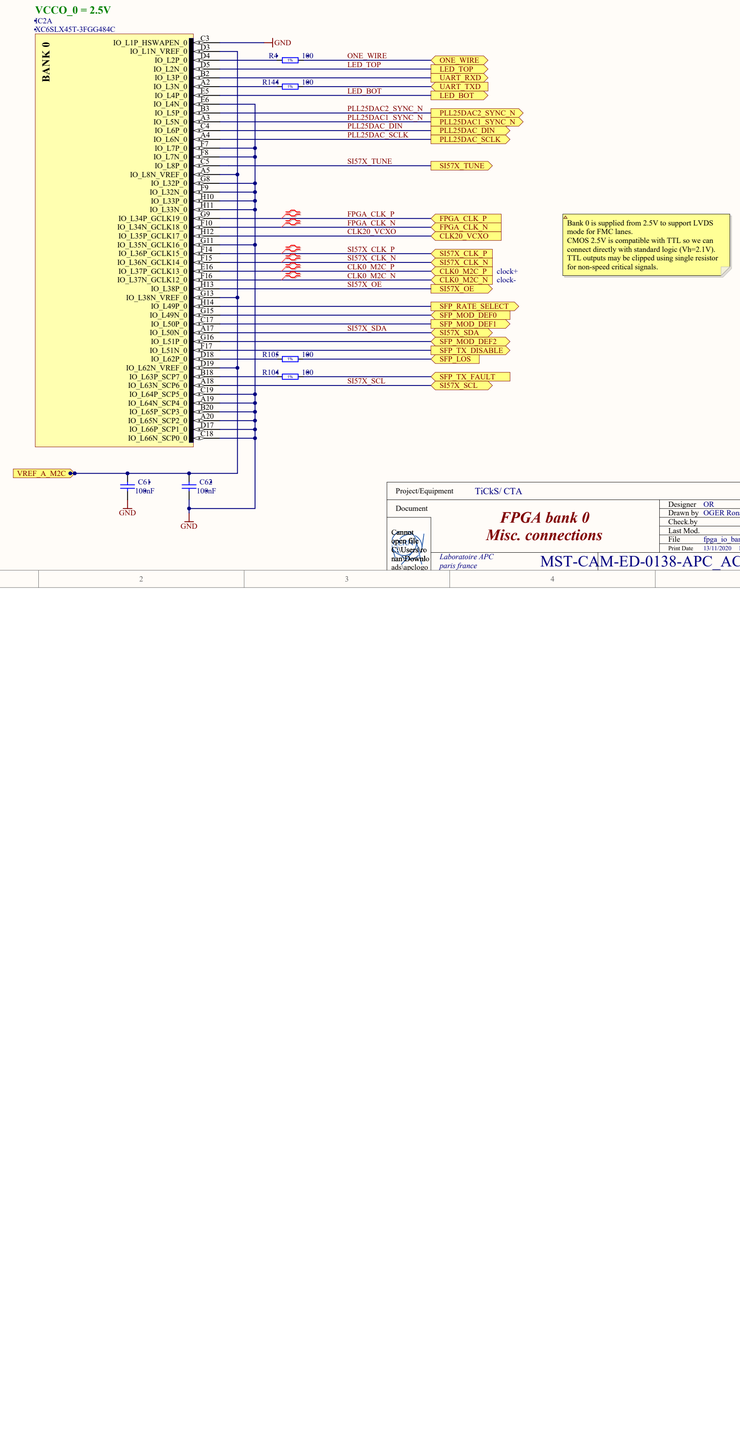


Project/Equipment	TiCkS/ CTA		
Document	*FPGA GTP transceivers*		
Designer OR			
Drawn by OGER Ronan		10/07/2016	
Check by		11/05/2017	
Last Mod. OR		04/10/2018	
File	fpga_gtpop.SchDoc		
Print Date	13/11/2020 16:22:02	Sheet 4 of 17	

Laboratoire APC
Paris France

MST-CAM-ED-0138-APC_ACTL-TIME/ FC1201a

Mount only one of the three options for HSWAP.
1) pull-up to P2V5 (FPGA IO in high-Z during configuration)
2) pull-down to GND (FPGA IO pulled-up during configuration)
3) from GN4124



Bank 0 is supplied from 2.5V to support LVDS mode for FMC lanes.
CMOS 2.5V is compatible with TTL so we can connect directly with standard logic (Vh>2.1V).
TTL outputs may be clipped using single resistor for non-speed critical signals.

Project/Equipment	TiCkS/ CTA		
Document	*FPGA bank 0 Misc. connections*	Designer OR	
		Drawn by OGER Ronan	10/07/2016
		Check by	11/05/2017
		Last Mod	04/10/2018
		File fpga_io_bank_0op.SchDoc	
		Print Date 13/11/2020 16:22:02	Sheet 5 of 17

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MST-CAM-ED-0138-APC_ACTL-TIME/ FC1201a

VCCIO_1=1.8V

VREF_GN4124

IC2B
XC6SLX45T-3FGG484C

BANK 1

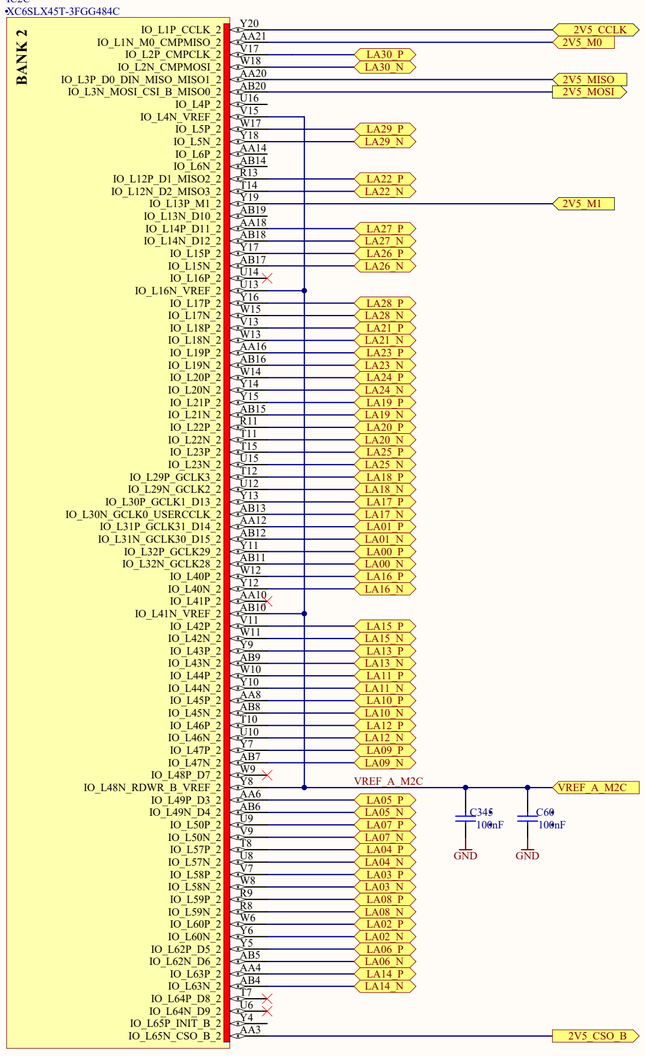
IO_L1P_A25_1	F18
IO_L1N_A24_VREF_1	F19
IO_L9P_1	H16
IO_L9N_1	H17
IO_L10P_1	B21
IO_L10N_1	B22
IO_L19P_1	J16
IO_L19N_1	J17
IO_L20P_1	C20
IO_L20N_1	C22
IO_L21P_1	L15
IO_L21N_1	K16
IO_L28P_1	D21
IO_L28N_VREF_1	D22
IO_L29P_A23_M1A13_1	G19
IO_L29N_A22_M1A14_1	G20
IO_L30P_A21_M1RESET_1	H18
IO_L30N_A20_M1A11_1	H19
IO_L31P_A19_M1CKE_1	J21
IO_L31N_A18_M1A12_1	J22
IO_L32P_A17_M1A8_1	F20
IO_L32N_A16_M1A9_1	F22
IO_L33P_A15_M1A10_1	J19
IO_L33N_A14_M1A4_1	J20
IO_L34P_A13_M1WE_1	K19
IO_L34N_A12_M1BA2_1	K18
IO_L35P_A11_M1A7_1	G20
IO_L35N_A10_M1A2_1	G22
IO_L36P_A9_M1BA0_1	K17
IO_L36N_A8_M1BA1_1	L17
IO_L37P_A7_M1A0_1	H21
IO_L37N_A6_M1A1_1	H22
IO_L38P_A5_M1CLK_1	C20
IO_L38N_A4_M1CLKN_1	J19
IO_L39P_M1A3_1	J20
IO_L39N_M1ODT_1	E22
IO_L40P_GCLK11_M1A5_1	M20
IO_L40N_GCLK10_M1A6_1	M19
IO_L41P_GCLK9_IRDY1_M1RASN_1	K21
IO_L41N_GCLK8_M1CASN_1	K22
IO_L42P_GCLK7_M1UDM_1	P20
IO_L42N_GCLK6_TRDY1_M1LDM_1	N19
IO_L43P_GCLK5_M1DQ4_1	N20
IO_L43N_GCLK4_M1DQ5_1	N22
IO_L44P_A3_M1DQ6_1	M21
IO_L44N_A2_M1DQ7_1	M22
IO_L45P_A1_M1LDQS_1	V20
IO_L45N_A0_M1LDQSN_1	V22
IO_L46P_FCS_B_M1DQ2_1	P21
IO_L46N_FOE_B_M1DQ3_1	P22
IO_L47P_FWE_B_M1DQ0_1	R20
IO_L47N_LDC_M1DQ1_1	R22
IO_L48P_HDC_M1DQ8_1	T21
IO_L48N_M1DQ9_1	T22
IO_L49P_M1DQ10_1	U20
IO_L49N_M1DQ11_1	U22
IO_L50P_M1UDQS_1	V21
IO_L50N_M1UDQSN_1	V22
IO_L51P_M1DQ12_1	W20
IO_L51N_M1DQ13_1	W22
IO_L52P_M1DQ14_1	Y21
IO_L52N_M1DQ15_1	Y22
IO_L53P_1	R19
IO_L53N_VREF_1	R19
IO_L58P_1	M16
IO_L58N_1	N15
IO_L59P_1	U19
IO_L59N_1	U20
IO_L60P_1	N16
IO_L60N_1	P16
IO_L61P_1	M17
IO_L61N_1	M18
IO_L70P_1	R15
IO_L70N_1	R16
IO_L71P_1	P17
IO_L71N_1	P18
IO_L72P_1	R17
IO_L72N_1	T17
IO_L73P_1	T19
IO_L73N_1	T18
IO_L74P_AWAKE_1	V19
IO_L74N_DOUT_BUSY_1	V20

Project/Equipment	TiCkS/ CTA		
Document	***FPGA bank 1***	Designer	OR
		Drawn by	OGER Ronan 10/07/2016
		Check.by	11/05/2017
		Last Mod.	OR 04/10/2018
		File	fpga_io_bank_1_PCIeop.SchDoc
Cannot open file C:\Users\ronan\Downloads\apclogo	*Laboratoire APC paris france*	Print Date	13/11/2020 16:22:02 Sheet 6 of 17

MST-CAM-ED-0138-APC_ACTL-TIME/ 1.1201a

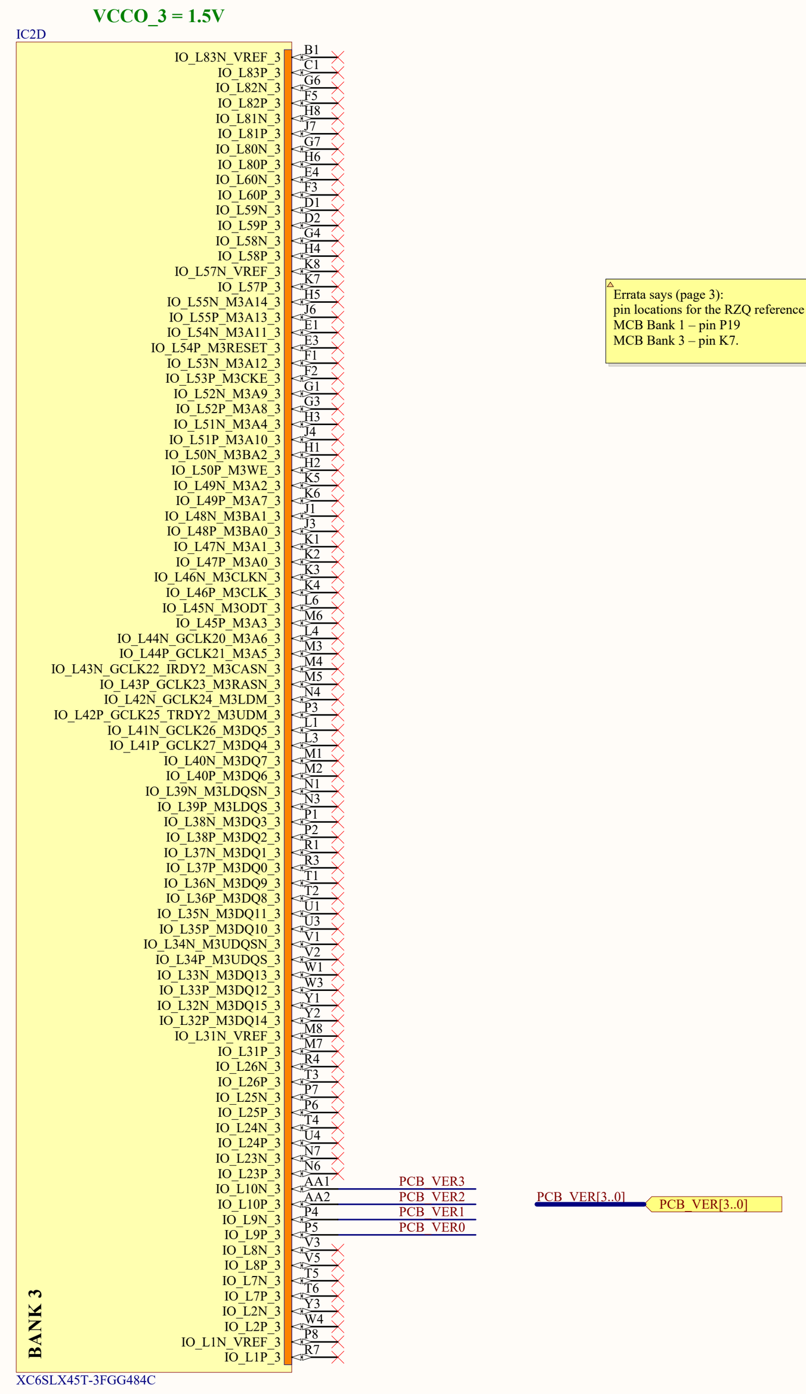
VCCO_2 = P2V5

C2C
XC6SLX45T-3FGG484C



Project/Equipment	Simple PCIe Carrier Board	
Document	**FPGA bank 2 FMC connections**	
Designer	GK, MC, TW, EB, PAS	
Drawn by	Greg Kasprowicz	10/07/2010
Check.by	MC, TW, EB	11/05/2011
Last Mod.	TW, MC	08/10/2018
File	fpga_io_bank_2_fmcop.SchDoc	
Print Date	13/11/2020 16:22:03	Sheet 7 of 17
BE-CO	European Organization for Nuclear Research, CH-1211 Geneve 23 - Switzerland	EDA-02189-V4-0
Size	A4	Rev -

Termination resistors must be placed close to FPGA.



Errata says (page 3):
pin locations for the RZQ reference resistor:
MCB Bank 1 – pin P19
MCB Bank 3 – pin K7.

Project/Equipment	TiCkS/ CTA		
Document	FPGA bank 3	Designer	OR
		Drawn by	OGER Ronan 10/07/2017
		Check.by	11/05/2017
		Last Mod.	04/10/2018
		File	fpga_io_bank_3_ddr3op.SchDoc
		Print Date	13/11/2020 16:22:03 Sheet 8 of 17
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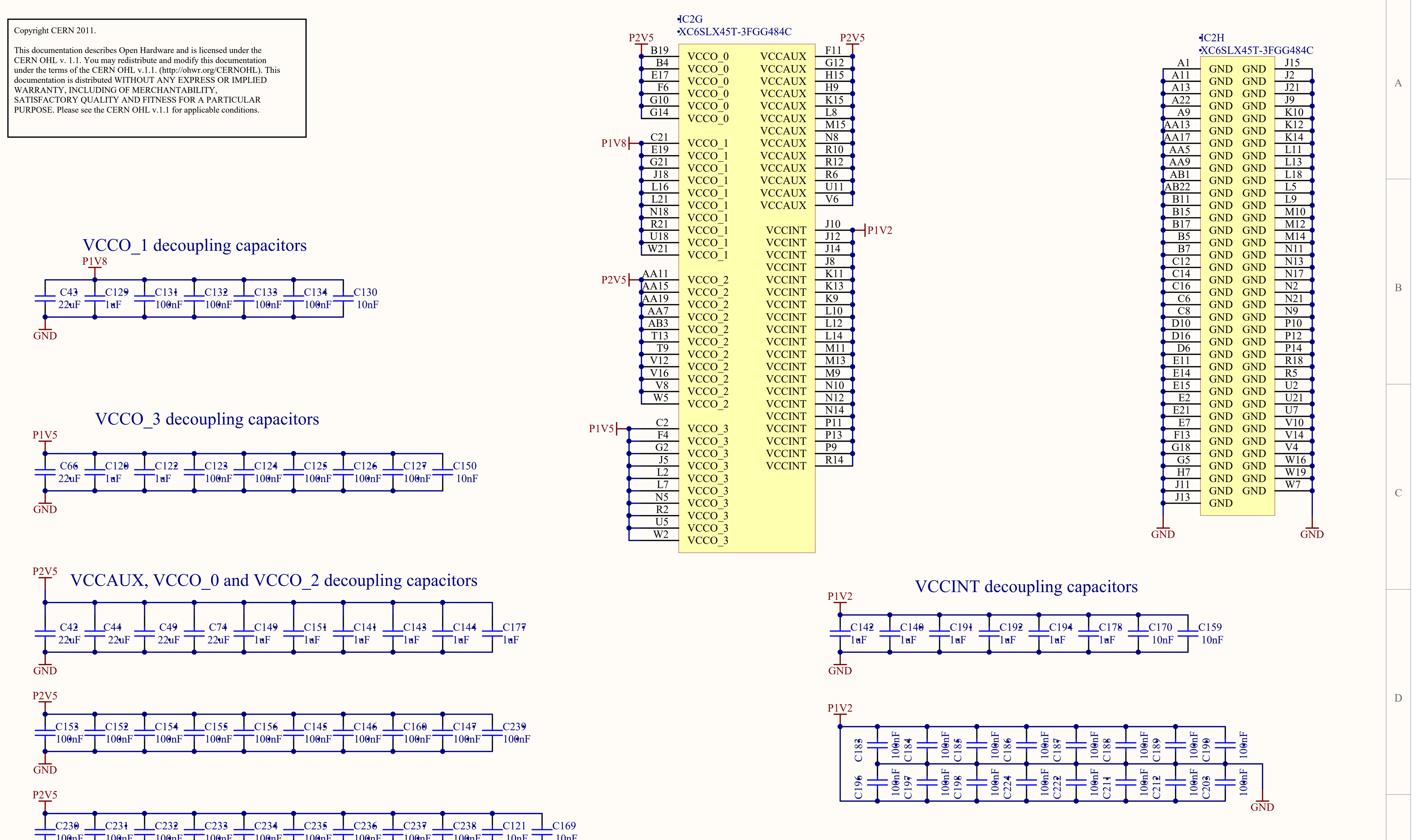

Project/Equipment	TiCkS/ CTA		
Document	**FPGA Power supplies**	Designer	OR
		Drawn by	Ronan OGER 10/07/2016
		Check.by	OR 11/05/2017
		Last Mod.	26/03/2019
		File	fpga_powerop.SchDoc
		Print Date	13/11/2020 16:22:03 Sheet 9 of 17
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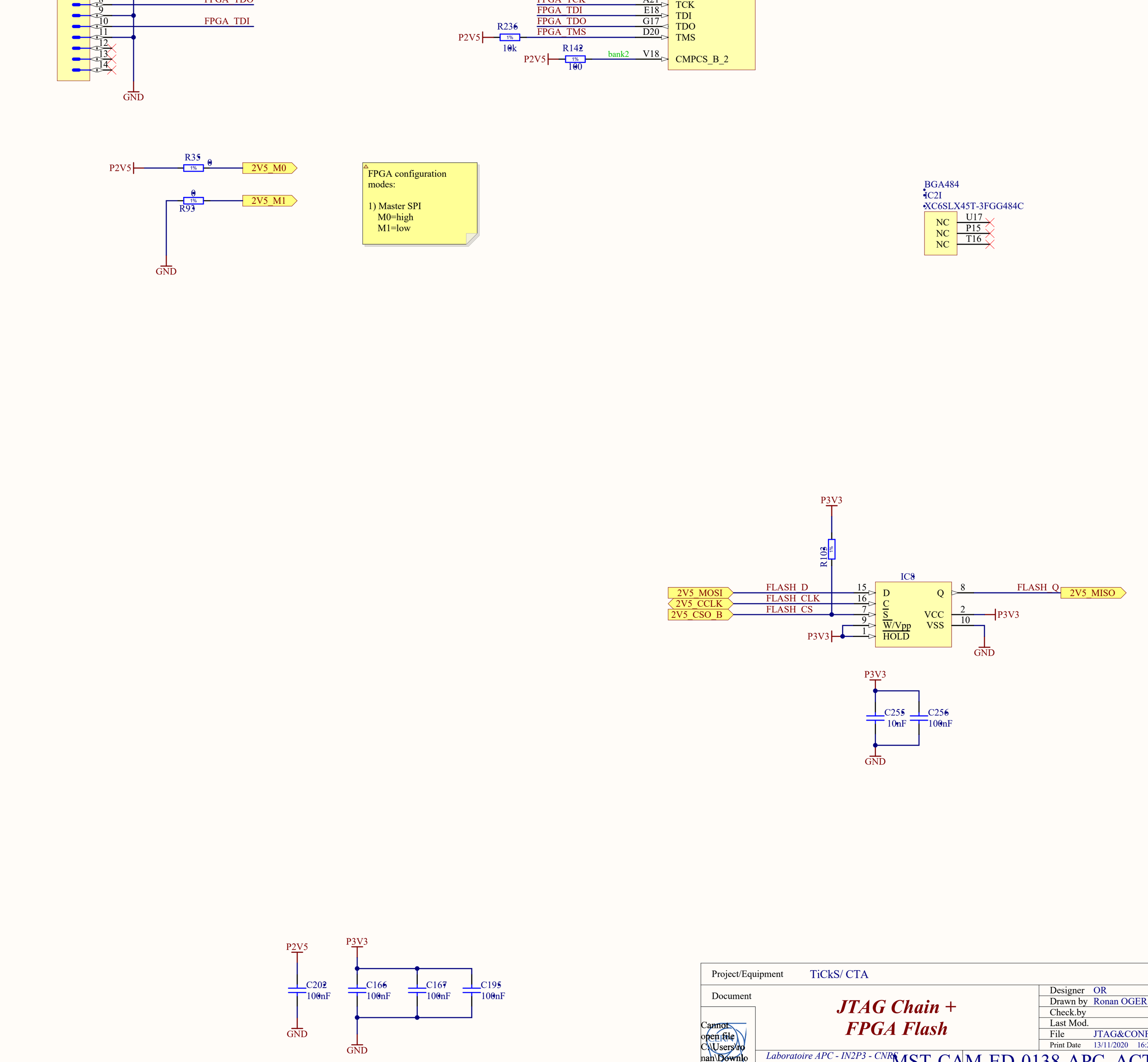

Project/Equipment	TiCkS/ CTA		
Document	**_JTAG Chain + FPGA Flash_**	Designer	OR
		Drawn by	Ronan OGER 10/07/2016
		Check.by	11/05/2017
		Last Mod.	28/03/2019
		File	JTAG&CONFIGop.SchDoc
		Print Date	13/11/2020 16:22:04 Sheet 10 of 17
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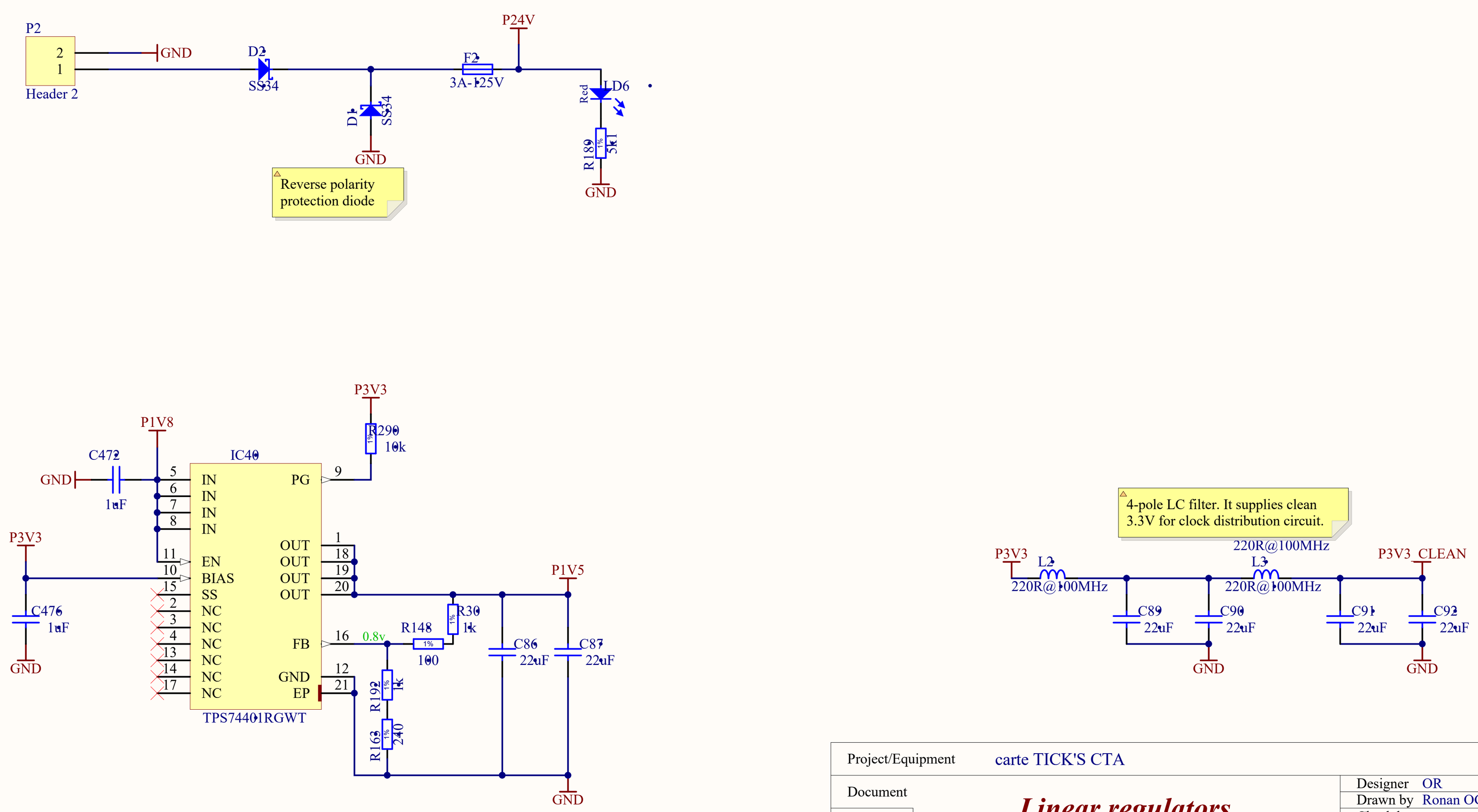
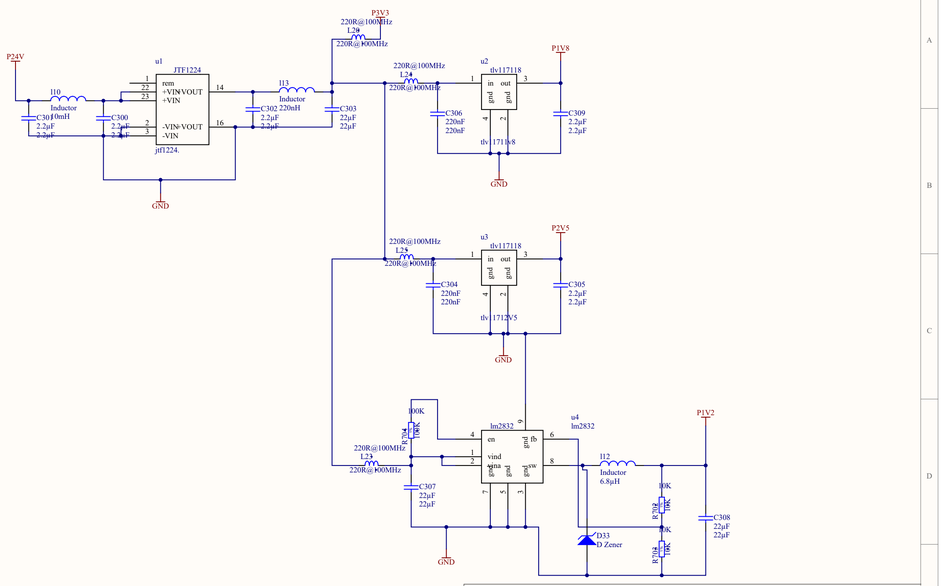


Project/Equipment	carte TICK'S CTA		
Document	**Linear regulators 1V5**	Designer	OR
		Drawn by Ronan OGER	10/07/2016
		Check.by	11/05/2017
		Last Mod.	28/03/2019
		File	power_supply_linearop.SchDoc
		Print Date 13/11/2020 16:22:04	Sheet 14 of 17
Cannot open file C:\Users\ronan\Downloads\apclogo	*Laboratoire APC Paris france*	MST-CAM-ED-0138-APC_ACTL-TIME/161201a	Size A4 Rev



Project/Equipment	CTA TiCkS board		
Document	*Switching regulators 3.3V, 2.5V, 1.8V and 1.2V*	Designer OR	
		Drawn by Ronan OGER	10/07/2016
		Check by	11/05/2017
		Last Mod.	09/10/2018
		File	power_supply_switchingop.SchDoc
		Print Date	13/11/2020 16:22:05 Sheet 15 of 17
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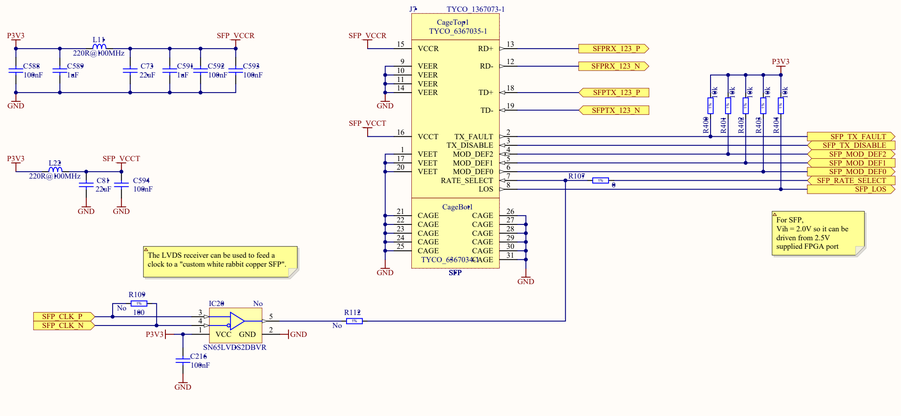

Project/Equipment	carte TICK'S CTA		
Document	SFP		
Designer	OR		
Drawn by	Ronan OGER	10/07/2016	
Check by		11/05/2017	
Last Mod.		04/10/2018	
File	sfpop.SchDoc		
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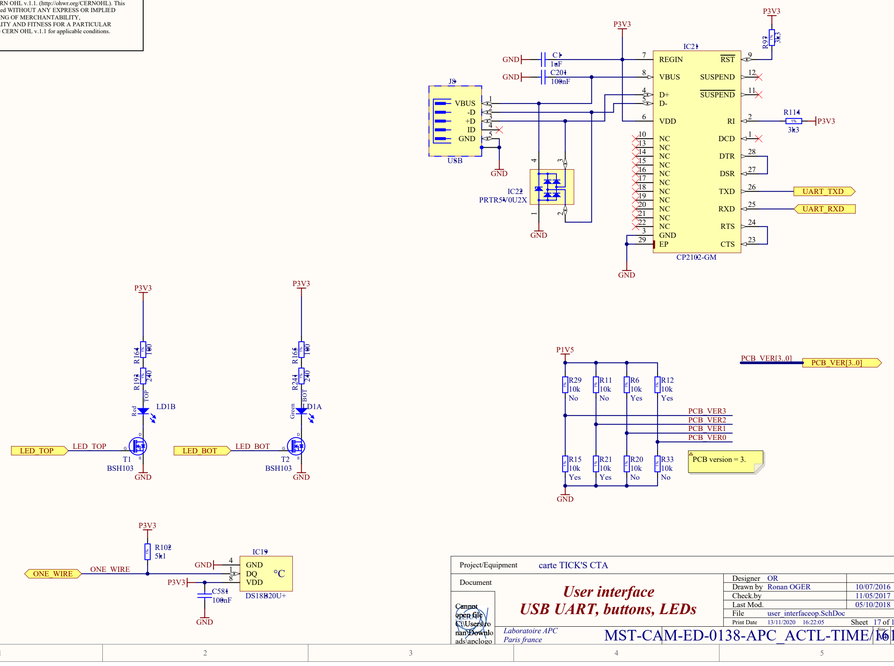
Paris france

MST-CAM-ED-0138-APC_ACTL-TIME/Ed1201a



Project/Equipment	carte TICK'S CTA		
Document	*User interface USB UART, buttons, LEDs*	Designer OR	
		Drawn by Ronan OGER	10/07/2016
		Check by	11/05/2017
		Last Mod.	05/10/2018
		File user_interfaceccp.SchDoc	
		Print Date 13/11/2020 16:22:05	Sheet 17 of 17

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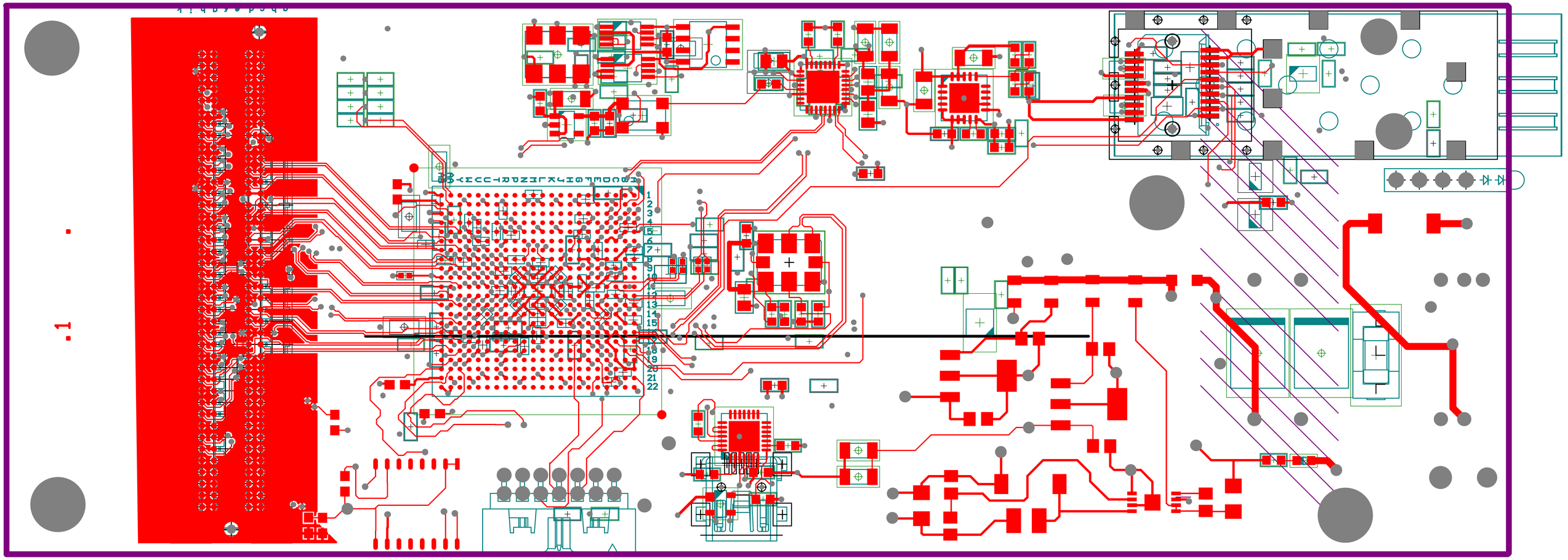
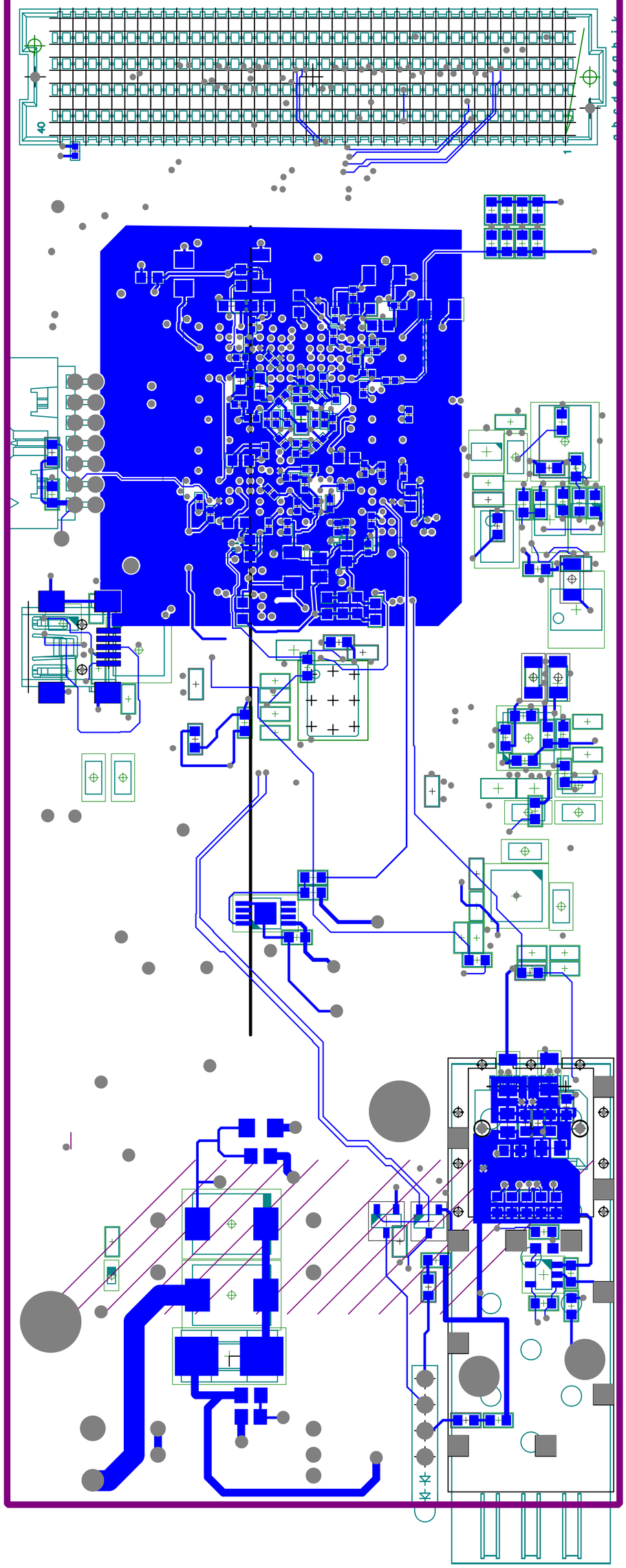
Laboratoire APC
Paris france

MST-CAM-ED-0138-APC_ACTL-TIME/Ed1201a

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Laboratoire APC / IN2P3 / CNRS
TiCKS CTA
R. Oger
JTAG
IC2
OSC2
OSC4
IC10
IC6
IC40
J4
J7
L20
L24
L25
L23
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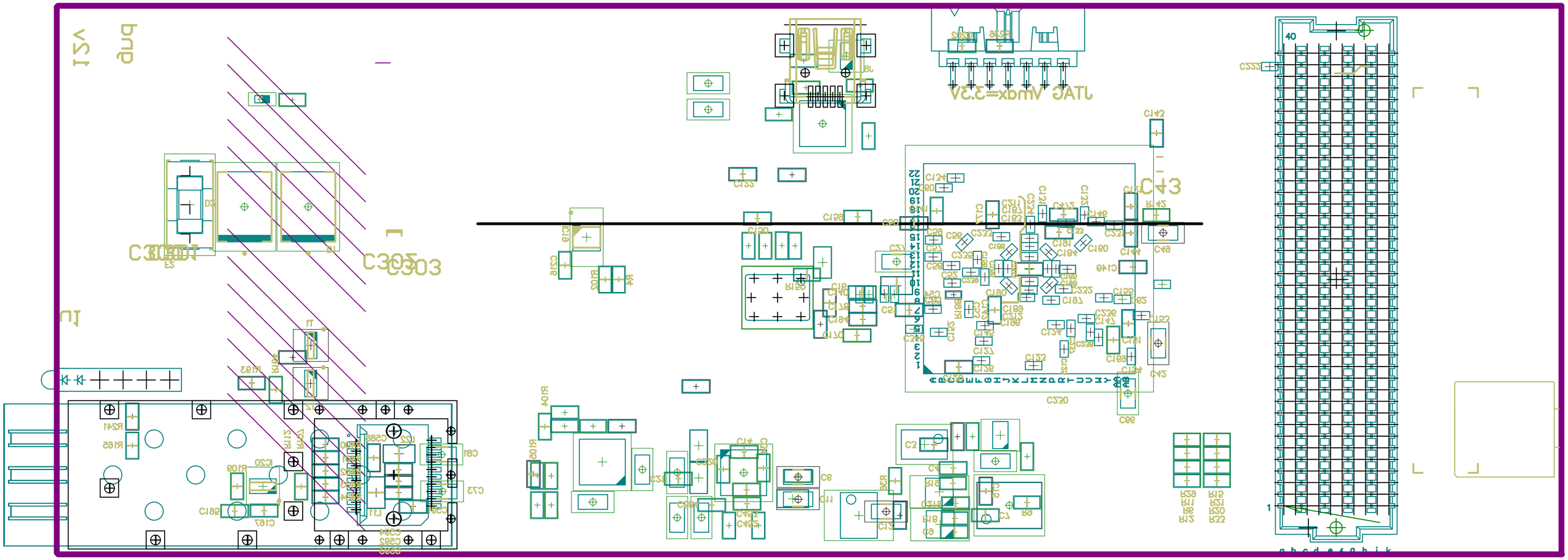
110
112
C306
C304
C309
C305
C308
C307
u2
u3
u4
D33
R702
R703
R704
R93
R35
R103
IC8
r701
r700
p3v3
p2v5
C256


C43
JTAG Vmax=3.3V
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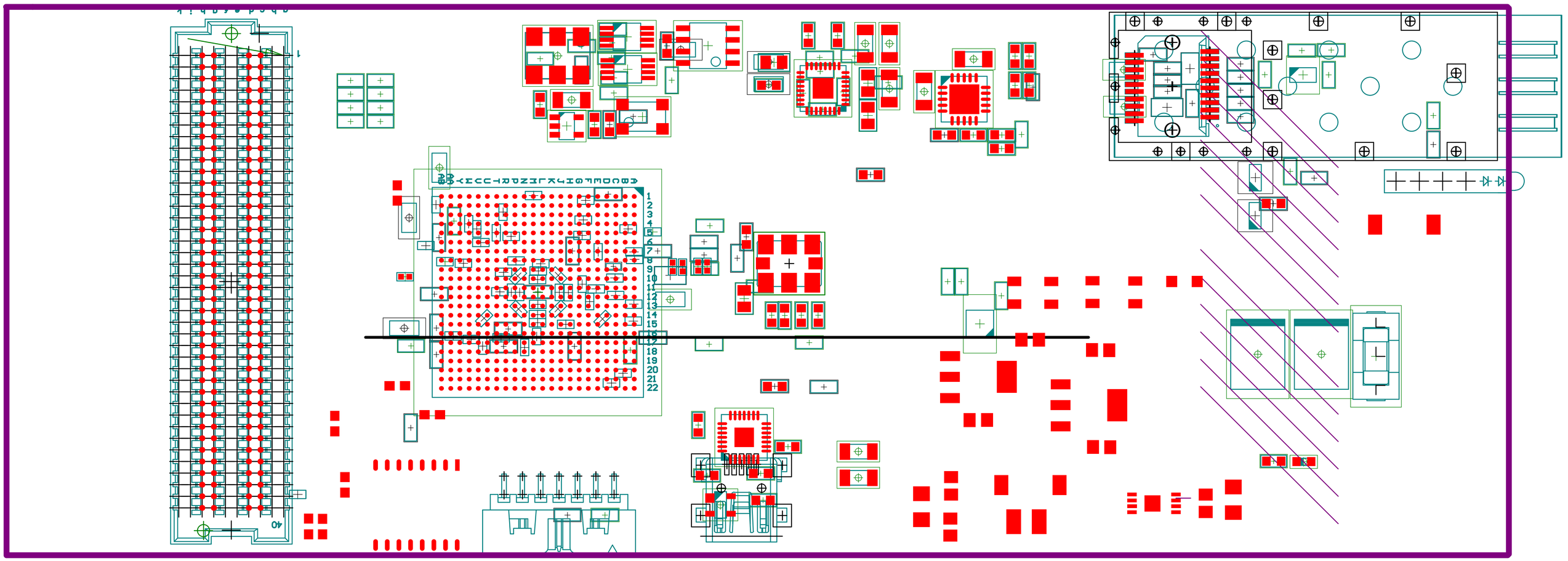

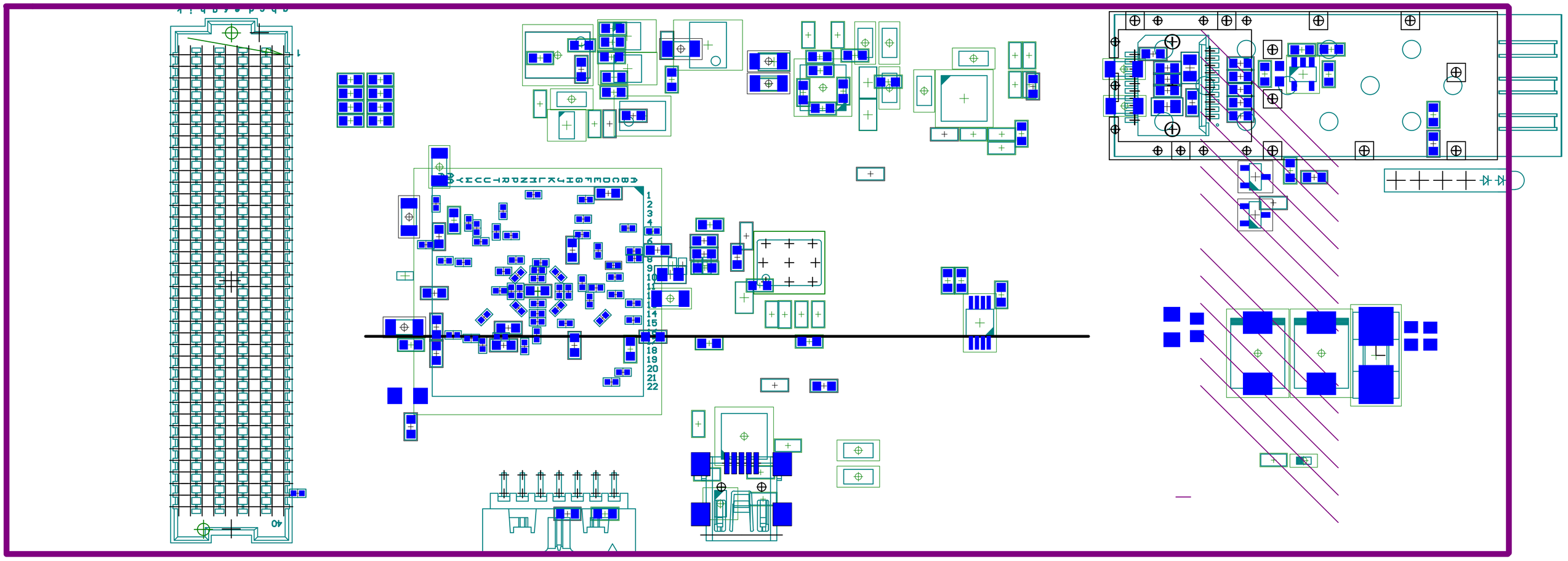
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