ATLAS iTK week – Read-Out Systems

A SPEC Based Data Acquisition System

Prototypes and preliminary results

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• Overview

Introduction

• Motivation and requirements

SPEC card

• Description and specifications

J/O

• Signal transceivers, passive protection

Level Adjustment

• DAC, Amplifier, Power supply and regulators

Triggering

• Programmable LEMO -TTL inputs

Programming

• Flip-Flops and Clock buffer

Connectors

• FMC, HE10 and LEMO

Mechanics

• Layout ad footprint

Open Issues

• Capacitors technology, interferences and design

Conclusions

• Outcome and prospects
• Introduction

Motivation and Requirements

Motivation

• Parallel sensor testing
• Unavailability of USB-PIX 2 and 3
• Compatibility with different ASIC technologies (FE-I4, RD53, Omegapix)
• J-TAG and antilog debugging required

Read-out system requirements:

• Generic reconfigurable design
• Open reprogrammable platform
• Rapid development time
• Test beam and irradiation compatible
• Availability and low cost

• Spec card
• I/O
• Level Adjustment
• Triggering
• Programming
• Connectors
• Mechanics
• Open Issues
• Conclusions

Motivation and Requirements

1. Low threshold (1000 e), low noise ~300 fF high leakage current (up to 100 nA per channel) tolerance
2. 8 bits local threshold adjustment
3. 3 bits Time-Over-Threshold measurement
4. Event pile-up rejection
**SPEC Card**

**Description and Specifications**

Base support for the I/O board:
- PCIe Bus (4 Gbit Max) speed
- Xilinx Spartan 6 FPGA
- 12V power line output
- J-TAG, USB and SATA interconnections
- Generic Linux driver module
- Low cost (~ 700€), high availability
- No extra specialised hardware needed

### 160 pin Low-Density FMC Connector

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power output voltage</td>
<td>12V</td>
</tr>
<tr>
<td>Available differential lines</td>
<td>34</td>
</tr>
<tr>
<td>Available digital inputs</td>
<td>68</td>
</tr>
<tr>
<td>Output FPGA level (digital signal)</td>
<td>2.5V</td>
</tr>
<tr>
<td>Memory</td>
<td>256 MB DDR3 RAM</td>
</tr>
<tr>
<td></td>
<td>4 MB Flash</td>
</tr>
<tr>
<td>Max. Output</td>
<td>2A</td>
</tr>
</tbody>
</table>

**PC – Xpress interface implemented**
Signal transceivers and protection

**Compatibility**
- Multi-level signal adjustment
  - Compatible with inputs form 0.5V to 5.5V
  - Programmable transceivers

**Protection**
- High Z functionality
  - Independent adjustment in each line (FE-I4 power return)
  - ZENER line protection

**Adaptability**
- Direction Autosense
  - Bi-directional communication
  - User-free intervention
  - Configurable as pseudo-differential or single lines
• Level Adjustment

DAC, Amplifier, Power Supply and Regulators

Digital to analog converter for continues voltage stepping

Symmetric operational amplifier for 64 line adjustment

Power Supply and regulation for negative voltage generation and stabilization
• Triggering

Signal transceivers and protection

**TTL Signal**
- Slow positive logic pulses
- μsec timescale
- 0 – 5V rise square shape pulse

**NIM signal**
- Fast timing systems
- nsec timescale
- 0 – 0.8V rise square shape pulse
- Negative pulses

**Trigger I/O**
- Six trigger inputs
- Individual FPGA lines assigned
- Appropriate level shifting to 2.5V
- Programmable input logic to manage NIM or TTL signals
Programming

Flip-flops and clock buffering

Serìal Programming
- Distribute 58 High-Z transceiver commands
- Transmit 4-bit DAC sequence
- 6 trigger commands

Clock distribution
- Synchronize command transmission
- Coordinate 58 input channels and 6 trigger inputs

Sacrifice minimum number FPGA lines

64 flip-flop in two 32 arrays

4 FPGA lines sacrificed
Connectors

HE-10, LEO, FMC

Data Input

Generic HE-10 Ribbon Connector

- Tree 24-pin connectors
- Standard low density ribbon cable

Data Output

FMC Low density connector

- High compatibility, low density
- Industrial standard
- System independent

Trigger

Six 50Ohm coaxial connectors

- Right angle LEMO 00 standard
- Small size, self latching ruggedized ports
• Mechanics

Layout and Footprint

Mechanical aspects

• Full assembly (SPEC + MLIB) occupies one PCI-Xpress slot
• Trigger inputs accessible from front side
• MLB Card contained within FMC footprint
• Data input connectors aligned with respect to SPEC card bottom opening

Fabrication aspects

• Only SMD components due to space issues
• 8-layer PCB
Open Issues

Capacitors, interferences and Design

First Prototypes tested at LAL

✓ Transceiver functional from 0.9 to 5.5 V
✓ Cadence design left-over introduced a third partially used flip-flop array
✓ Some interferences form chosen power supply
✓ Capacitors at low SMD series used are no-longer Low-ESR, 25Ohm equivalent series resistance
✓ Tested with good results up to 20MHz, capacitors problems becomes predominant
Conclusions

Prospects and suggestions

Conclusions

• First iteration fully functional
• Programmable interface
• Initial tests up to 20MHz
• Capacitor technology issue identified

Prospects

• Use aluminium-polymer capacitors
• Replace the PSU with a proper unit
• Remove third martially used flip-flop array
• 2 weeks redesign time

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