SPEC7 V2

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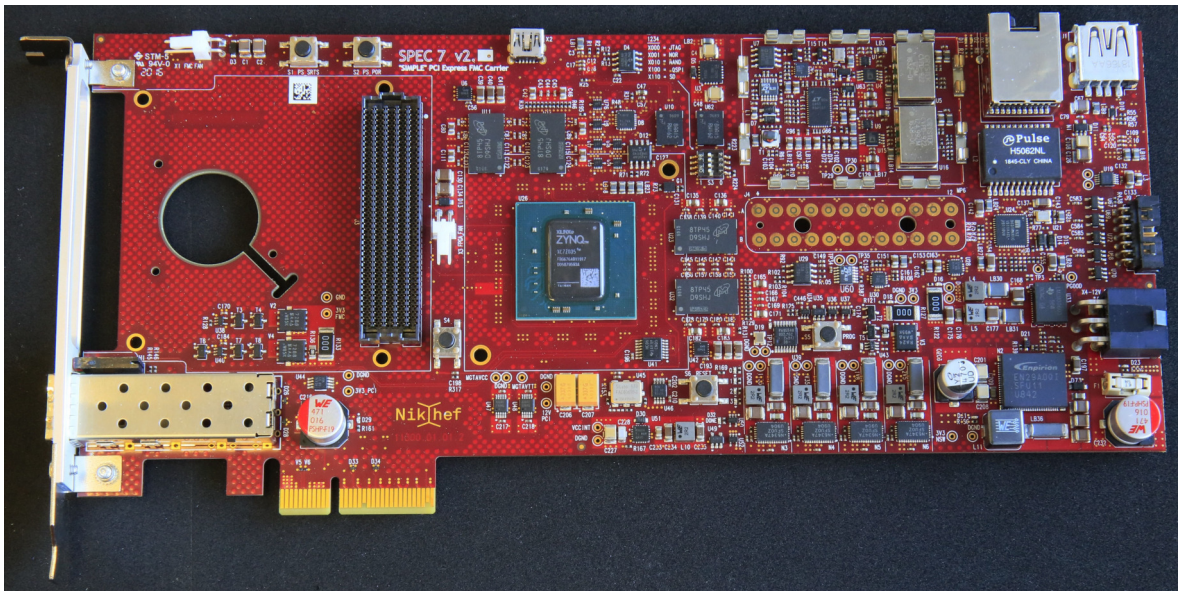
05-10-2021



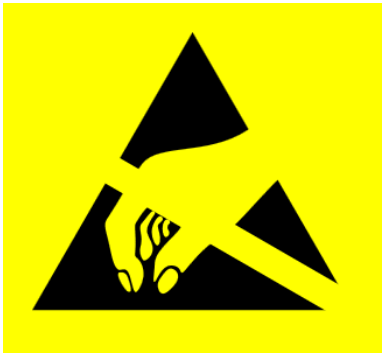
Contents

Revision History

Revision	Date	Author(s)	Description
0.0	13-03-2020	G C Visser	Created.
0.1	16-07-2020	P Jansweijer	1st (very) preliminary public version.
0.2	15-09-2020	P Jansweijer	add details on reference and WRITE design.
0.3	30-05-2021	P Jansweijer	SPEC7.git origin set to ohwr.org.
0.4	24-09-2021	P Jansweijer	add note on 10MHz phase noise bump.

1 Safety directions

Please read this chapter before using the SPEC7



- Never exceed the maximum rated input voltage, a higher voltage as stated as maximum will damage the device. See section 8 for maximum allowed voltages.
- The electronics is **ESD** sensitive, use a safe **ESD** workplace.
- Although ESD protected, SiliconLabs CP2105 (U54, dual UART) seems to be a weak spot. When the SPEC7 is operated stand alone then the chassis of the PC that is connected to the mini USB connector (X2) must be at SPEC7 ground potential. See also section 1.

2 Introduction

The SPEC7 [4] is the successor of the SPEC [5]. SPEC7 stands for Simple PCIe FMC Carrier, based on Xilinx 7-series FPGAs. More specifically the board utilizes a Xilinx Zynq-7000 FPGA (Z030 or Z035) with Dual-Core ARM processor integrated. The FMC PCIe Carrier is an FMC carrier that can hold one FMC card and an SFP connector. As was the case with the SPEC, the SPEC7 is specifically designed to enable White Rabbit deployment. To facilitate this, the board contains Voltage Controlled Crystal Oscillators (VCXOs) and Digital to Analog Converters (DACs).

The design was optimized for low phase noise. For demanding users (like metrology institutes) the SPEC7 can be equipped with an external oscillator in order to further decrease phase noise. It is left to the demanding user how much money is spend on a better external oscillator such that they can make their own trade-offs. An example design that uses a high precision external oscillator is the High Precision External Slave Clock (HPSEC [3]) design which incorporates a SPEC7.

2.1 Overview of the SPEC7

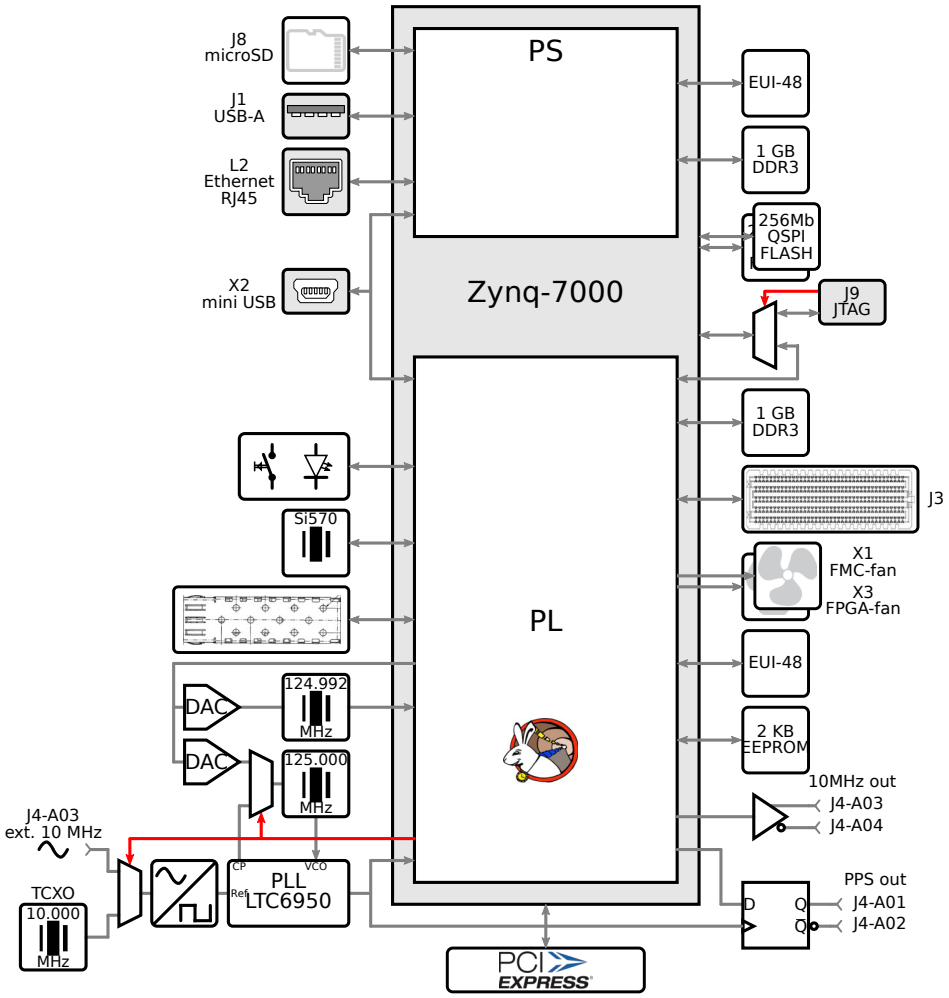


Figure 1: SPEC7 block diagram.

Xilinx Zynq-7000 devices contain a Processing System (PS) and Programmable Logic (PL). Both PS, PL and their respective connections are shown in the SPEC7 block diagram (figure 1).

2.2 White Rabbit Clocking

The SPEC7 contains an LTC6950 PLL which is used to distribute and generate the White Rabbit 125 MHz reference clock. The LTC6960 needs to be configured via SPI by software.

Two LEDs show the status of the LTC6950. LED D74 is lit red when there is no reference clock found. LED D72 is lit green when the PLL is locked. Without configuration and without reference clock LED D74 is on (default after power up with no FPGA image). Mode bits WR_MODE(1:0) determine how clocks are routed. Table 2 and the paragraphs below explain how clocks are routed according to the WR_MODE(1:0) status.

WR_MODE(1:0)	
00	Reserved
01	Free-running Master
10	Slave
11	Grand Master

Table 2: WR_MODE(1:0) (FPGA pins C12, B12) select White Rabbit Clocking options.

The following sections describe the White Rabbit modes that can be selected.

2.2.1 Mode Slave

Traditionally the SPEC7 is used as a WR-node which means that it operates in mode slave. Figure 2 shows how the DAC is selected to tune the VCXO that feeds the LTC6950. In this mode the PLL is switched of and the LTC6950 is only used as a clock distribution system. In this mode LEDs D72 (Lock) and D74 (NoRef) are both off.

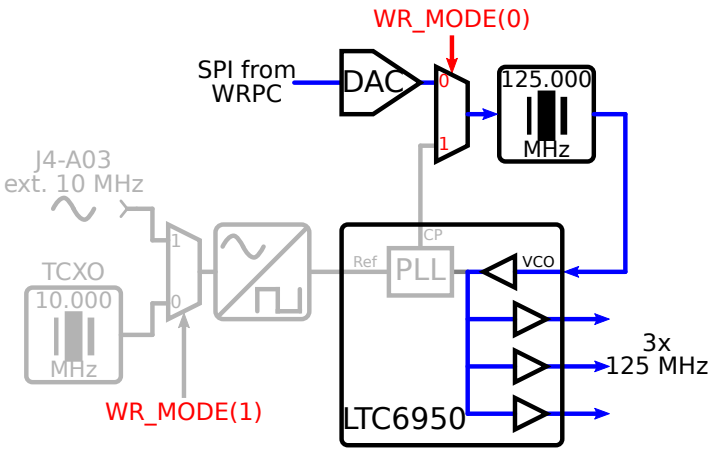


Figure 2: Clock selection for Mode Slave.

The configuration shown in figure 2 also allows for the traditional WR *mode master* and *mode gm* where the 125 MHz VCXO is taken as a reference clock or the 125 MHz VCXO is phase locked and aligned to an external 10MHz source, respectively.

2.2.2 Mode Master

The SPEC7 can be operated as a free running master. In this mode an on board TCXO 10MHz oscillator is switched on (see figure 3). This clock is fed to the PLL of the LTC6950. The PLL Charge Pump signal is now tuning the VCXO. The PLL divides by 2 and multiplies by 25 to generate and distribute the 125MHz reference clock. In this mode LEDs D72 (Lock) is on and D74 (NoRef) is off.

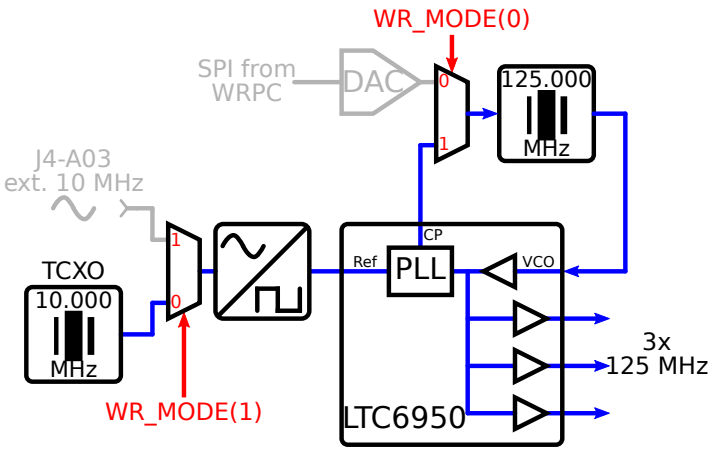


Figure 3: Clock selection for Mode Master.

2.2.3 Mode Grand Master

The SPEC7 can be operated as Grand Master. In this mode and external 10MHz (sine-wave) reference (and 1PPS) is applied (see figure 4). This clock is fed to the PLL of the LTC6950. The PLL Charge Pump signal is now tuning the VCXO. The PLL divides by 2 and multiplies by 25 to generate and distribute the 125MHz reference clock. When a reference clock is present then LED D74 (NoRef) should be off. When a reference clock has the proper frequency and the PLL can lock then LED D72 (Lock).

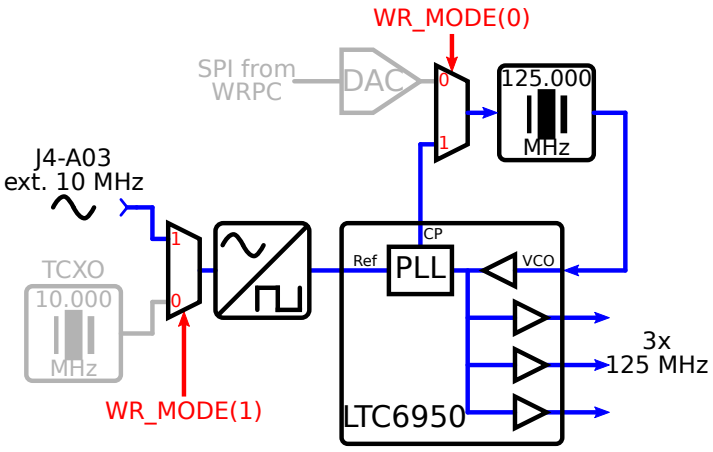


Figure 4: Clock selection for Mode Grand Master.

2.3 JTAG Header J9

The JTAG chain on the SPEC7 is routed through the Zynq FPGA and the FMC. By default the JTAG chain is connected to the PL of the Zynq FPGA (see table 3). This enables a JTAG connection between the logic in the FPGA and devices JTAG present on the FMC.

PL User JTAG	Direction	FPGA Pin
TCK	out	K12
TMS	out	E13
TDI	out	C13
TDO	in	A13

Table 3: PL FPGA pins that connect to the SPEC7 JTAG chain.

The presence of an FMC is detected by the PRSNT_M2C signal. When an FMC card is absent then the FMC connector TDI and TDO are automatically connected by an electronic switch.

A Xilinx Download Cable can be plugged in connector J9 to configure the FPGA. Once a Download Cable is plugged into J9 the JTAG chain it is automatically connected. Presence of a Download Cable is detected by pin 1 of J9 (see figure 5). Most[1] programming cables have pin 1 grounded.

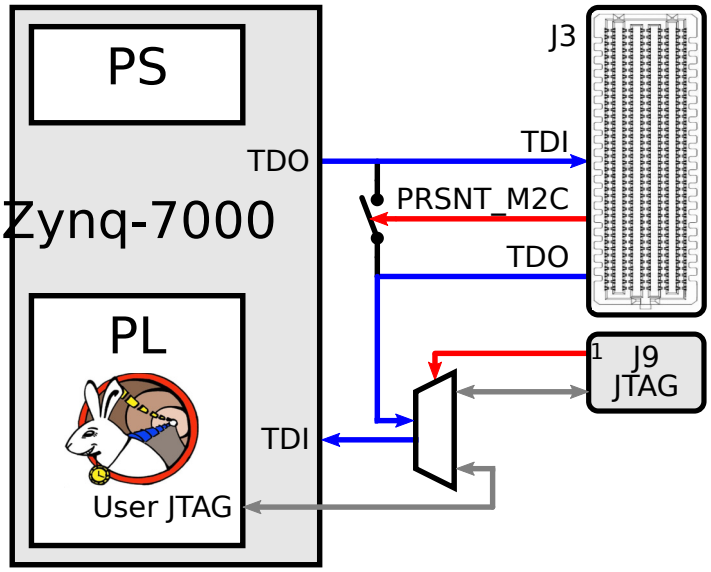


Figure 5: J9: Presence of an FMC and a Xilinx Download Cable is automatically detected.

[1]Download cables that do **not** have pin 1 grounded are Xilinx Platform Cable USB II and Digilent JTAG-HS2. This causes an error "no device detected on target" in Vivado.

3 Specifications

3.1 General

- 2-lane PCIe Gen2
- Xilinx Zynq-7000 FPGA (XC7Z030-1FBG676C) with Dual-Core ARM processor integrated
- Possible upgrade to XC7Z035-1FBG676C or XC7Z045-1FBG676C
- 4 GTX Transceivers (2 used for PCIe, 1 for SFP, 1 external accessible)
- 2 GTX Reference Clocks (1 for PCIe, 1 for WR Clock)
- FMC slot with High Pin Count (HPC) connector (only fully populated as LPC)
- Z035 and Z045 support 4 GTX transceivers DP[3:0]_M2C/C2M an 2 extra GTX Reference Clocks
- JTAG accessible from the FPGA. JTAG switches automatically to the download cable when it is plugged.

3.2 Clocking resources

- 1x Fixed frequency 33.33 MHz oscillator for Application Processor Unit (APU)
- 1x 10-280 MHz VCXO controlled by I2C and a DAC with SPI interface. Starts up at 125 MHz (Silicon Labs Si570/Si571, freely usable)
- 1x 125.000 MHz VCXO controlled by a DAC with SPI interface (used by White Rabbit PTP core)
- 1x 124.992 MHz VCXO controlled by a DAC with SPI interface (used by White Rabbit PTP core)
- Low jitter external 10MHz via LTC6950 (supporting mode Grand Master & AbsCal)
- 10MHz TCXO for IEEE1588 v2.1 compliance (see J5.6.1) in Free-running Master mode.

3.3 On board memory

- 1x 8 Gbit (1 GByte) DDR3 connected to the 32-bit wide Memory Interface (main use for the APU)
- 1x 8 Gbit (1 GByte) DDR3 connected to the programmable logic (32 bit wide)
- 2x QSPI 256 Mbit flash PROM for multi-boot FPGA power-up configuration, storage of the FPGA firmware.
- 64K (8K x 8-bit) I2C Serial EEPROM (24AA64T-I/MC) for storing serial number, calibration parameters and other critical data such as the MAC address of the card
- 2x 2K (128 x 8-bit) I2C Serial EEPROM (24AA025E48) which provides EUI-48 (2 MAC addresses for APU and for WR)
- MicroSD slot for flash memory for storing programs

3.4 Miscellaneous

- Thermometer (XADC) and semi-unique ID (DNA_PORTE2) provided by the FPGA

3.5 Front panel containing

- 1x Small Formfactor Pluggable+ (SFP+) cage for fiber-optic transceiver (WhiteRabbit support).
- Programmable Red and Green LEDs
- FMC front panel

3.6 Internal connectors

- 1x JTAG header for Xilinx programming during debugging
- 1x mini USB Type B connector (serves 2 UARTs, one UART interface of the ARM and one to user logic, e.g. PTP core; Warning! See chapter 1.)
- 1x USB Type A connector connected to USB 2.0 port of the ARM
- Ethernet RJ45 connector, magnetics and MicroChip KSZ9031RNX, 10/100/1000 Mbps PHY (interface to ARM GigE)
- Samtec Bulls Eye connector (BDRA)
- 2x connector for optional cooling fans
- FPGA configuration via JTAG header, via ARM (i.e. Dual QSPI or using [PS PCAP / ICAP](see chapter 6.1.8 Zynq-7000 SoC Technical Reference Manual)

3.7 Stand-alone features

- External 12V 150W-ATX power supply connector
- USB Type A connector
- mini USB Type B connector (Warning! See chapter 1.)
- 10/100/1000 Mbps copper Ethernet RJ45
- SFP+ cage for fibre-optic transceiver(White Rabbit support)
- 7x LEDs (2x front panel, 4x on PCB, 1x PCI SMB-bus)
- 5x buttons
- 1 PS_POR connected to reset controller
- 1 PS_SRTS_B
- 1 PL system reset
- 1 general purpose
- 1 PROGram button for FPGA

4 SPEC7 Firmware

4.1 SPEC7 reference design and SPEC7 HPSEC design

There are two designs, a SPEC7 reference design and a SPEC7 HPSEC design that have many things in common. Figure 6 is a block diagram which that focuses on the PCIe connections common to both.

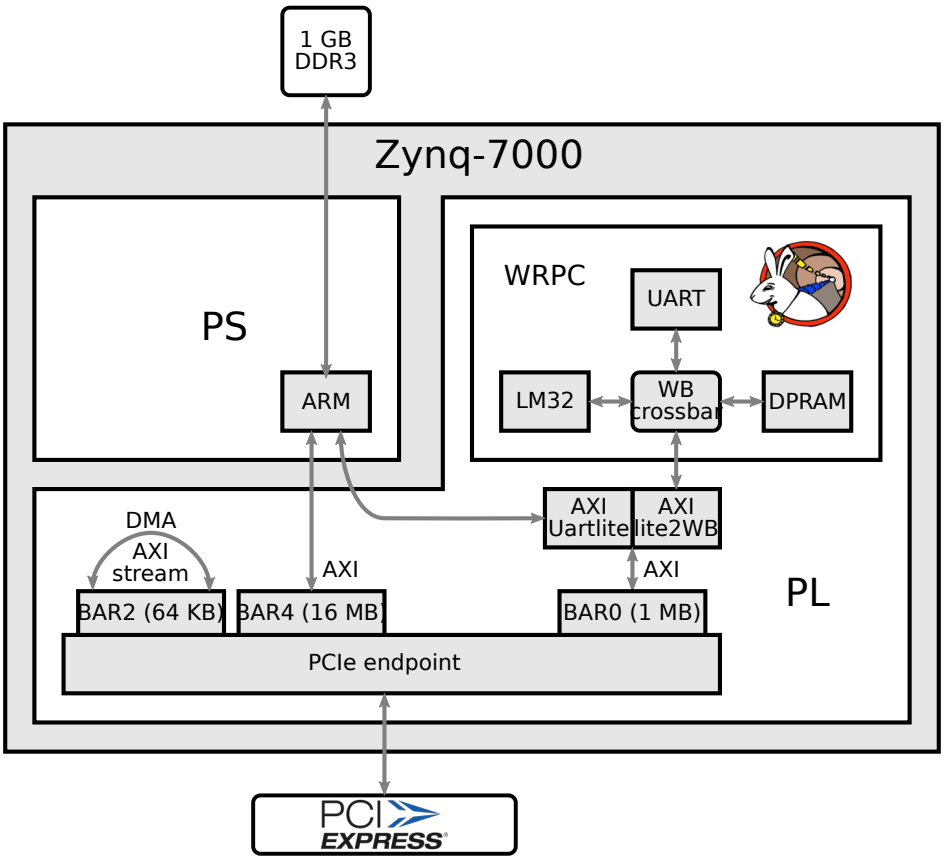


Figure 6: PCIe block diagram.

As explained in the introduction (see: 2.1) the Zynq FPGA contains a Processing System (PS) and a Programmable Logic (PL) section. A basic processing system is a minimum requirement for FPGA configuration from QSPI (see also Appendix C).

The PCIe endpoint, located in PL, has three BARs:

- BAR0 (1 MB) is divided in two 512 KB sections. The lower 512 KB of the address space is connected to A WR PTP Core (WRPC [7]). This connection enables direct access to the DPRAM (that contains the LM32 executable), the virtual UART and other registers that are mapped on the WRPC wishbone bus (for details, please refer to [7]). The upper 512 KB of the address space is reserved. Currently 64 KB (of which only a small portion is used) is connected to a UART that enables a connection to UBoot-UART1 via PCIe.
- BAR2 (64 KB) is connected to a DMA engine that is looped back via its AXI stream interface. For the time being, it is implemented for test purposes.

- BAR4 (16 MB) is mapped to DDR memory via the PS. This enables to write PL configuration file from PCIe to DDR such that PL can be configured from DDR using UBoot.

4.1.1 SPEC7 reference design

The SPEC7 reference design operates the SPEC7 like users were used to with the SPEC [5] reference design. A Digital IO FMC [6] can be plugged onto the SPEC7 so 1PPS/10MHz in and 1PPS out signals are available. Table 4 shows which reference design signal is assigned to what DIO LEMO connector.

DIO LEMO nr.	Reference design signal	direction
1	PPS	out
2	n.a.	n.a.
3	abscal_txts	out
4	PPS	in
5	10 MHz	in

Table 4: DIO LEMO connector reference design signal assignment.

4.1.2 SPEC7 HPSEC design

The SPEC7 reference design operates the SPEC7 without DIO card. The design aims for lower phase noise than the "standard" SPEC7 reference design. Differential timing signals (PPS and 10MHz) are routed to the Bulls Eye connector J4. The PPS out signal is re-clocked to remove FPGA switching phase noise. In Grand Master mode the design accepts 10MHz and 1PPS input via connector J4.

Bulls Eye connector J4 provides a well defined high bandwidth connection to the outside world. It should be used when the SPEC7 is deployed in demanding applications where users aim for the highest quality signals, for example when SPEC7 is used in combination with a high precision external oscillator (like the HPSEC design [3]).

4.2 HDL synthesis

Before running the synthesis process you have to make sure your environment is set up correctly. You will need Vivado 2019.2 from your Xilinx vendor.

4.2.1 Downloading the sources

The SPEC7 sources are part of the wr-cores repository. Usualy the *hdlmake* tool is used to gather the sources needed to build the firmware. Unfortunately *hdlmake* does not support *.tcl*, "Block Memory Mapping" (*.bmm*) or Memory Mapping Information (*.mmi*) files. Tcl scripting is needed for automatic ARM processing system block diagram generation. The *.bmm* and *.mmi* files are needed to merge software into the FPGA configuration bitfile without the need for re-synthesis of the firmware.

A top SPEC7 repository facilitates the above. The wr-cores repository, containing the sources, is its submodule:

```
git clone https://ohwr.org/project/spec7.git
cd spec7
git checkout proposed_master
git submodule init
git submodule update
cd hdl/wr-cores
git submodule init
git submodule update
```

Synthesis is started in the corresponding project *syn* directory. It is important to source the script from the project/syn directory because it contains the project specific files:

- *proj_properties.tcl*: project specific settings (for example target FPGA)
- *proj_file_list.txt*: list of files needed by the project (i.e. the output of *hdlmake list-files* plus a few files that are not supported by *hdlmake*.)

4.2.2 Building the SPEC7 reference design

To build the firmware for the reference design:

```
%cd hdl\syn\spec7_ref_design
```

Start Vivado and source the tcl script.

```
vivado
%source ..\..\..\sw\scripts\viv_do_all.tcl
```

Synthesis en bitfile generation may take quite some time. If the process is successful then you will end up with:

- *spec7_ref_design_z035_YYDDMM_HHMM.bit*
- *spec7_ref_design_z035_YYDDMM_HHMM.mmi*
- *spec7_ref_design_z035_YYDDMM_HHMM.log*

in the syn directory, where YYMMDD_HHMM is the build date and time. The *.log* file contains the SHA codes from the repositories and sub-modules that were used for the build.

4.2.3 Building the SPEC7 HPSEC design

The SPEC7 reference design operates the SPEC7 without DIO card. Timing signals are routed to the Bulls Eye connector J4. In Grand Master mode the design accepts 10MHz and 1PPS input via this connector. The design also generates 10MHz and 1PPS out via this connector.

```
%cd hdl\syn\spec7_ref_design
```

Edit "proj_properties.tcl" to select the HPSEC design for build:

```
# ====================================================
# SELECT DESIGN TO BUILD:
# ====================================================
# Reference Design (using fmc-dio-5chttla => https://ohwr.org/project/fmc
    -dio-5chttla/wikis/home)
# HPSEC Design (using Bulls-Eye connector)
#set spec7_design spec7_ref_top
set spec7_design spec7_hpsec_top
# ====================================================
```

Start Vivado and source the tcl script.

```
vivado
%source ..\..\..\sw\scripts\viv_do_all.tcl
```

If the process is successful then you will end up with:

- *spec7_hpsec_design_z035_YYDDMM_HHMM.bit*
- *spec7_hpsec_design_z035_YYDDMM_HHMM.mmi*
- *spec7_hpsec_design_z035_YYDDMM_HHMM.log*

in the syn directory, where YYMMDD_HHMM is the build date and time. The *.log* file contains the SHA codes from the repositories and sub-modules that were used for the build.

4.2.4 Merging .bit and .elf files

The Vivado installation is contains an *updatemem* command. An FPGA configuration *.bit* file that contains a memory space (like the LM32 memory embedded in wr-cores) can be updated with new memory content (i.e. executable software) using *updatemem*. In order to be able to do this, *updatemem* needs information to locates all BRAM blocks that build up the memory space. This information is provided by the generated Memory Mapping Information *.mmi* file. One can merge new compiled software in Executable Loader Format *.elf* with the *.bit* without the need for time consuming re-synthesis. A script is available to merge an *.elf* file with a *.bit* and *.mmi* file using *updatemem*.

First get into the project directory; the location of the new build *.bit* and *.mmi*.

```
cd ..
```

next

```
..\..\sw\scripts\do_vivado_mmi_elf.cmd <bitfile>.bit <elffile>.elf
```

which will generate a *bitfile_elf.bit*.

5 Connector pinout

This section describes the various connectors which are available on the SPEC7.

5.1 J4: Samtec Bulls Eye connector

Table 5 shows the pinout of Bulls Eye connector J4. The pin number assignment is show in figure 7. On the PCB the connector is just a land pattern that accepts a Samtec BDRA assembly (see figure 8).

To order a BDRA assembly the following part number is recommended BDRA-92SPP-02-12-0500 (12 pairs, 2.0 ps phase matched, 2.92 mm Straight Plug, length 0.5 m). Individual coaxial cables cables (BE23) can be extracted by a special tool with part number CAT-EX-SCC-03.

Pin Nr	Description	Levels	Note
A1	P PPS_OUT	LVPECL	DC coupled
A2	N PPS_OUT	LVPECL	DC coupled
A3	P 10 MHz_OUT	LVPECL	AC coupled
A4	N 10 MHZ_OUT	LVPECL	AC coupled
A5	P 125 Reference Clock out	LVPECL	AC coupled
A6	N 125 Reference Clock out	LVPECL	AC coupled
A7	P TX Spare GTX OUT		AC coupled
A8	N TX Spare GTX OUT		AC coupled
A9	P ABSCAL_TXTS OUT	LVDS	DC coupled
A10	N ABSCAL_TXTS OUT	LVDS	DC coupled
A11	P General Purpose Spare out		
A12	N General Purpose Spare out		
B1	P PPS_IN		
B2	N PPS_IN		
B3	P 10 MHz_IN		
B4	N 10 MHz_IN		
B5	P Reference Clock in GTX		
B6	N Reference Clock in GTX		
B7	P RX Spare in GTX		
B8	N RX Spare in GTX		
B9	P DMTD Spare IN		
B10	N DMTD Spare I		
B11	PPS IN Single ended	5V TTL	DC coupled
B12	NC	Not Routed	

Table 5: J4, Samtec bulls eye connector

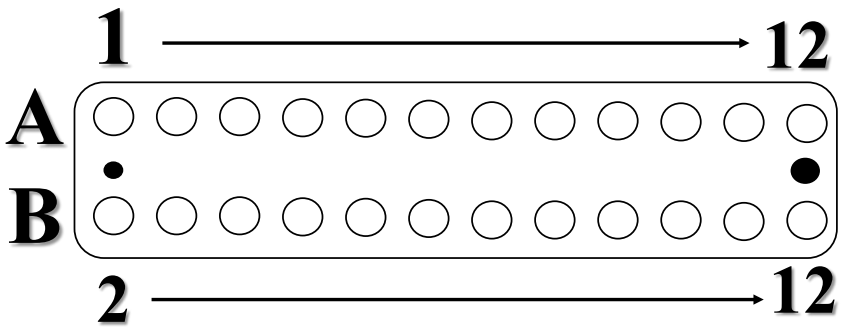


Figure 7: Top view bulls eye connector.

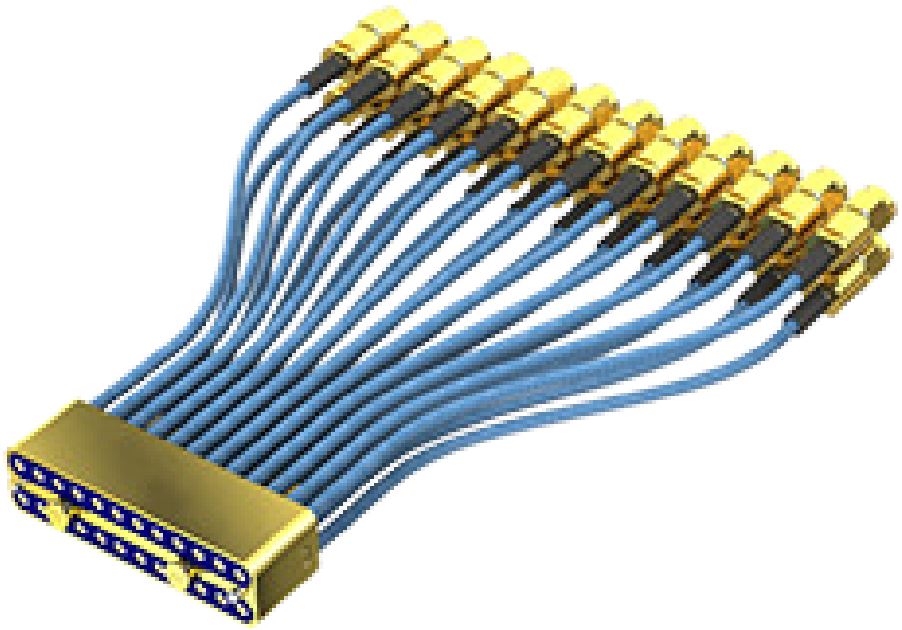


Figure 8: BDRA assembly.

5.2 X4: ATX power connector

The SPEC7 can be powered stand-alone via connector X14 which is compliant with the PCI Express x16 Graphics 150W ATX specification see [9], [10]. Additional power may also be applied via X4 when the maximum allowed PCI-express slot power, that can be delivered by the motherboard, is exceeded. Molex part number 0455590002 is recommend as mating connector. Maximum input voltage and current ratings are stated in the following chapter 8

Pin Nr	Description	Remark
1	Power	12V
2	Power	NC
3	Power	12V
4	GND	Power return
5	Sense0	Not Used
6	GND	Power return

Table 6: 6-position cable assembly

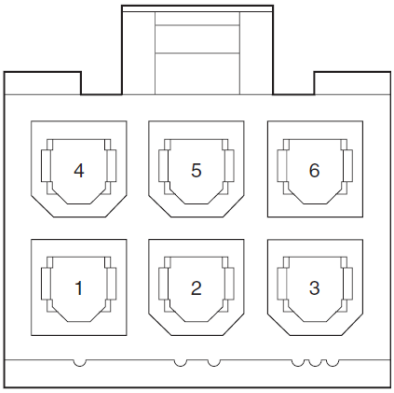


Figure 9: Power connector (Molex PartNo. 0455590002).

5.3 J3: FMC connector

In order to be compatible with the previous version of the SPEC [5] Vadj is fixed to 2,5V. Note that the IO lines of the FMC connector have no additional ESD protection. Therefore, please respect ESD rules.

The FMC connector is fully populated according to the Low Pin Count (LPC) signal definitions [8]. The SPEC7 FMC connector is a High Pin Count (HPC) type which allows for the possibility to access 4 additional GTX transceivers on signal pins DP[3:1]. The pin list is show in table 7 and the pin potions are shown in figure 10.

Table 7: Pinout FMC

Pin Nr	Pin Name	remark	Pin Nr	Pin Name	Remark
A1	DGND		B1	-	NC
A2	DP1_M2C_P		B2	DGND	
A3	DP1_M2C_N		B3	DGND	
A4	DGND		B4	-	NC
Continued on next page					

Table 7 – continued from previous page

Pin Nr	Pin Name	remark	Pin Nr	Pin Name	Remark
A5	DGND		B5	-	NC
A6	DP2_M2C_P		B6	DGND	
A7	DP2_M2C_N		B7	DGND	
A8	DGND		B8	-	NC
A9	DGND		B9	-	NC
A10	DP3_M2C_P		B10	DGND	
A11	DP3_M2C_N		B11	DGND	
A12	DGND		B12	-	NC
A13	DGND		B13	-	NC
A14	-	NC	B14	DGND	
A15	-	NC	B15	DGND	
A16	DGND		B16	-	NC
A17	DGND		B17	-	NC
A18	-	NC	B18	DGND	
A19	-	NC	B19	DGND	
A20	DGND		B20	-	NC
A21	DGND		B21	-	NC
A22	DP1_C2M_P		B22	DGND	
A23	DP1_C2M_N		B23	DGND	
A24	DGND		B24	-	
A25	DGND		B25	-	
A26	DP2_C2M_P		B26	DGND	
A27	DP2_C2M_P		B27	DGND	
A28	DGND		B28	-	NC
A29	DGND		B29	-	NC
A30	DP3_C2M_P		B30	DGND	
A31	DP3_C2M_P		B31	DGND	
A32	DGND		B32	-	NC
A33	DGND		B33	-	NC
A34	-	NC	B34	DGND	
A35	-	NC	B35	DGND	
A36	DGND		B36	-	NC
A37	DGND		B37	-	NC
A38	-	NC	B38	DGND	
A39	-	NC	B39	DGND	
A40	DGND		B40	-	NC
C1	DGND		D1	PG_C2M	
C2	DP0_C2M_P		D2	DGND	
C3	DP0_C2M_N		D3	DGND	
C4	DGND		D4	GBTCLK0_M2C_P	
C5	DGND		D5	GBTCLK0_M2C_N	
C6	DP0_M2C_P		D6	DGND	
C7	DP0_M2C_N		D7	DGND	

Continued on next page

Table 7 – continued from previous page

Pin Nr	Pin Name	remark	Pin Nr	Pin Name	Remark
C8	DGND		D8	LA01_CC_P	
C9	DGND		D9	LA01_CC_N	
C10	LA6_P		D10	DGND	
C11	LA6_N		D11	LA05_P	
C12	DGND		D12	LA05_N	
C13	DGND		D13	DGND	
C14	LA06_P		D14	LA09_P	
C15	LA06_N		D15	LA09_N	
C16	DGND		D16	DGND	
C17	DGND		D17	LA13_P	
C18	LA14_P		D18	LA13_N	
C19	LA14_N		D19	DGND	
C20	DGND		D20	LA17_CC_P	
C21	DGND		D21	LA17_CC_N	
C22	LA18_CC_P		D22	DGND	
C23	LA18_CC_N		D23	LA23_P	
C24	DGND		D24	LA23_N	
C25	DGND		D25	DGND	
C26	LA27_P		D26	LA26_P	
C27	LA27_N		D27	LA26_N	
C28	DGND		D28	DGND	
C29	DGND		D29	TCK	
C30	FMC_SCL		D30	ZYNQ_TDO_FMC_TDI	
C31	FMC_SDA		D31	CONN_TDO	
C32	DGND		D32	3V3_FMC	Power
C33	DGND		D33	TMS	
C34	DNGD		D34	TRST_L	
C35	12V	Power	D35	DGND	
C36	DGND		D36	3V3_FMC	Power
C37	12V	Power	D37	DGND	
C38	DGND		D38	3V3_FMC	Power
C39	3V3_FMC	Power	D39	DGND	
C40	DGND		D40	3V3_FMC	Power
E1	DGND		F1		
E2	-	NC	F2		
E3	-	NC	F3		
E4	DGND		F4		
E5	DGND		F5		
E6	-	NC	F6		
E7	-	NC	F7		
E8	DGND		F8		
E9	-	NC	F9		
E10	-	NC	F10		

Continued on next page

Table 7 – continued from previous page

Pin Nr	Pin Name	remark	Pin Nr	Pin Name	Remark
E11	DGND		F11		
E12	-	NC	F12		
E13	-	NC	F13		
E14	DGND		F14		
E15	-	NC	F15		
E16	-	NC	F16		
E17	DGND		F17		
E18	-	NC	F18		
E19	-	NC	F19		
E20	DGND		F20		
E21	-	NC	F21		
E22	-	NC	F22		
E23	DGND		F23		
E24	-	NC	F24		
E25	-	NC	F25		
E26	DGND		F26		
E27	-	NC	F27		
E28	-	NC	F28		
E29	DGND		F29		
E30	-	NC	F30		
E31	-	NC	F31		
E32	DGND		F32		
E33	-	NC	F33		
E34	-	NC	F34		
E35	DGND		F35		
E36	-	NC	F36		
E37	-	NC	F37		
E38	DGND		F38		
E39	-	NC	F39		
E40	DGND		F40		
G1			H1		
G2			H2		
G3			H3		
G4			H4		
G5			H5		
G6			H6		
G7			H7		
G8			H8		
G9			H9		
G10			H10		
G11			H11		
G12			H12		
G13			H13		

Continued on next page

Table 7 – continued from previous page

Pin Nr	Pin Name	remark	Pin Nr	Pin Name	Remark
G14			H14		
G15			H15		
G16			H16		
G17			H17		
G18			H18		
G19			H19		
G20			H20		
G21			H21		
G22			H22		
G23			H23		
G24			H24		
G25			H25		
G26			H26		
G27			H27		
G28			H28		
G29			H29		
G30			H30		
G31			H31		
G32			H32		
G33			H33		
G34			H34		
G35			H35		
G36			H36		
G37			H37		
G38			H38		
G39			H39		
G40			H40		
J1	DGND		K1		
J2	-	NC	K2		
J3	-	NC	K3		
J4	DGND		K4		
J5	DGND		K5		
J6	-	NC	K6		
J7	-	NC	K7		
J8	DGND		K8		
J9	-	NC	K9		
J10	-	NC	K10		
J11	DGND		K11		
J12	-	NC	K12		
J13	-	NC	K13		
J14	DGND		K14		
J15	-	NC	K15		
J16	-	NC	K16		

Continued on next page

Table 7 – continued from previous page

Pin Nr	Pin Name	remark	Pin Nr	Pin Name	Remark
J17	DGND		K17		
J18	-	NC	K18		
J19	-	NC	K19		
J20	DGND		K20		
J21	-	NC	K21		
J22	-	NC	K22		
J23	DGND		K23		
J24	-	NC	K24		
J25	-	NC	K25		
J26	DGND		K26		
J27	-	NC	K27		
J28	-	NC	K28		
J29	DGND		K29		
J30	-	NC	K30		
J31	-	NC	K31		
J32	DGND		K32		
J33	-	NC	K33		
J34	-	NC	K34		
J35	DGND		K35		
J36	-	NC	K36		
J37	-	NC	K37		
J38	DGND		K38		
J39	-	NC	K39		
J40	DGND		K40		

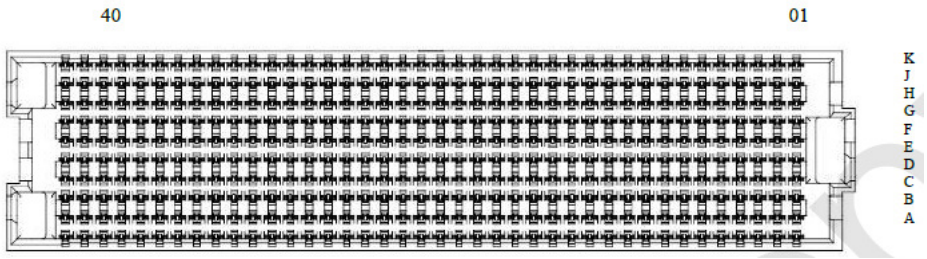


Figure 10: FMC Connector J3.

6 Measured Data

The following chapter presents measured results. All measurements are done with the default firmware for the SPEC7.

6.1 Phase Noise

The following setup is used to measure the phase noise of the SPEC7 card as shown in figure 11. For more information about the custom 125 MHz reference generator see appendix A. Phase noise is measured at point C using a Rohde&Schwarz phase noise analyzer (FSWP). Point C is the Bulls Eye connector.

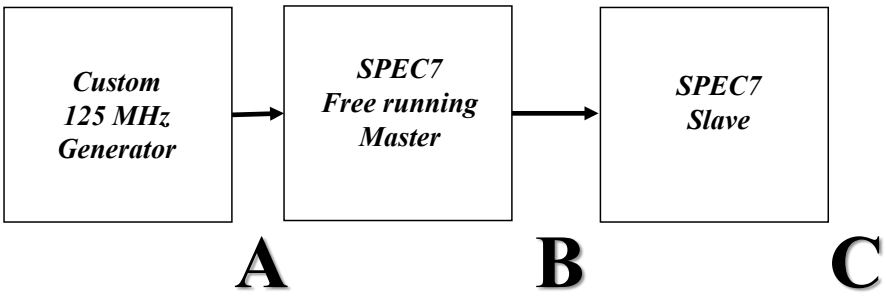


Figure 11: Phase noise measurement setup

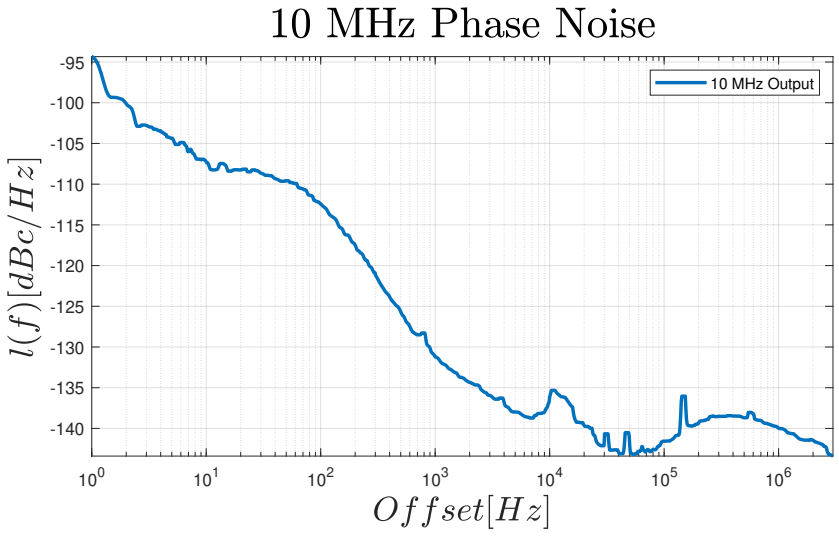


Figure 12: Phase noise 10 MHz output (J4 A03/A04).

A small bump around 13 KHz can be seen in the phase noise plot of figure 12. The cause of the phase noise around 13KHz can also be seen in the spectrum and spectrogram of figure 13. The noise sources are the 2V5 and 1V8 Switched Mode Power Supplies (N6, N5: Intel EN6347QA). Keep in mind that this noise has no major effect since it only reaches -135 dBc/Hz over a limited bandwidth.

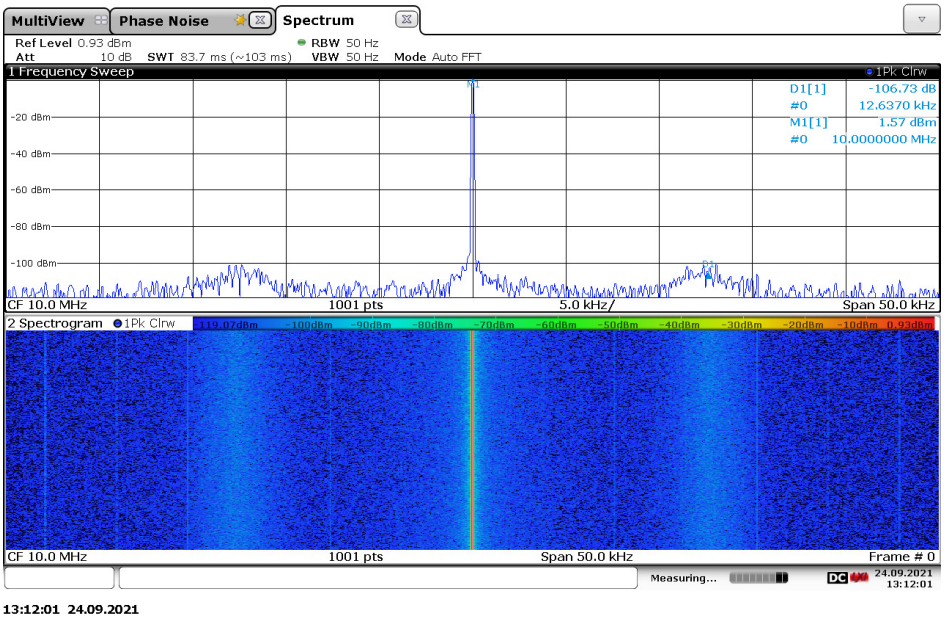


Figure 13: Spectrum of the 10 MHz with some noise at 13 KHz distance from the carrier.

The phase noise between 10^5 and 10^6 in figure 12 is caused by the 500 MHz MMCME2_ADV PLL in the FPGA that is used in the spec7_ref_design to create a White Rabbit phase aligned 10MHz.

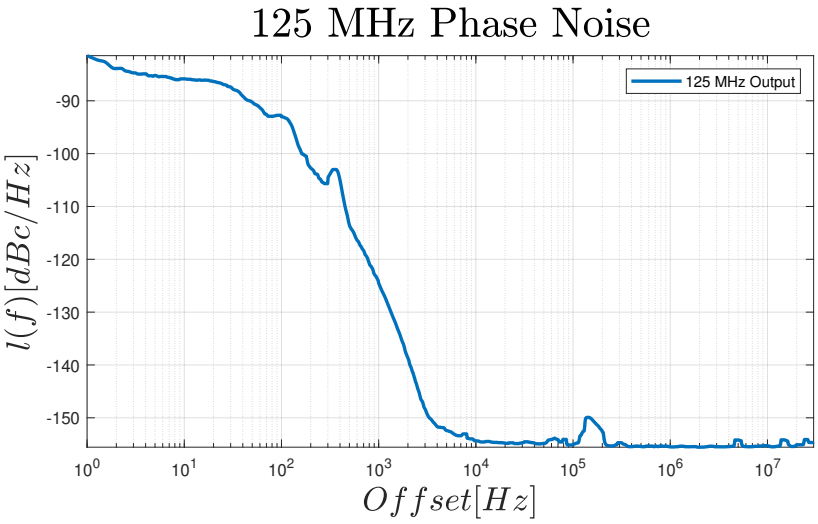


Figure 14: Phase noise 125 MHz output (J4 A05/A06).

6.2 Spurs

The figures below show the frequency spectrum for the 10 MHz and 125 MHz outputs.

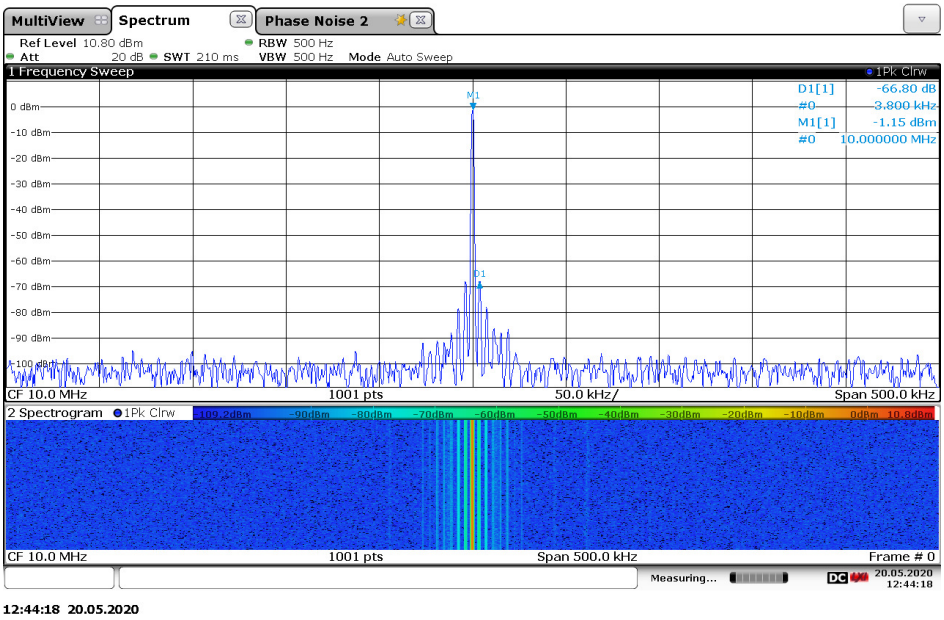


Figure 15: Spectrum 10 MHz Output.

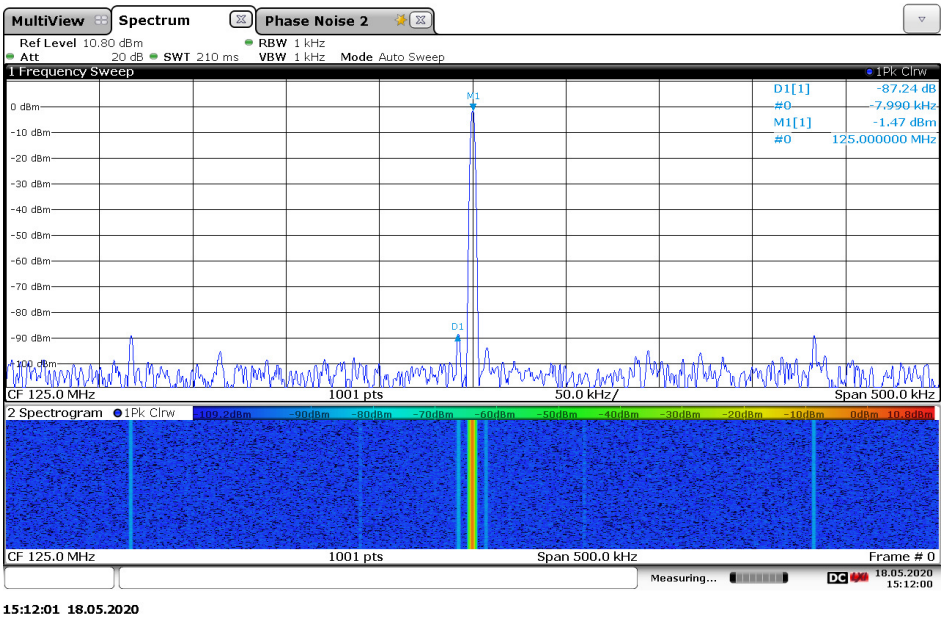


Figure 16: Spectrum 125 MHz Output.

6.3 Time Domain

allen dev plot

6.4 Restart Error

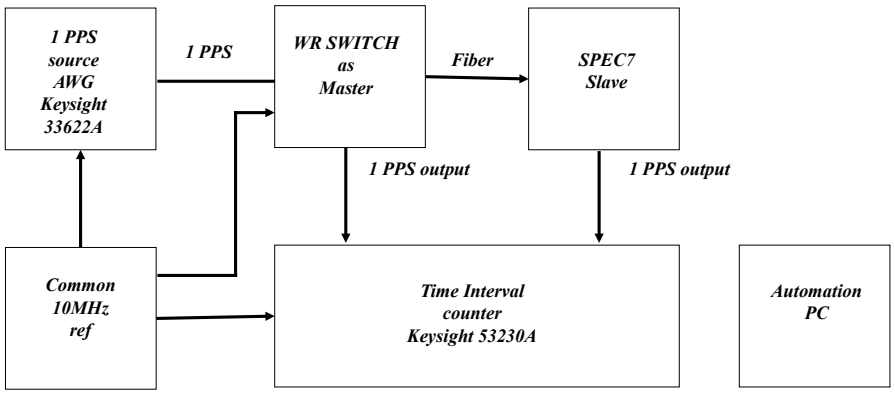


Figure 17: PPS Restart Error measurement setup.

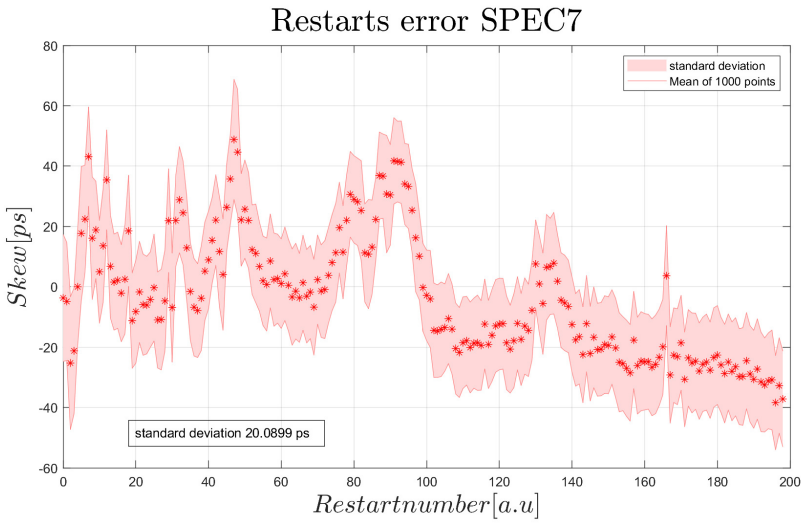


Figure 18: PPS Restart Error.

6.5 PPS Pulse to Pulse Jitter

6.6 Boot time on board flash memory

The SPEC7 is capable of booting from a dual Quad-SPI flash memory setup. Two Micron [2] chips (2x MT25QL256ABA8E12-1SIT in a Dual QUAD SPI configuration) are present on the card and connected to the Zynq Processor System. The SPEC7 can reach boot times down to 735 milliseconds. This can be seen in figure 19, where the 12V supply voltage (red) is depicted along an user application (green), the yellow line is a probed qspi clock signal to display when the memory is being accessed.

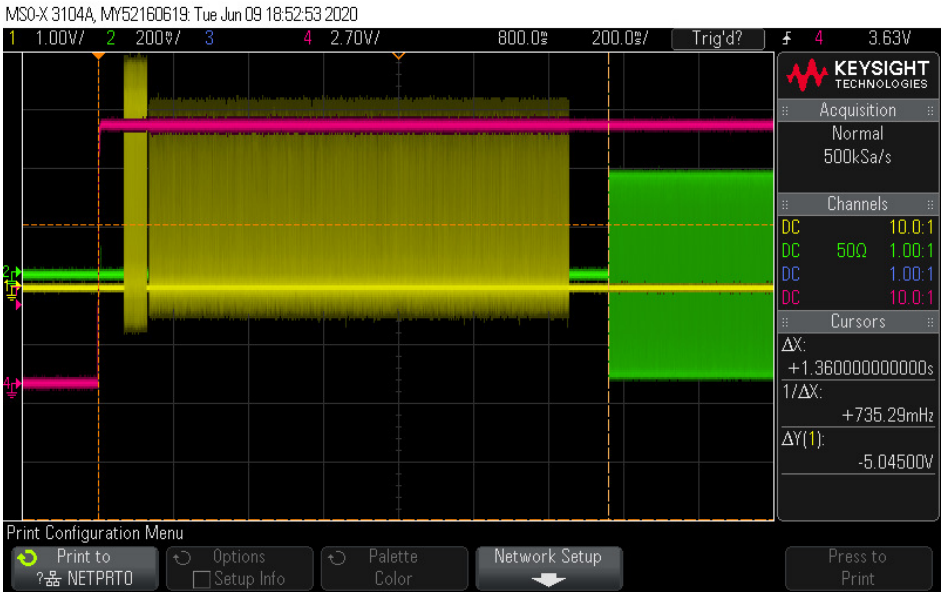


Figure 19: QPSI boot time of an uncompressed bitfile. Notice how the QSPI clock signal (yellow) is divided into two "stages". The first is the Bootloader being loaded into the Zynq, the second stage is the bitstream being loaded into the programmable logic.

These 735 milliseconds are currently a worst case scenario. Boot times can be greatly reduced by enabling bitsream compression [13], along with other optimizations [12]. An example of booting a compressed bitstream is depicted in figure 20 where the boot time is reduced to 265 milliseconds.

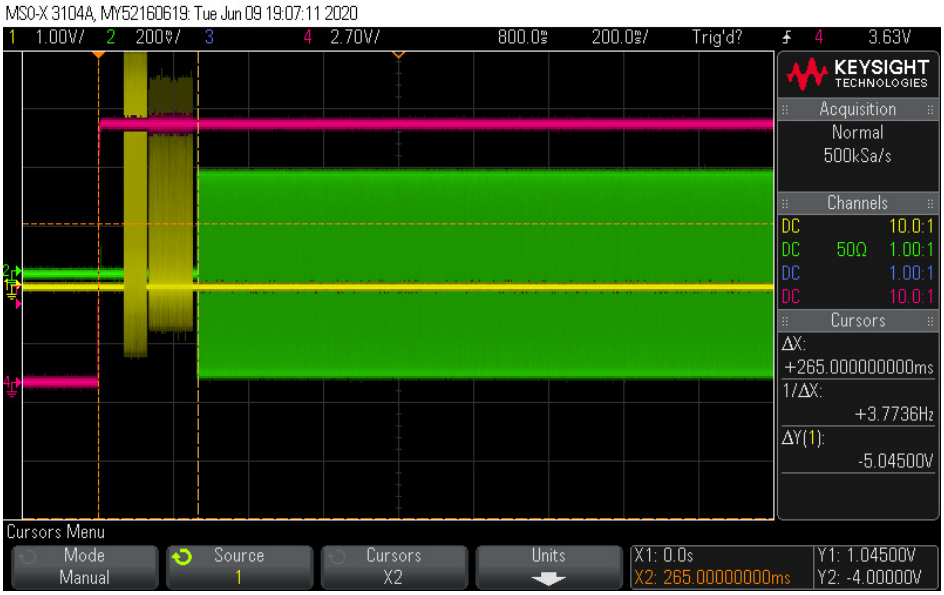


Figure 20: QPSI boot time of an compressed bitfile.

7 PCIe interface

The PCIe interface is only tested on the physical level for transaction rates 2.5GT/sec and 5GT/sec. The device under test is a Zynq Z035 device. The 2.5GT/sec eye diagram is shown in figure 21. The 5GT/sec eye diagram is shown in figure 22.

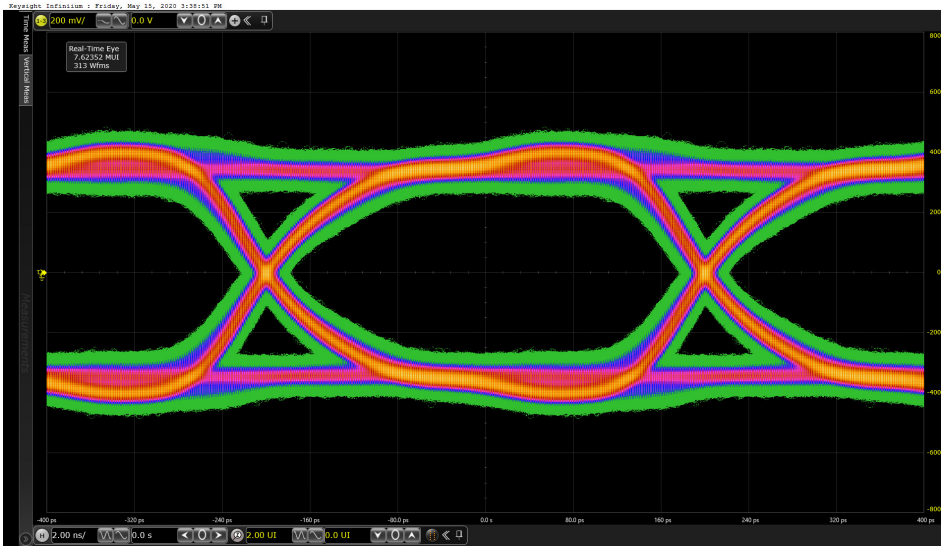


Figure 21: PCIe 2.5GT/sec eye diagram.

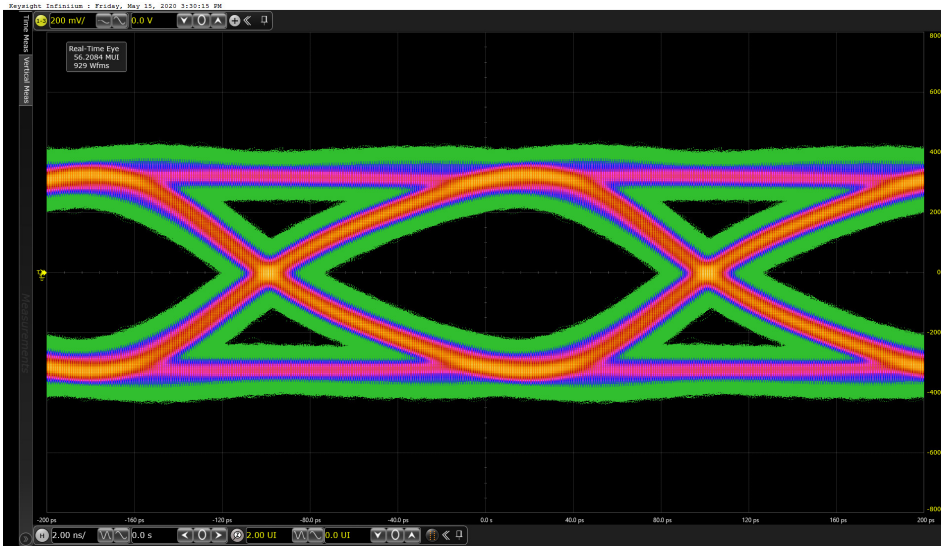


Figure 22: PCIe 5GT/sec eye diagram.

More information about the test setup can be found in appendix D

Figure 23 shows the SPEC7 being recognized by the oprerating system (i.e. "lspci").

```
01:00.0 Serial controller: Xilinx Corporation Device 7022 (prog-if 01 [16450])
        Subsystem: Xilinx Corporation Device 0007
        Flags: fast devsel, IRQ 16
        Memory at f7000000 (64-bit, non-prefetchable) [virtual] [size=1M]
        Memory at f7100000 (64-bit, non-prefetchable) [virtual] [size=64K]
        Memory at f6000000 (32-bit, non-prefetchable) [virtual] [size=16M]
        Capabilities: <access denied>
        Kernel driver in use: spec7
        Kernel modules: spec7
```

Figure 23: Example result of lspci: SPEC7 is recognized

8 Power & Maximum Ratings

8.1 Power Ratings

Description	Value	Unit	Tolerance	Note
Input voltage Range	12	V	+/-5%	
Absolute Maximum input voltage	12.65	V		Note 1
Nominal current draw	1	A		Note 2

Table 8: ATX power connector

1. **Stress above the stated voltage will damage the SPEC7 and/or a possible connected FMC mezzanine.**
2. **The stated current is only when a a White rabbit core is loaded, the actual current consumption heavily depends on your end application**

8.2 Power Up Sequence

The SPEC7 can either be powered when plugged into a PCIe slot or it can be used stand alone by using an external 12V power supply. When plugged into a PCI slot then the main power of the SPEC7 is derived from 12V on the PCIe connector while the FMC card is powered by 3V3 on the PCIe connector. This is done in order not to exceed the maximum power that may be drawn per PCIe slot.

Many different voltages are needed by the Zynq FPGA and DDR3 memories. The power supplies are enabled sequentially. Figure 24 shows the power sequence after 12V is applied. First 3V3 non-switched (3V3_NWS) is created by the 10A switched mode power supply N2. Next 1V35 is enabled which serves as a pre-regulator for the 1V0 VCCINT regulator. Finally VCCINT is supplied by a linear regulator in order to create a low noise 1V0 voltage since the phase noise performance of the FPGA depends on the quality of VCCINT.

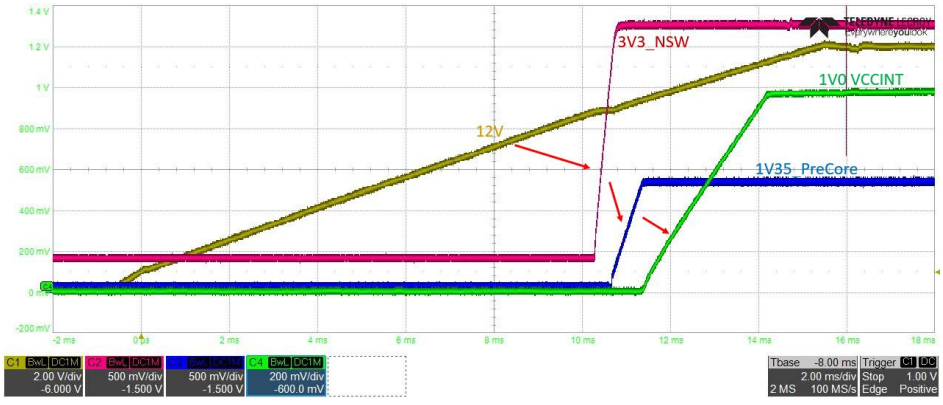


Figure 24: Power Sequence: 12V input ⇒ 3V3 Non Switched ⇒ 1V35 PreCore ⇒ 1V0 VCCINT

Figure 25 shows the power sequence of power supplies for the FPGA. After VCCINT is applied then the FPGA BANK voltages 1V8, 1V35 and 2V5 are supplied.

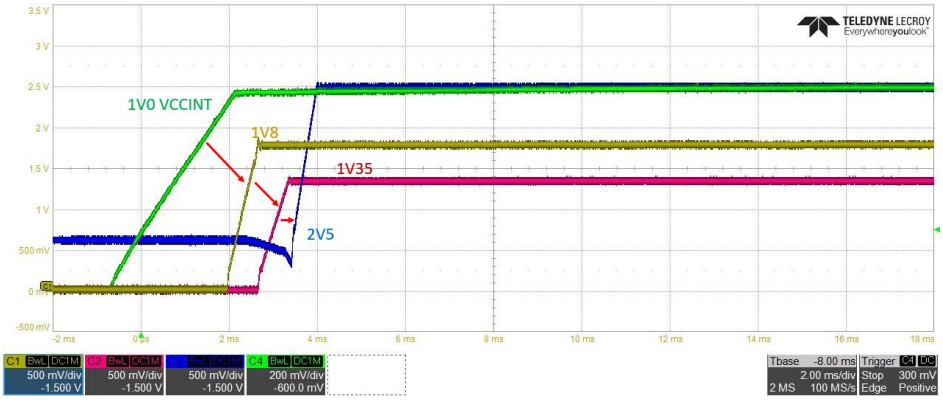


Figure 25: Power Sequence: 1V0 VCCINT ⇒ 1V8 ⇒ 1V35 ⇒ 2V5

When all FPGA voltages are supplied then finally 3V3 is enabled. In order to lower the inrush current MOSFET V3 is switched on gradually as can be seen in figure 26

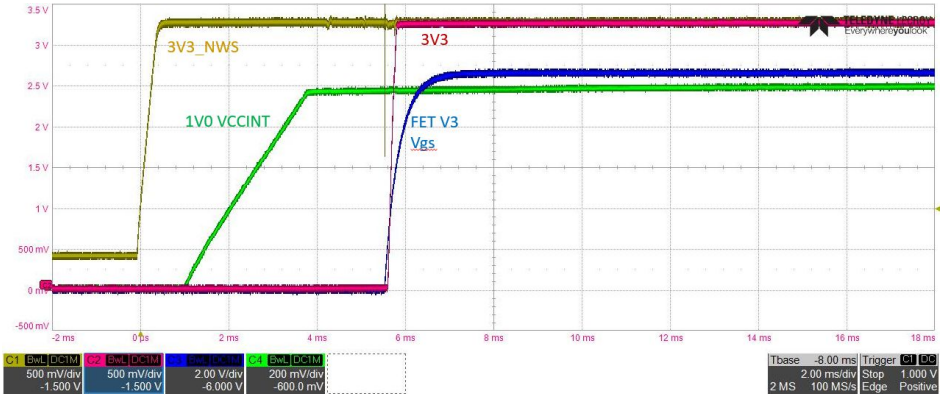


Figure 26: Gradually turn on V3 to enable 3V3

Depending on whether the SPEC7 is powered by a PCIe slot or by an external power supply, either MOSFET V2 or V4 is gradually switch on to enable 3V3 for the FMC card (see figure 27)

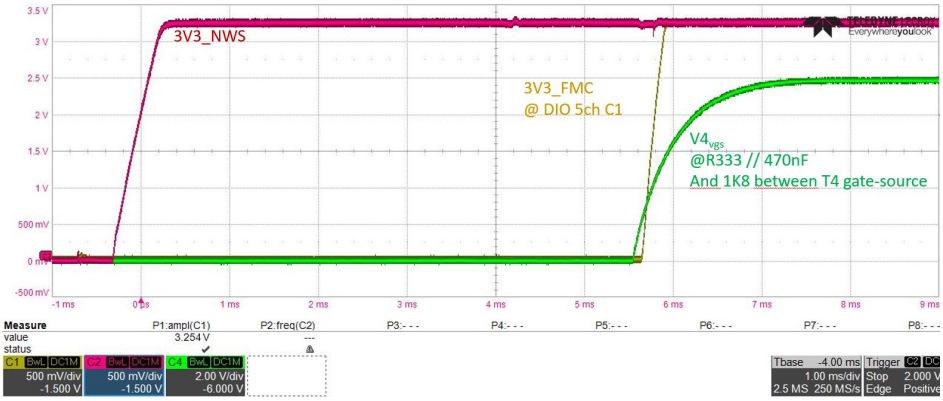


Figure 27: Gradually turn on V4 to enable 3V3 for the FMC card

8.3 Power Down Sequence

Xilinx DS191 [11] paragraph "PS Power-On/Off Power Supply Sequencing" states: "Before VCCINT reaches 0.80V the reference clock to the PS_CLK input is disabled to ensure PS eFUSE integrity." Figure 28 shows that this condition is met.

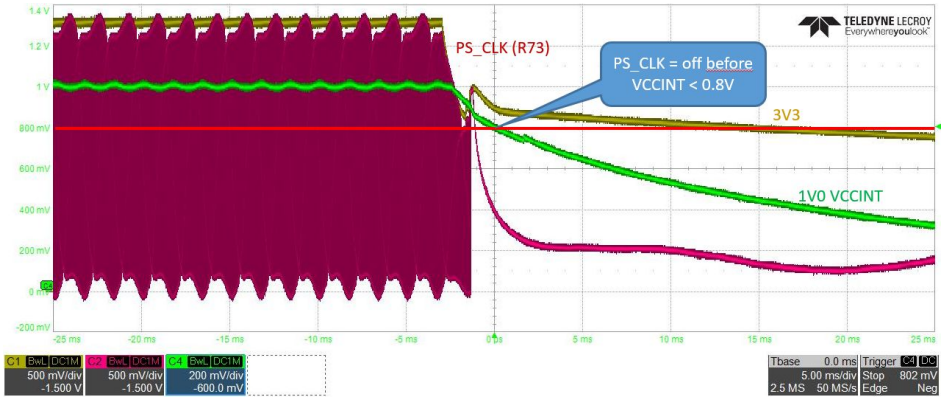


Figure 28: Power Down Sequence

9 Optional Heatsink, Fans and RF-Shielding

The SPEC7 may be optionally be equipped with a heatsink, fans or an Clip-On EMI Shielding Can. Table 9 shows manufacturers and part numbers that will fit the SPEC7 design.

9.1 Heatsink

Depending on the application the Zynq FPGA on the SPEC7 may need a heatsink and/or a fan. The type of heatsink that will fit on the SPEC7 is a "Square Skived Fin 5ommx50mm, Height=14mm, mounted on PCB", Manufacturer AAVID, Part Number 342943 (see figure 29). Note that the total height of the heatsink (14 mm) plus Zynq (2.44 mm) is now 16.44 mm while the PCIe specification restricts the total height to 14.47mm. Unfortunately this is inevitable since a market survey showed that there were no other suitable cooling profiles found on the market. If a cooling profile is necessary and the total height poses a problem then a work around is to mill-off 2 mm from the profile.

Figure 29: Heatsink AAVID 342943

9.2 Fans

A 5V DC fan for the FPGA can be connected to connector X3. The FPGA fan can be controlled via FPGA pin AD26.

For FMC cards that need cooling, a 5V DC fan can be mounted in at the back of the SPEC7 at the location of the hole in the PCB. Both a fan from Sunon Fans, part number "UB5U3-700" (see figure 30) or "Delta Electronics", part number "KDB0305HA3-00C1J" will fit. The fan can be connected to X1 and can be controlled via FPGA pin AD25.

Figure 30: Sunon Fan UB5U3-700

The counterpart for X1 and X3 is a Molex connector, part number 0022013027.

9.3 RF-Shielding Can

The SPEC7 is equipped with RF Shield Clips such that a Clip-On EMI Shield can be placed over the clocking circuits to minimize phase noise degradation due to external EMI noise sources. Placing of this EMI shield is optional. All measurements that are reported in this document are performed without a shield.

	Manufacturer	**Part Number**
Heatsink	AAVID	342943
Fan 5V DC	Sunon Fans	UB5U3-700
Fan 5V DC	Delta Electronics	KDB0305HA3-00C1J
Counterpart X1, X3	Molex	0022013027
Clip-On EMI Shielding Can 35x50mm, Height=10mm	Holland Shielding	1500-35-50-10-TS0.20

Table 9: Optional Heatsink, Fans, Connecto, RF-Shielding Can

10 Known bugs & Errors

1. The EN pin of U28 is '1' which enables OUT0/1 but disables OUT2/3. In contrast to what is stated in the schematics, Table 1 of datasheet CDCLVD2102 see [1] shows that both outputs are enabled when EN is "open"

2. Although ESD protected, SiliconLabs CP2105 (U54, dual UART) seems to be a weak spot. When the SPEC7 is operated stand alone then the chassis of a PC that is connected to the mini USB connector (X2) must be at SPEC7 ground potential.

References

[1] Texas Instruments. Dual1:2lowadditivejitterlvdsbuffer. https://www.ti.com/lit/ds/symlink/cdclvd2102.pdf?ts=1590402921717, may-2010.

[2] Inc. Micron Technology. Mt25ql128aba8esf catalog. https://www.micron.com/products/nor-flash/serial-nor-flash/part-catalog/mt25ql128aba8esf-0sit, 2020.

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[11] Xilinx. Ds191: Zynq-7000 soc (z-7030, z-7035, z-7045, and z-7100): Dc and ac switching characteristics. https://www.xilinx.com/support/documentation/data_sheets/ds191-XC7Z030-XC7Z045-data-sheet.pdf, 02-Juy-2018.

[12] Xilinx. Answer record 55572. https://www.xilinx.com/support/answers/55572.html, 18-may-2018.

[13] Xilinx. Answer record 16996. https://www.xilinx.com/support/answers/16996.html, 27-april-2016.

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Appendices

A 125 MHz reference generator

Figure 31 shows a block diagram of the 125 MHz reference generator that is custom made and build around a 10 MHz master source (Morion MV336M-A005D-10.0MHz-ULN-1.5E-13). This is an OCXO with exceptional low phase noise, very good short term stability (Allan deviation) of up to $1,5 \times 10^{-13}\delta(t)$ per 1 sec.

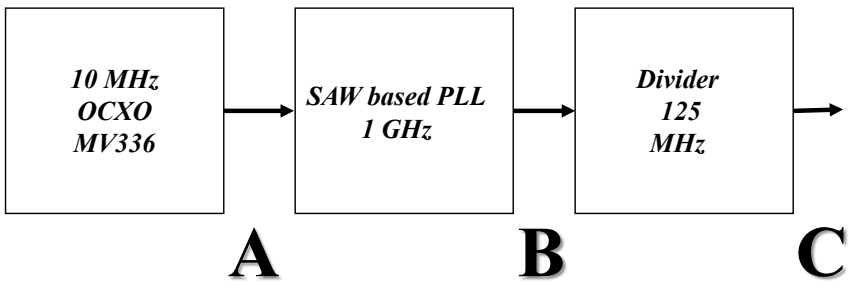


Figure 31: Phase noise measurement setup 125 Mhz reference generator.

The phase noise of the OCXO is plotted in the following figure 32. This is measured on position **A**. For completeness the phase noise at position **B** (1 GHz) is show in figure 33 The final output frequency 125MHz on position **C** is shown in figure 34

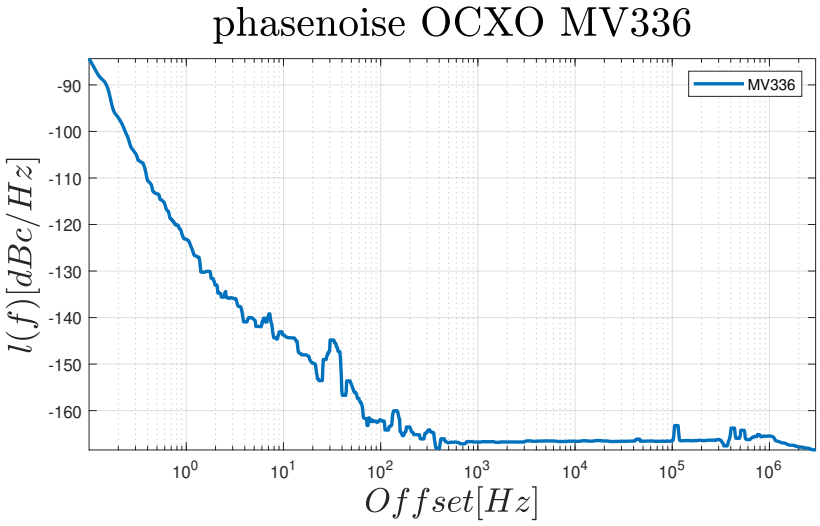


Figure 32: Phase noise @**A**: 10 MHz OCXO MV336M

Phase noise power levels (in dB) will increase when multiplying and decrease when dividing frequency, according to equation (1) where N is the multiplication factor.

$$20 * log_{10}(N) \tag{1}$$

Phase noise power level at 1 GHz is expected to be 40 dB higher than at 10 MHz ($N =$ 1GHz/10MHz $= 100$). In addition the PLL phase noise is added.

It can be seen that the oscillator phase noise at 10 Hz (where the plateau starts) is approximately -142 dBc/Hz (figure 32) so the phase noise to be expected at 1 GHz is at least -102 dBc/Hz. The actual measured phase noise at 1 GHz (figure 33) at 10 Hz is approximately -92 dBc/Hz. This leads to the conclusion that additive phase noise of the PLL (HMC 704) is 10 dB. For a next design it should be considered to use a PLL that performs better.

The bandwidth of the PLL is set to $\approx$ 500 Hz hence the bump in the phase noise plot.

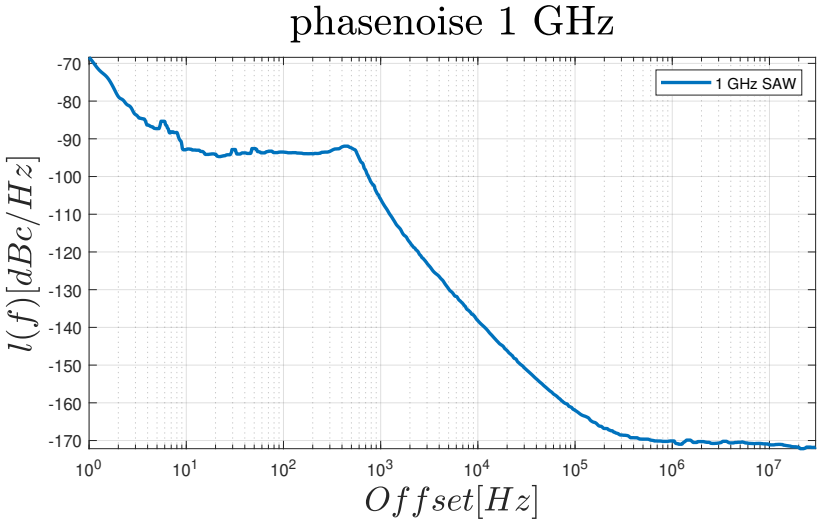


Figure 33: Phase noise @**B**: 1 GHz OCXO MV336M

Phase noise power level at 125 MHz is expected to be 18 dB lower than at 1 GHz ($N = \frac{1}{8}$). The actual measured phase noise at 125 MHz (figure 34) at 10 Hz is approximately -110 dBc/Hz.

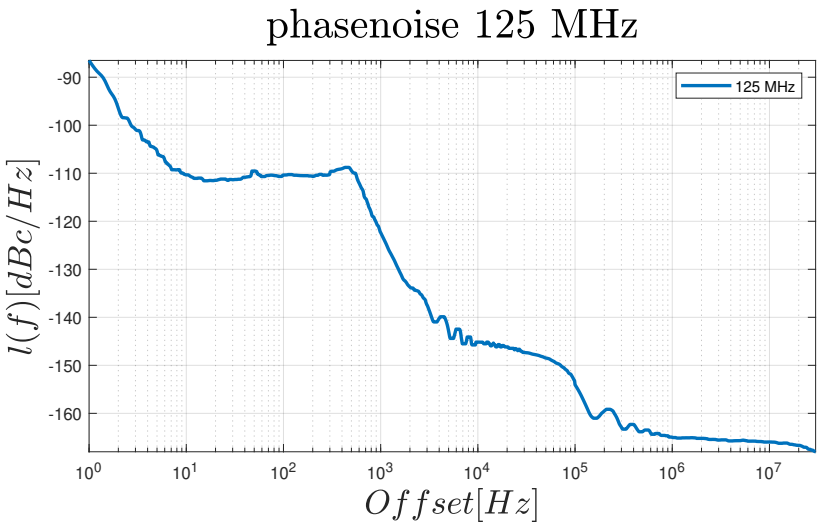


Figure 34: Phase noise @**C**: 125 MHz OCXO MV336M

B SPEC7 10 MHz phase noise output HPSEC versus WR-LJ

Figure 35 shows the 10 MHz phase noise when using the SPEC7 as a slave device, either:

- connected to a White Rabbit Low Jitter switch (WRS-LJ), or
- connected to a SPEC7 in master mode that is clocked by a 125 MHz reference generator (see Appendix A)

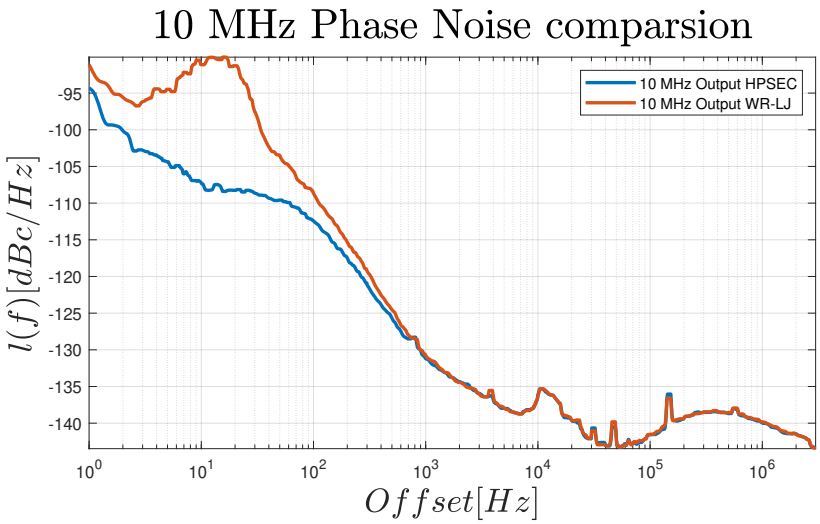


Figure 35: Compare SPEC7 slave 10MHz phase noise when using a HPSEC versus a WRS-LJ as master

C How to boot from QSPI

The SPEC7 is capable of booting from on board dual QSPI flash. In order to do so, a HDL design containing a ZYNQ Processing System (PS) IP core must be used [citation needed]. This section describes the process of flashing your design into the QSPI flash memory. This "How-to" uses Vivado 2019.2 and Vitis 2019.2.

1. Make sure that your design has the Zynq Processing System IP core. The IP core does not need to "do" anything. The PS is needed to transfer the FPGA configuration from QSPI via the PS to the Programmable Logic (PL). After the transfer it may idle.

2. Generate your bitfile as you would do normally.

3. In Vivado, go to: File → Export → Export Hardware. Check "Include bitfile" and click "OK". Remember the path provided here.

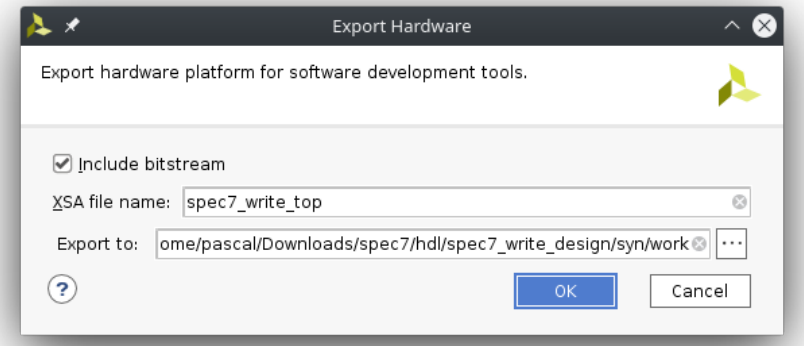


Figure 36: Export Hardware window in Vivado.

4. In Vitis, go to: File → New → Platform project. Make up a name for your platform (for example "SPEC7_Z035") and hit "Next".

5. Check "Create from hardware specification (XSA)" and hit "Next".

6. Click "Browse" and provide the XSA file on the path specified in step 3. And click on "Finish".

7. Include the Xilffs package by clicking on the "platform.spr" file and modify the BSP in the standalone domain to include xilffs. As can be seen in figure 37.

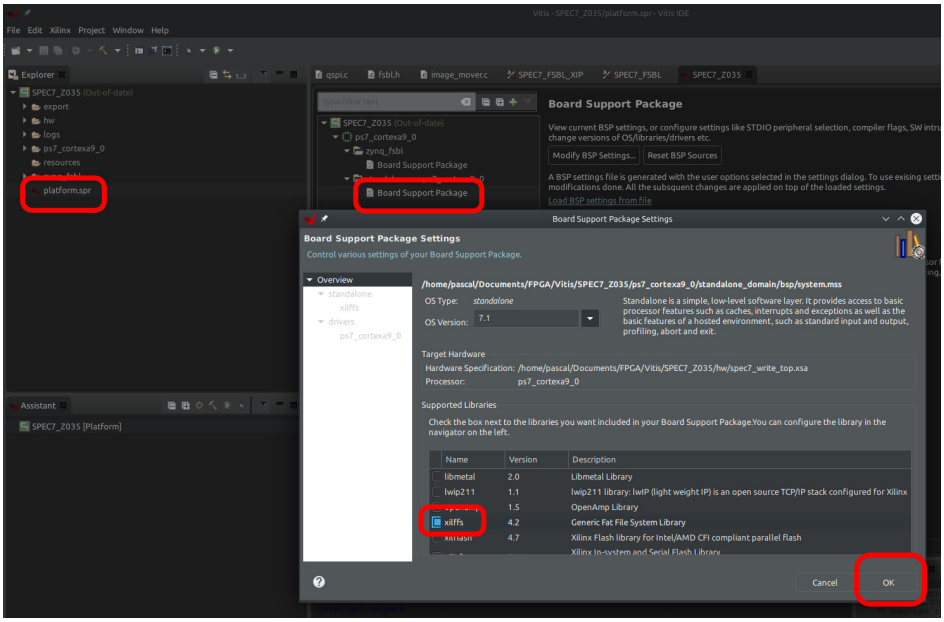


Figure 37: Include xilffs in the platform file in Vitis

8. Build the project by clicking on the build icon in the menu bar, or press Ctrl+B.

9. Now to build a First Stage BootLoader (FSBL), go to: File → New → Application project. Make up a name for your bootloader (for example "SPEC7_FSBL") and click "Next" three times.

10. Select "Zynq FSBL" as template and click "Finish".

11. (Optional) To significantly decrease boot time, change line 251 in the file *qspi.c* in the bootloader project from "XQSPIPS_CLK_PRESCALE_8" to "XQSPIPS_CLK_PRESCALE_2".

12. Build the bootloader by clicking on the build icon in the menu bar, or press Ctrl+B.

13. Go to: Xilinx → create boot image. Specify a location for the *.bif* file by clicking on "Browse". Select MCS as output format.

14. Click on "Add" in Boot Image Partitions to specify the first stage bootloader (*.elf*) file, generated in step 12". Set the partition type to "Bootloader" and click on "OK".

15. Click on "Add" another time and specify your bitfile and click on "OK". Your "Create Boot Image" window should look something like figure 38

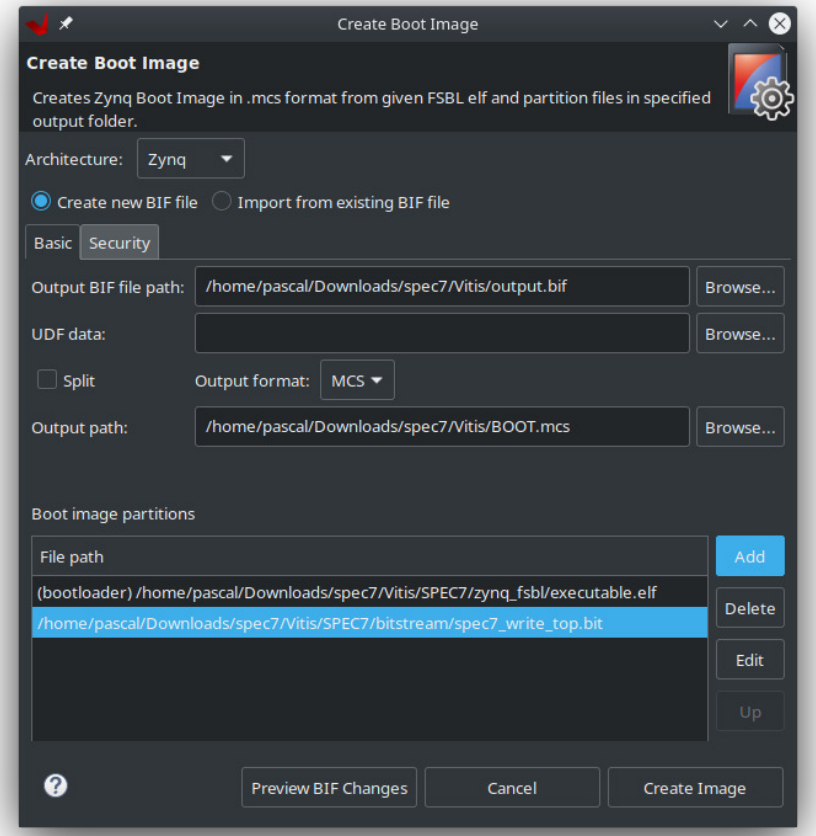


Figure 38: Create Boot Image in Vitis

16. Click on "Create Image" and wait for the MCS file to be generated.

17. Make sure the SPEC7 is in JTAG mode by checking the DIP switches of S3. switch 2,3 and 4 should be "zero" by facing the right side of the pcb (towards the printed numbers on the switch).See figure **??** how they look.

18. Go to: Xilinx → Program Flash. Double check if the *.MCS* and *.elf* files are the same as the ones generated in step 16 and 12. Then check if the flash type is set to "qspi-x8-dual-parallel". As can be seen in figure 39.

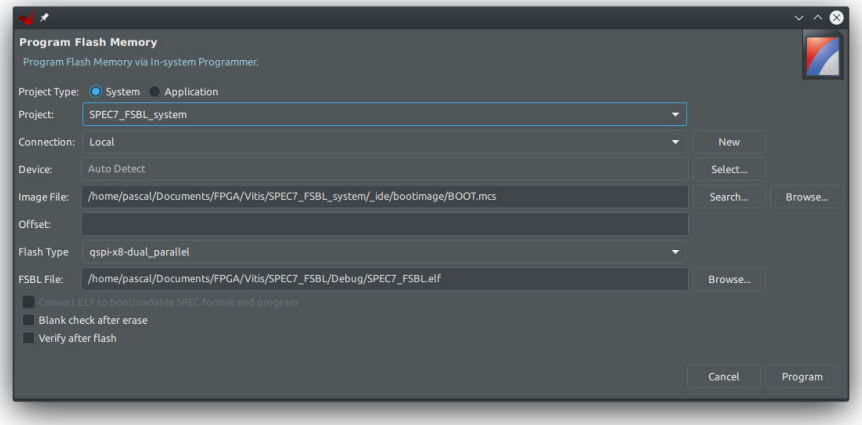


Figure 39: Program Flash in Vitis

19. Click on "Program" and wait (a while) for the programmer to write the flash memory.

20. After the flash operation has finished, power down the board. Change the number two Switch on S3 to the "one" position, facing the left side of the board.

21. Finally power on the SPEC7, booting should be finished within one second.

22. See how to program or flash the following section **??**

D Physical layer PCIe test set up

It should be noted that not all PCIe compliance tests are performed, only basic transmitter eye diagram measurements where performed for data rates 2,5GT/S and 5GT/S. The card is inserted in the PCI Express GEN-3 Compliance Base Board (CBB [9]) see figure 40, the CBB is test fixture where all the high speed differential lines are routed to SMP coax connectors to hook up test equipment.

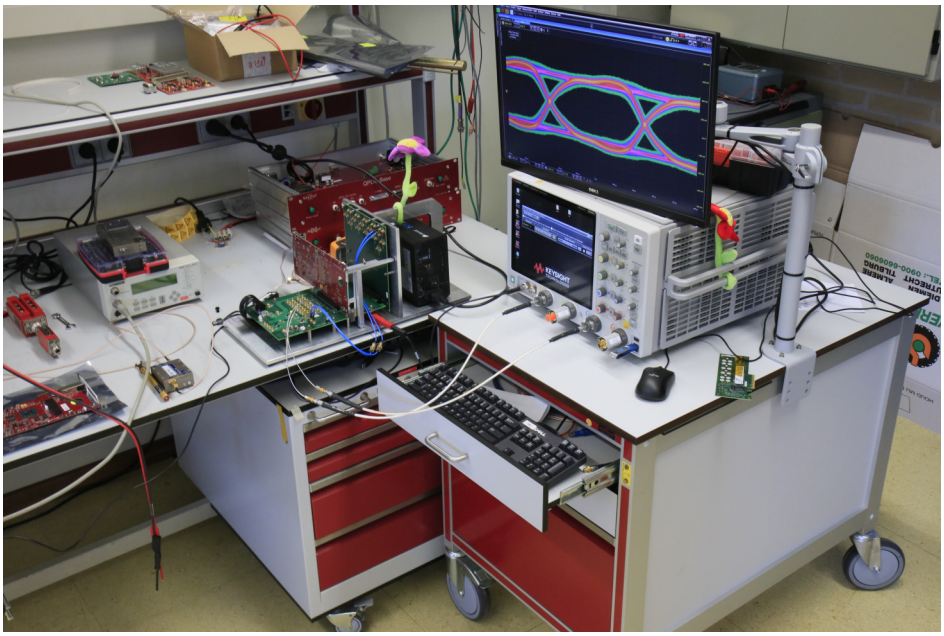
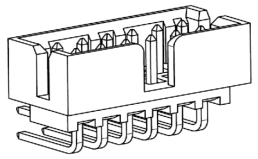


Figure 40: PCIe CBB setup

For reference purposes the schematic of the spec 7 is shown.

E Schematics

SPEC7_JTAG_Chain
Sheet 26



FMC_JTAG
PRSNT_M2C_L
ZYNQ_JTAG
PL_JTAG

PS_USB_OTG
Sheet 22

USB Type A (2.0)

USB_OTG

PL_USER_IO
Sheet 25

SD_CARD
BOARD_VERSION
PL_User_IO

PL_PS_UART
Sheet 23

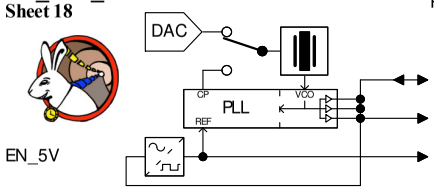
Mini USB Type B

PL_PS_Dual_UART

PL_I2C EEPROM_Unique_ID
Sheet 28

EEPROM_UID

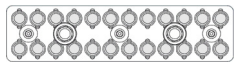
PL_WR_Oscillators
Sheet 18



EN_5V

PL_WR_DACS
PLL_CTRL
BULLS_EYE
WR_CLOCKS
10MHZ_CLK

PL_BullsEye
Sheet 21

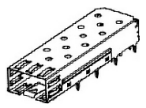


WR_CLOCKS
BULLS_EYE
TIMING_SIGNALS

PL_SI570
Sheet 29

PL_SI57X

PL_SFP_Connector
Sheet 24



PL_SFP

USB_OTG
SD_CARD
BOARD_VERSION
PL_User_IO
PL_PS_Dual_UART
EEPROM_UID
PL_WR_DACS
PLL_CTRL
BULLS_EYE
WR_CLOCKS
10MHZ_CLK
TIMING_SIGNALS
PL_SI57X
PL_SFP

ZYNQ
XC7
(Z030)
Z035
(Z045)
FBG676

Sheet 2

PL_JTAG
ZYNQ_JTAG
Force_PS_POR
RESET_CONFIG
FPGA_CONFIG
PL_DDR
PS_DDR
PL_FMC
PS_RGMII
PL_PCIe_2x
PG_VCCINT

SPEC7_Power_System
Sheet 30

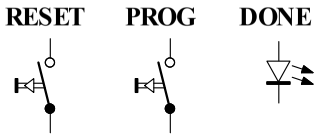
EN_5V
PGOOD

SPEC7_Mechanical_Parts
Sheet 35

FMC_JTAG
ZYNQ_JTAG
PL_JTAG
Force_PS_POR
RESET_CONFIG
FPGA_CONFIG
PL_DDR
PS_DDR
PL_FMC
PRSNT_M2C_L
PG_C2M
R325
0
PS_RGMII
PL_PCIe_2x

SPEC7_Resets
Sheet 27

Force_PS_POR
RESET_CONFIG
FPGA_CONFIG
PL_PCIe_2x
PGOOD



PL_DDR3
Programmable Logic
Sheet 13

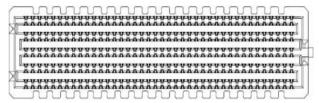
PL_DDR

PS_DDR3
Processor System
Sheet 12

PS_DDR

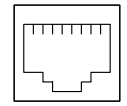
PL_FMC_Connector
Sheet 17

FMC_JTAG
PL_FMC



PS_Phy_CopperEthernet
Sheet 15

PS_RGMII



PL_PCIe_12x_Edge_Con
Sheet 14

PCIe_2x

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Sheetname : Top

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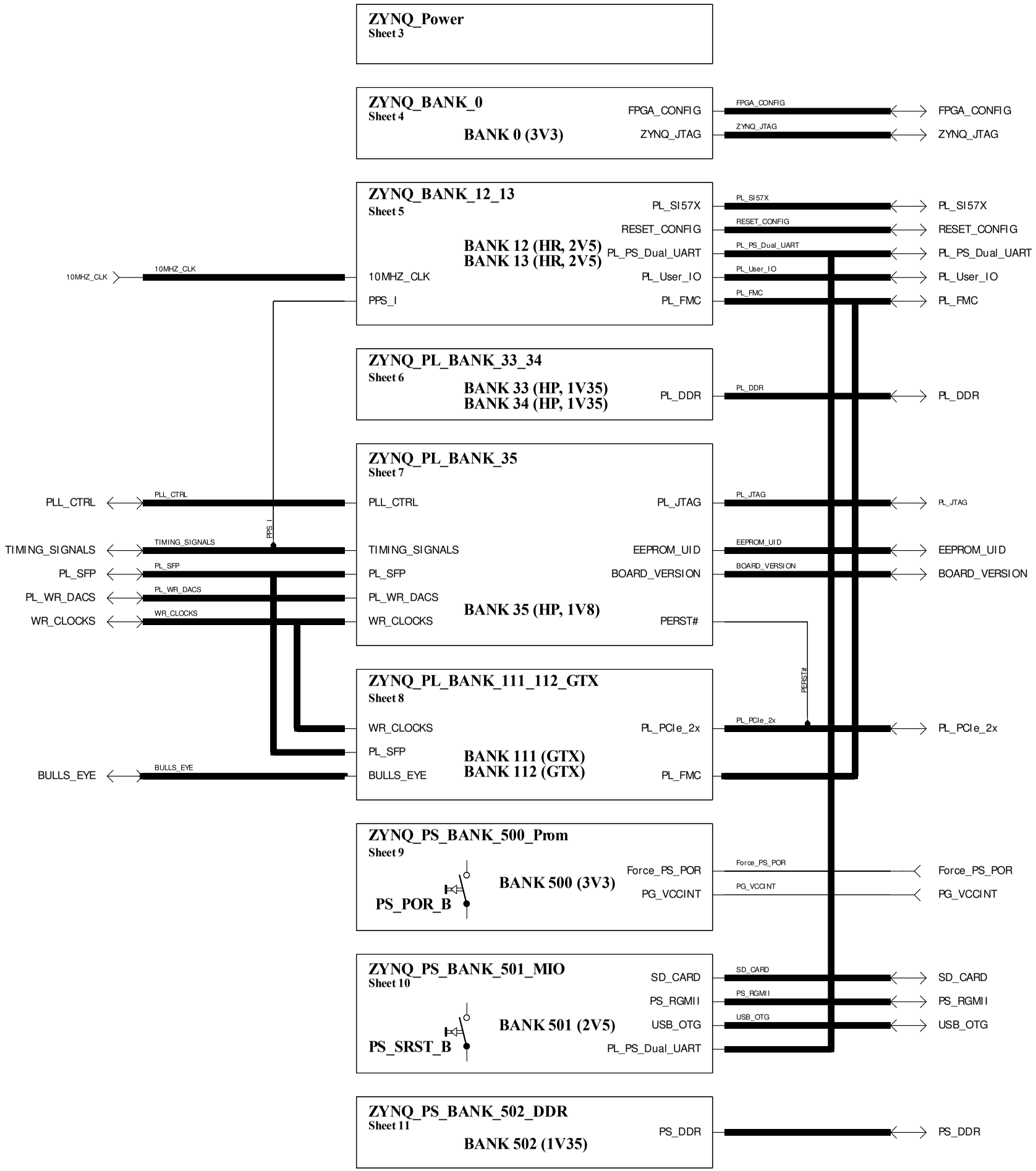
Size: 420 x 297mm
Sheet: 1 of 35 A3
Date: 2020-01-31



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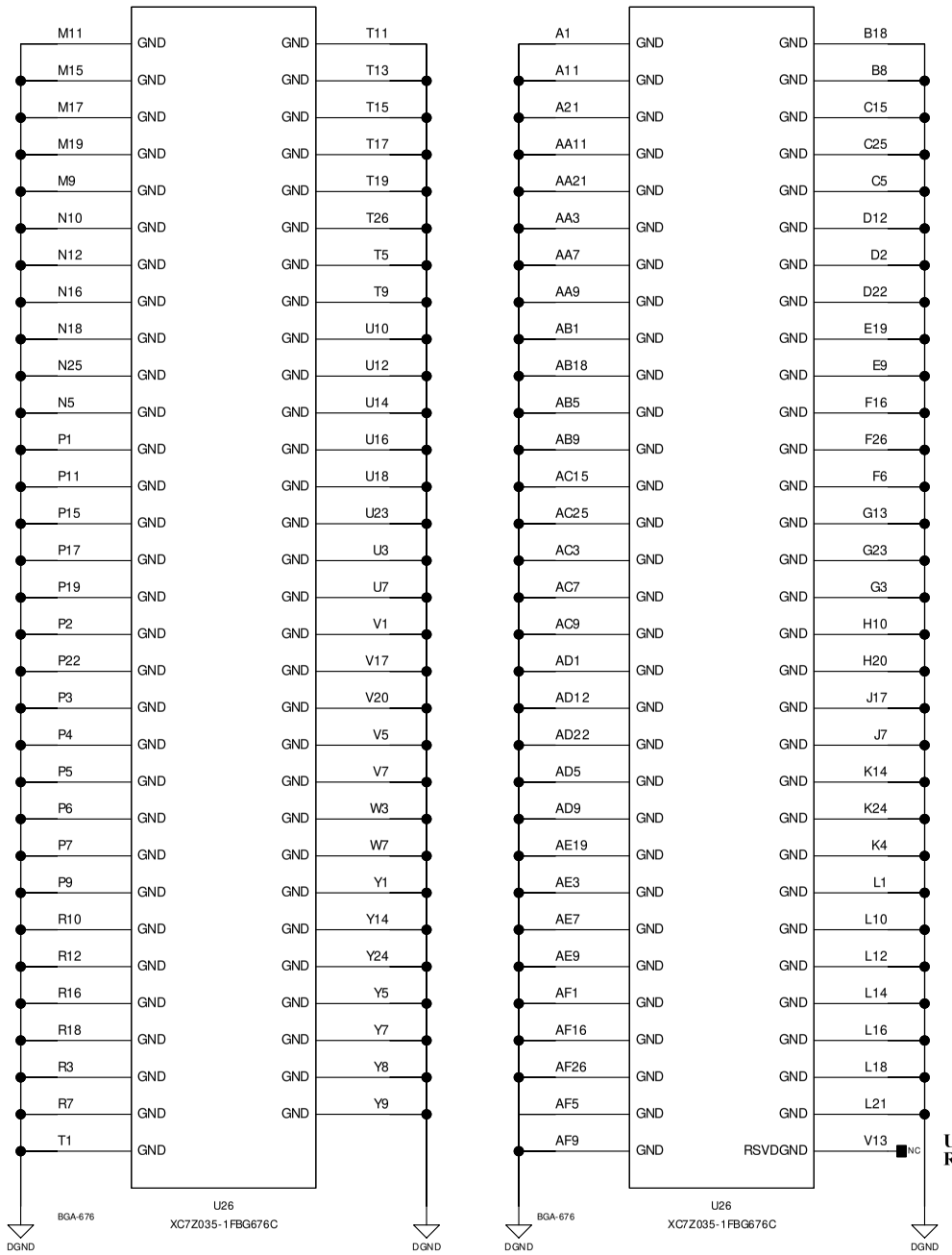
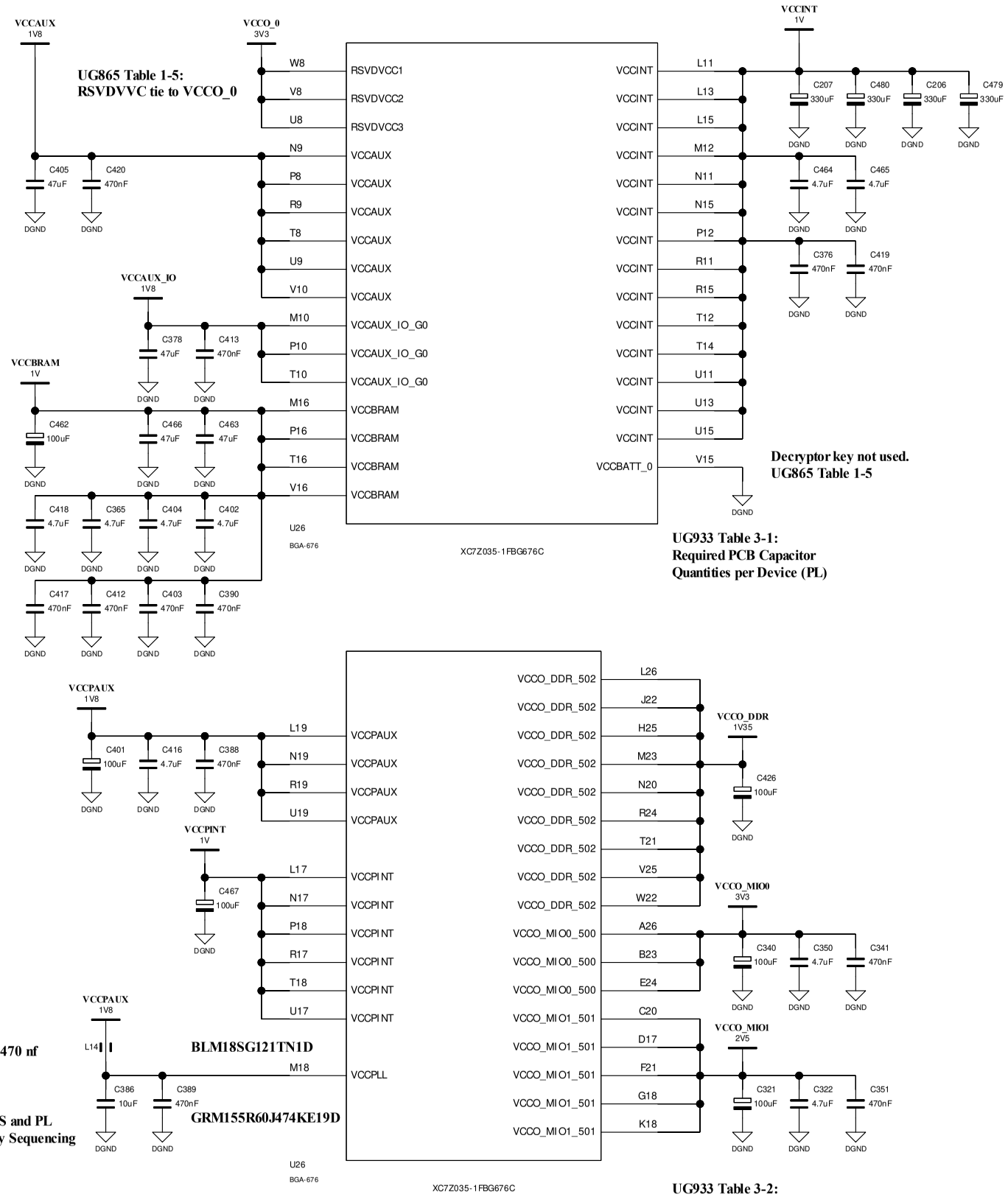


UG865 Table 1-5:
RSVDGND do not connect

Layout recommendation
see UG933 figure 5-2 & 5-3
Note recommended part for 470 nf and ferrite bead!

VCCPLL See also DS191 PS and PL Power-On/Off Power Supply Sequencing



UG933 Table 3-2:
Required PCB Capacitor
Quantities per Device (PS)

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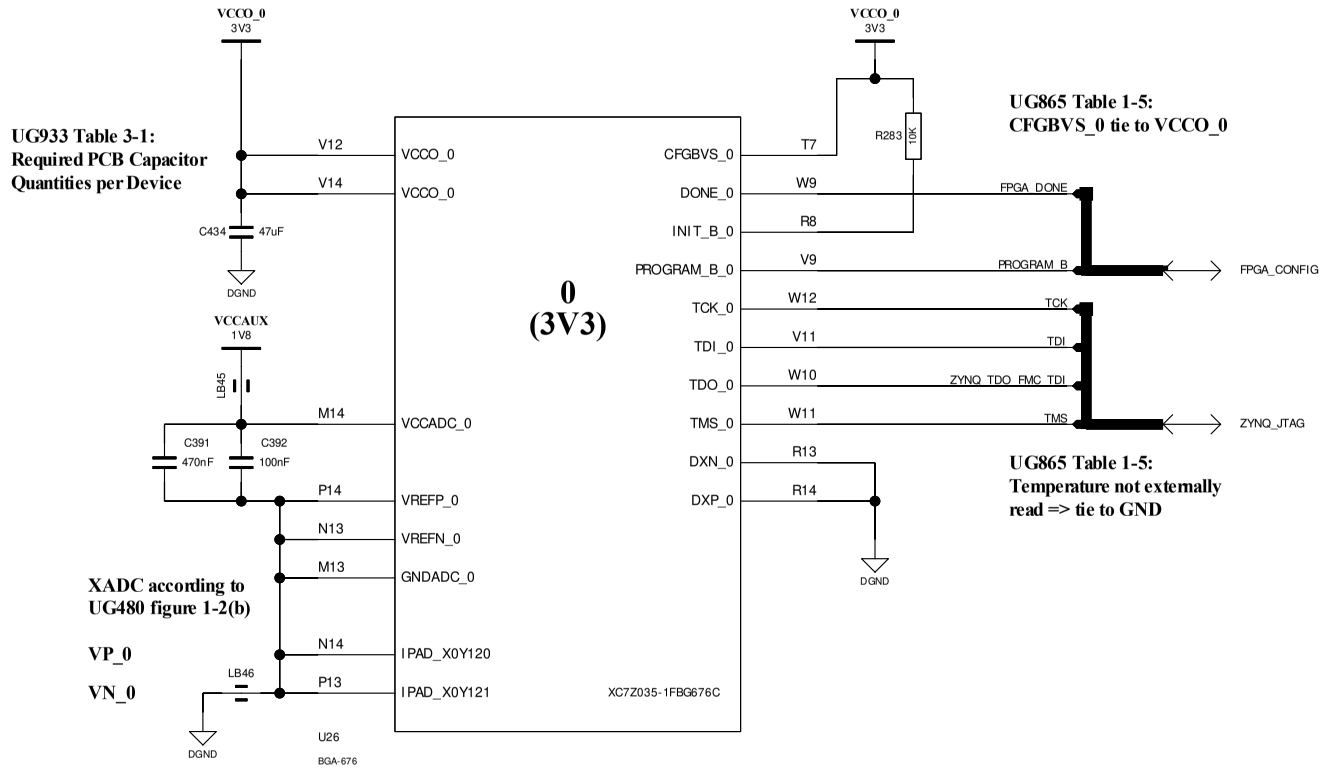

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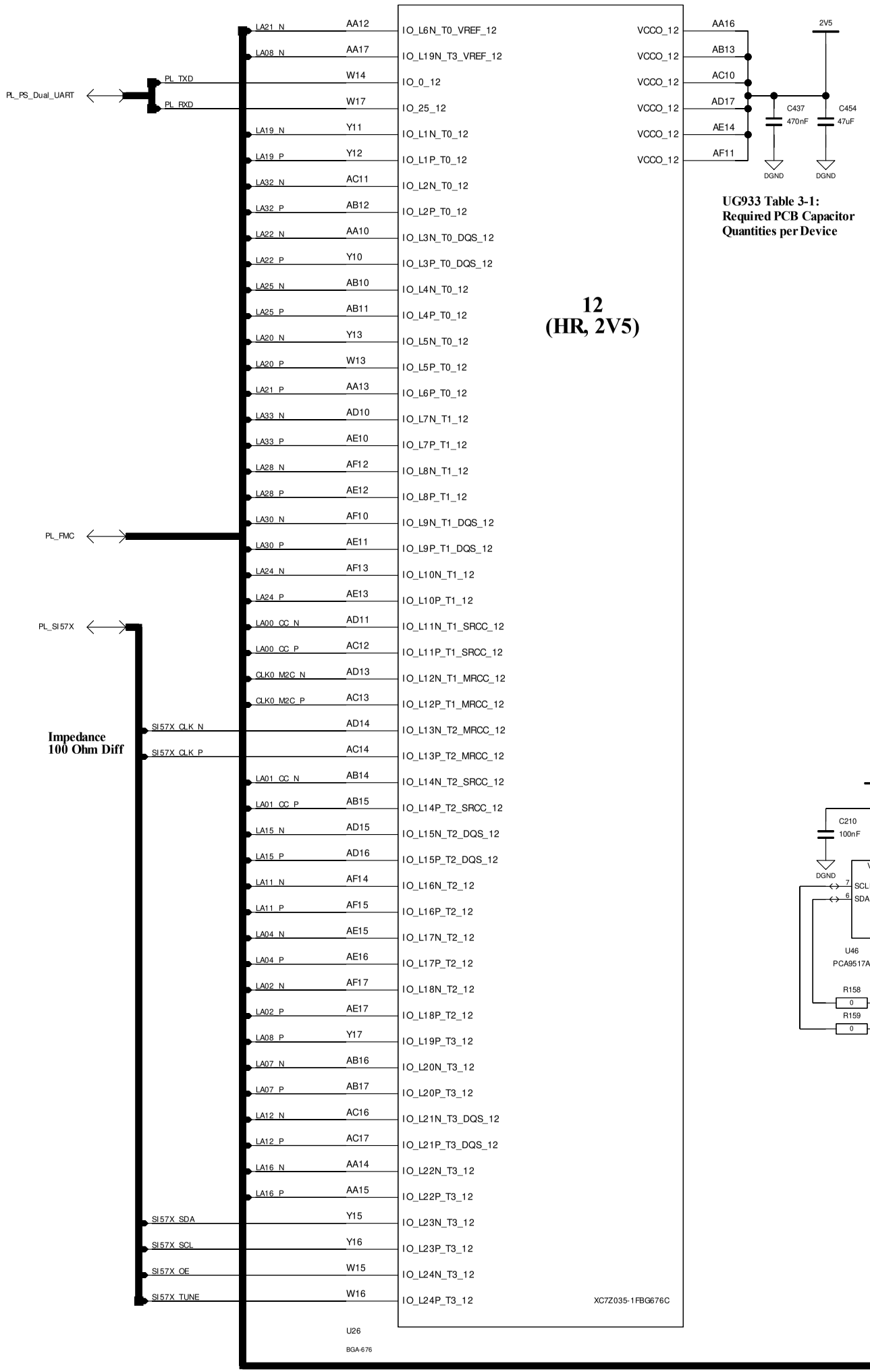

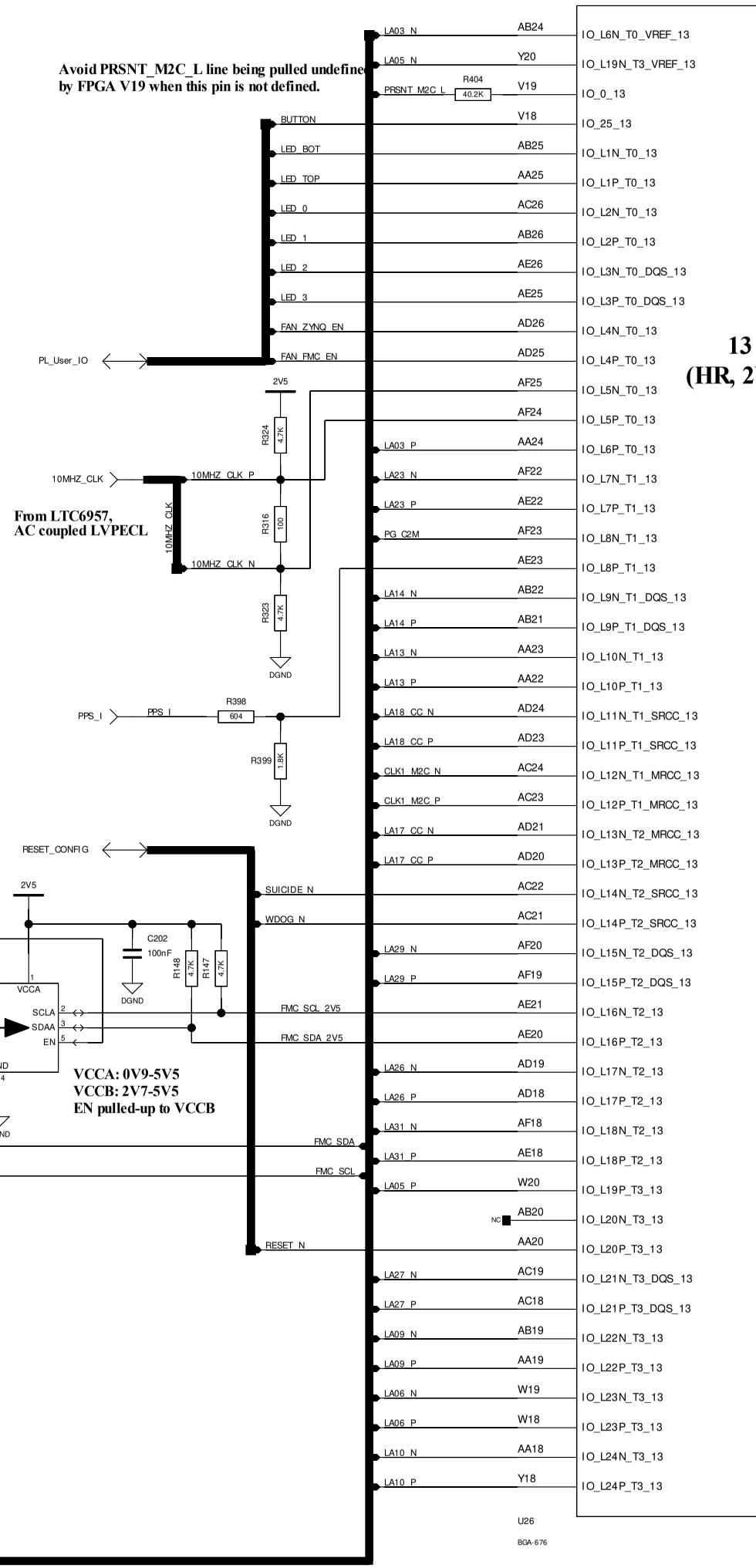

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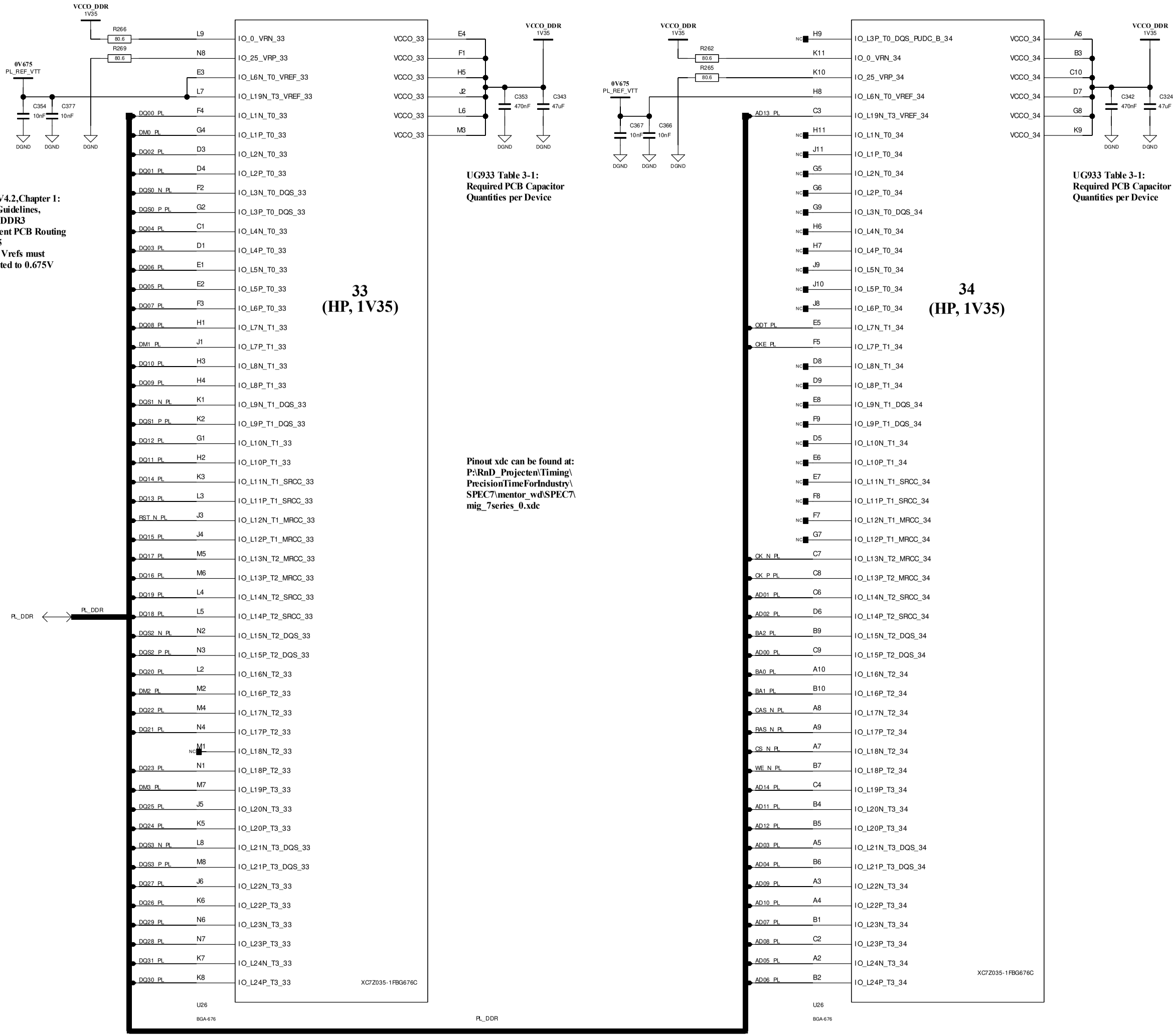

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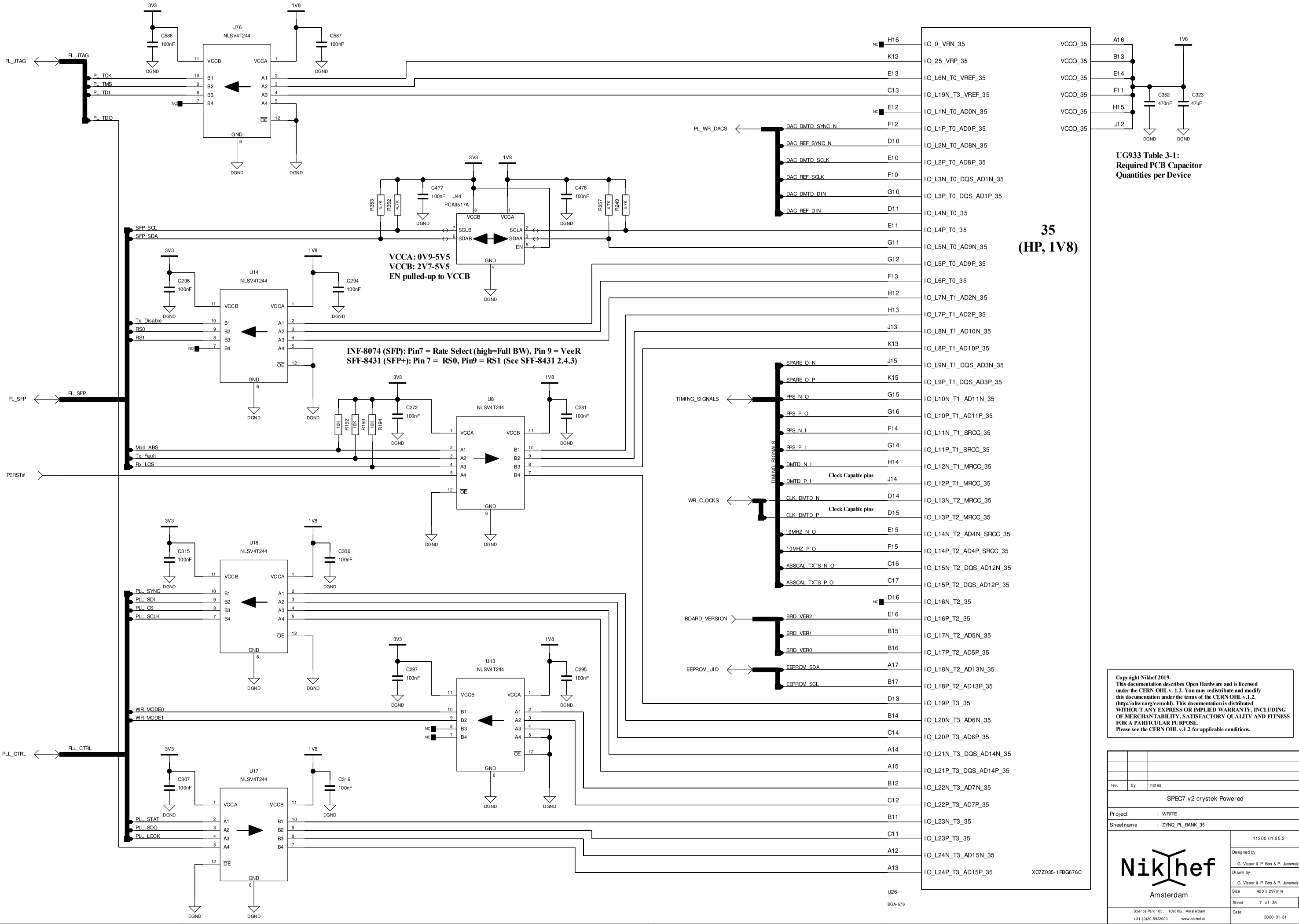

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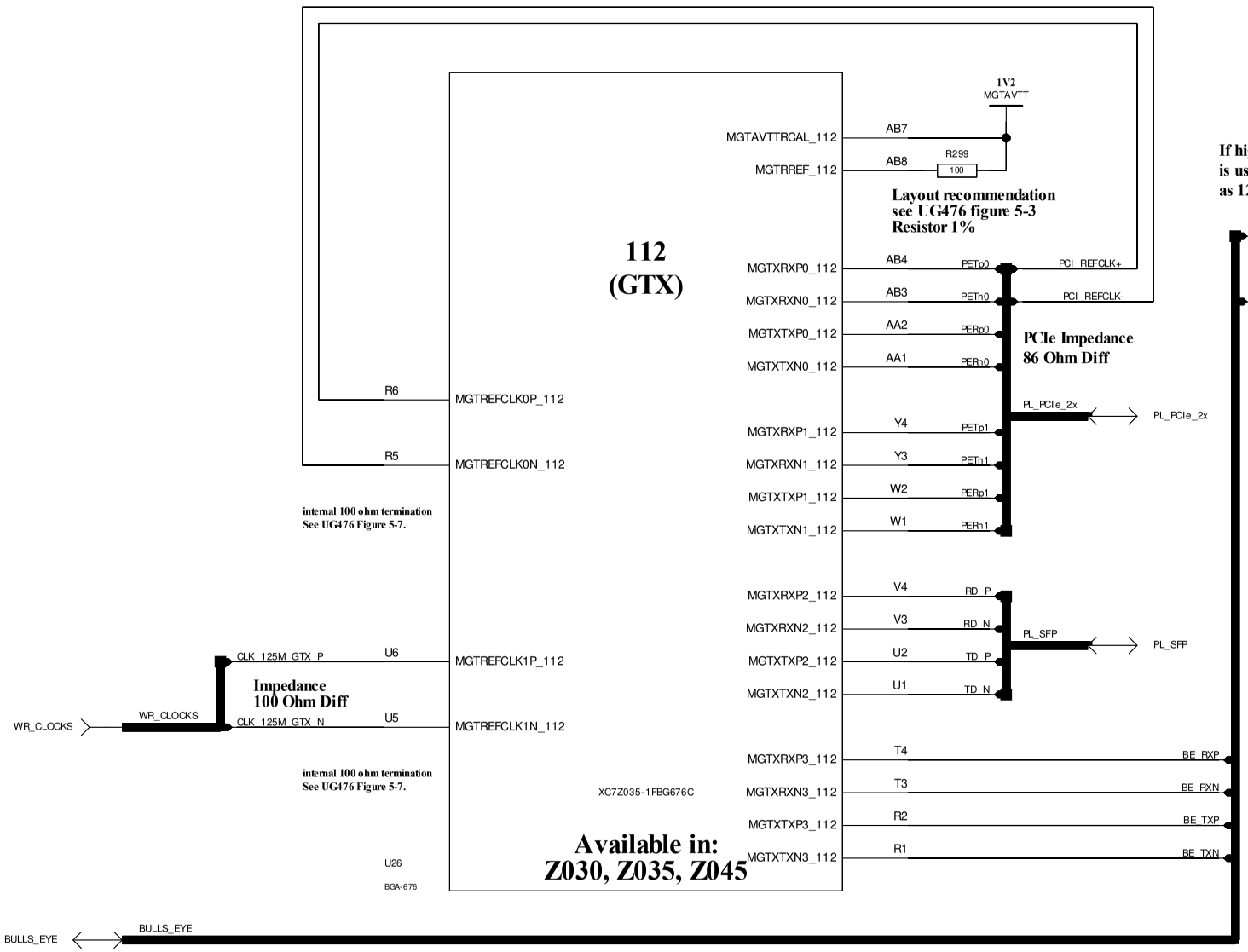

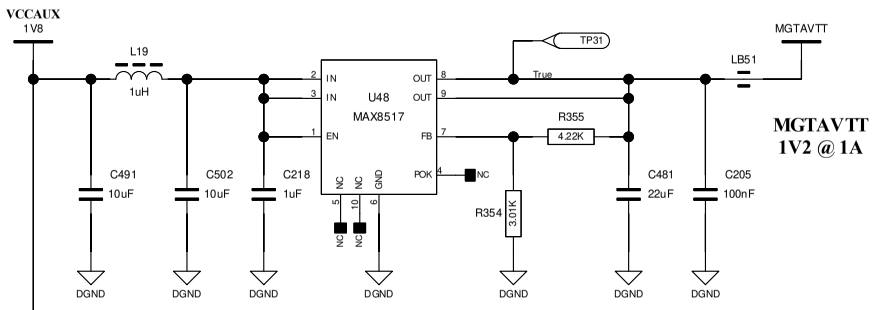

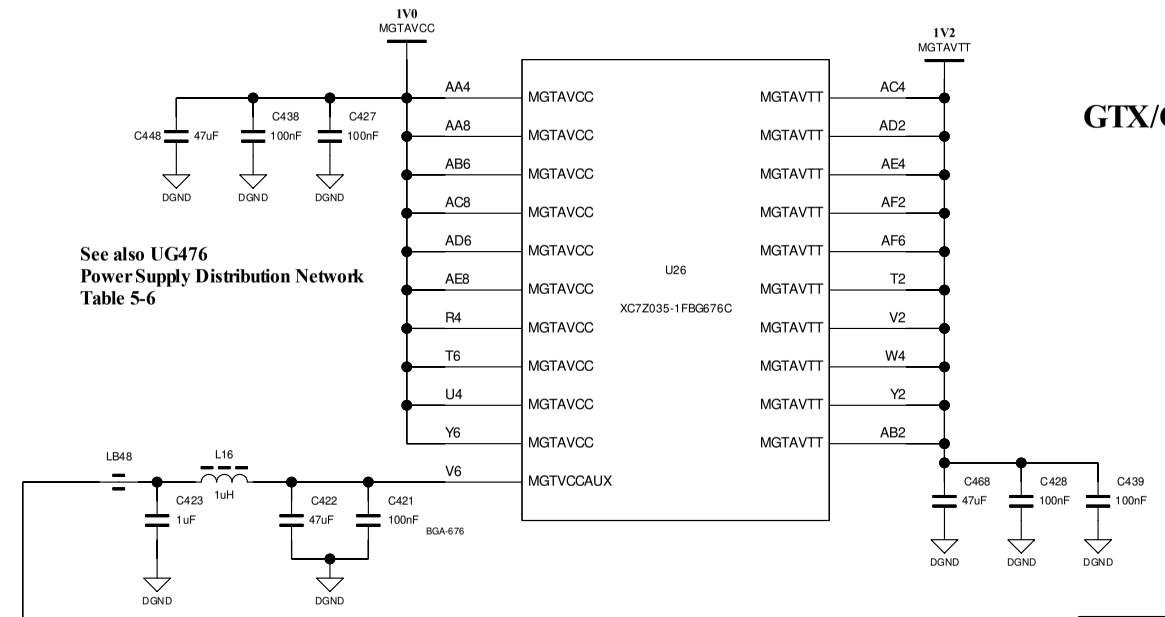

General GTX remark:
See also UG476 Table 5-7
GTX/GTH Transceiver PCB Design Checklist

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Project : WRITE

Sheetname : ZYNQ_PL_BANK_111_112_GTX

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Sheet 8 of 35 A3

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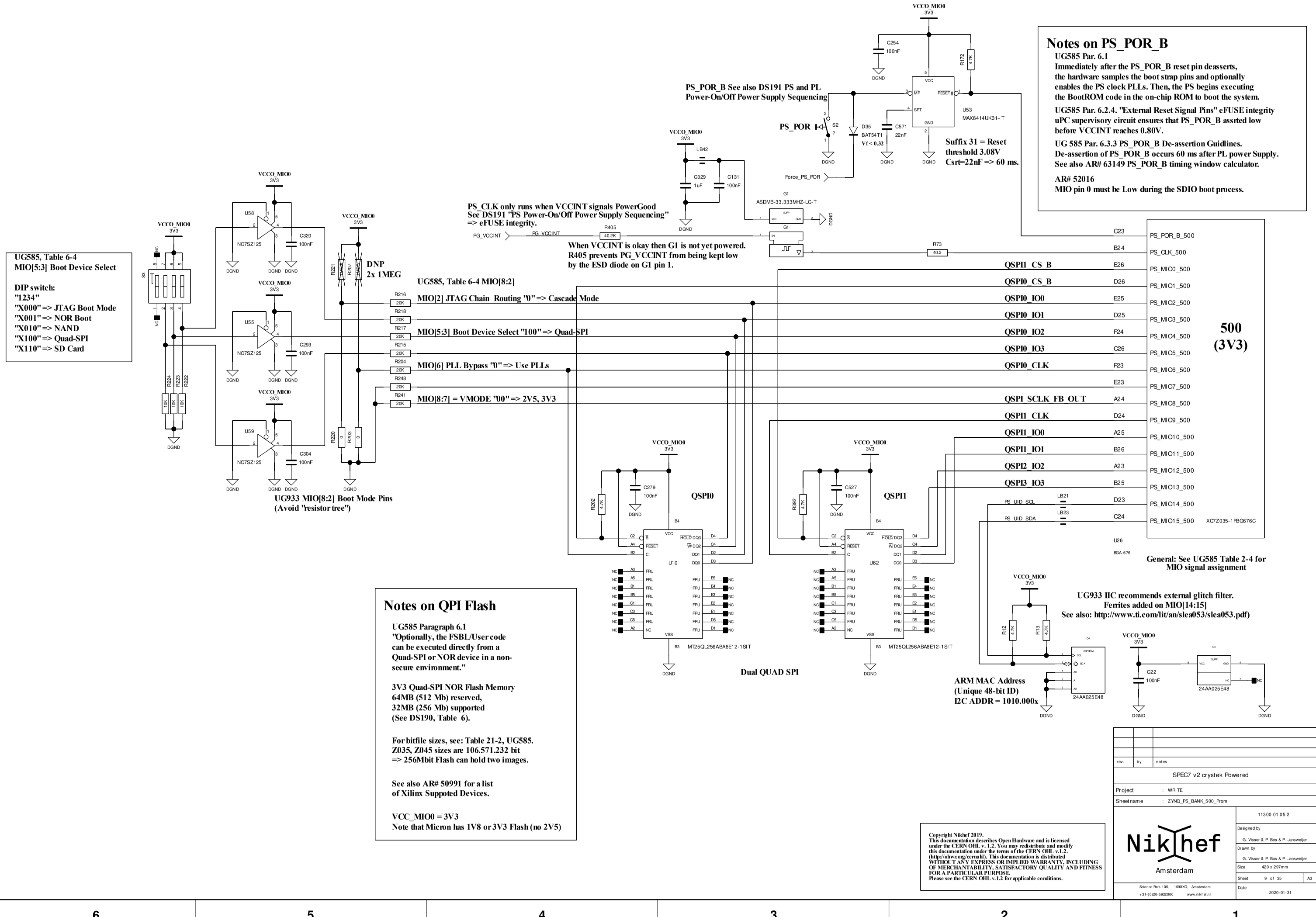
Notes on PS_POR_B
UG585 Par. 6.1
Immediately after the PS_POR_B reset pin deasserts, the hardware samples the boot strap pins and optionally enables the PS clock PLLs. Then, the PS begins executing the BootROM code in the on-chip ROM to boot the system.
UG585 Par. 6.2.4. "External Reset Signal Pins" eFUSE integrity
uPC supervisory circuit ensures that PS_POR_B assrted low before VCCINT reaches 0.80V.
UG 585 Par. 6.3.3 PS_POR_B De-assertion Guidlines.
De-assertion of PS_POR_B occurs 60 ms after PL power Supply.
See also AR# 63149 PS_POR_B timing window calculator.
AR# 52016
MIO pin 0 must be Low during the SDIO boot process.
PS_POR_B See also DS191 PS and PL Power-On/Off Power Supply Sequencing
PS_POR
Suffix 31 = Reset threshold 3.08V
Csrt=22nF => 60 ms.
PS_CLK only runs when VCCINT signals PowerGood
See DS191 "PS Power-On/Off Power Supply Sequencing"
=> eFUSE integrity.
When VCCINT is okay then G1 is not yet powered.
R405 prevents PG_VCCINT from being kept low by the ESD diode on G1 pin 1.
UG585, Table 6-4
MIO[5:3] Boot Device Select
DIP switch:
"1234"
"X000" => JTAG Boot Mode
"X001" => NOR Boot
"X010" => NAND
"X100" => Quad-SPI
"X110" => SD Card
DNP
2x 1MEG
UG585, Table 6-4 MIO[8:2]
MIO[2] JTAG Chain Routing "0" => Cascade Mode
MIO[5:3] Boot Device Select "100" => Quad-SPI
MIO[6] PLL Bypass "0" => Use PLLs
MIO[8:7] = VMODE "00" => 2V5, 3V3
UG933 MIO[8:2] Boot Mode Pins
(Avoid "resistor tree")
QSPI0
QSPI1
Dual QUAD SPI
MT25QL256ABA8E12-1SIT
Notes on QPI Flash
UG585 Paragraph 6.1
"Optionally, the FSBL/User code can be executed directly from a Quad-SPI or NOR device in a non-secure environment."
3V3 Quad-SPI NOR Flash Memory
64MB (512 Mb) reserved,
32MB (256 Mb) supported
(See DS190, Table 6).
For bitfile sizes, see: Table 21-2, UG585.
Z035, Z045 sizes are 106.571.232 bit
=> 256Mbit Flash can hold two images.
See also AR# 50991 for a list of Xilinx Suppoted Devices.
VCC_MIO0 = 3V3
Note that Micron has 1V8 or 3V3 Flash (no 2V5)
500 (3V3)
XC7Z035-1FBG676C
BGA-676
General: See UG585 Table 2-4 for MIO signal assignment
UG933 IIC recommends external glitch filter.
Ferrites added on MIO[14:15]
See also: http://www.ti.com/lit/an/slea053/slea053.pdf)
ARM MAC Address
(Unique 48-bit ID)
I2C ADDR = 1010.000x
24AA025E48
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rev. by notes
SPEC7 v2 crystek Powered
Project : WRITE
Sheetname : ZYNQ_PS_BANK_500_Prom
11300.01.05.2
Nikhef Amsterdam
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Drawn by G. Visser & P. Bos & P. Jansweijer
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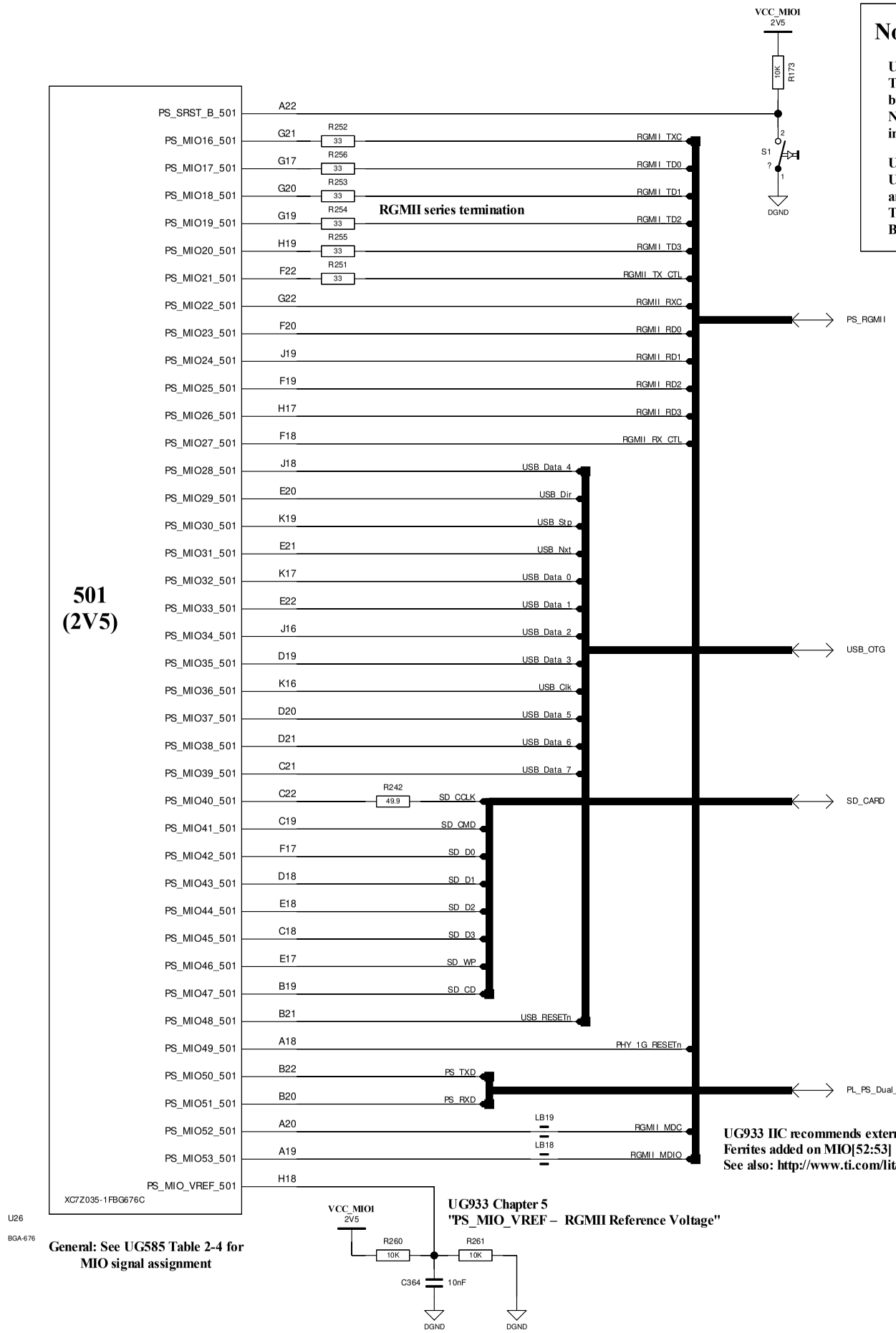

Notes on PS_SRTS_B

UG585 Par. 6.1
The non-POR type resets also cause the BootROM to execute, but without the hardware sampling the strap pins. Non-POR resets include the PS_SRST_B pin and several internal reset sources.

UG585 Par. 6.2.4. "External Reset Signal Pins"
Used to force a system reset. It can be tied or pulled High, and can be High during the PS power supply ramp-up. The PS_SRST_B signal must not be asserted while the BootROM is executing from a POR reset

Notes on SD Card

PCB Design Guide
UG933, Par. SDIO

UG585, SD Card Boot
Table 6-15 MIO[40:45]

UG585 Chapter 6.3.7:
"In SD card boot mode, the BootROM does not perform a header search and does not support multiboot."

UG585 Par. 13.3.7 (figure 13-8)
card detect (CD) and write protect (WP)

UG933 IIC recommends external glitch filter.
Ferrites added on MIO[52:53]
See also: http://www.ti.com/lit/an/slea053/slea053.pdf)

General: See UG585 Table 2-4 for MIO signal assignment

UG933 Chapter 5
"PS_MIO_VREF – RGMII Reference Voltage"

rev.	by	notes

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Project	: WRITE
Sheetname	: ZYNQ_PS_BANK_501_MIO

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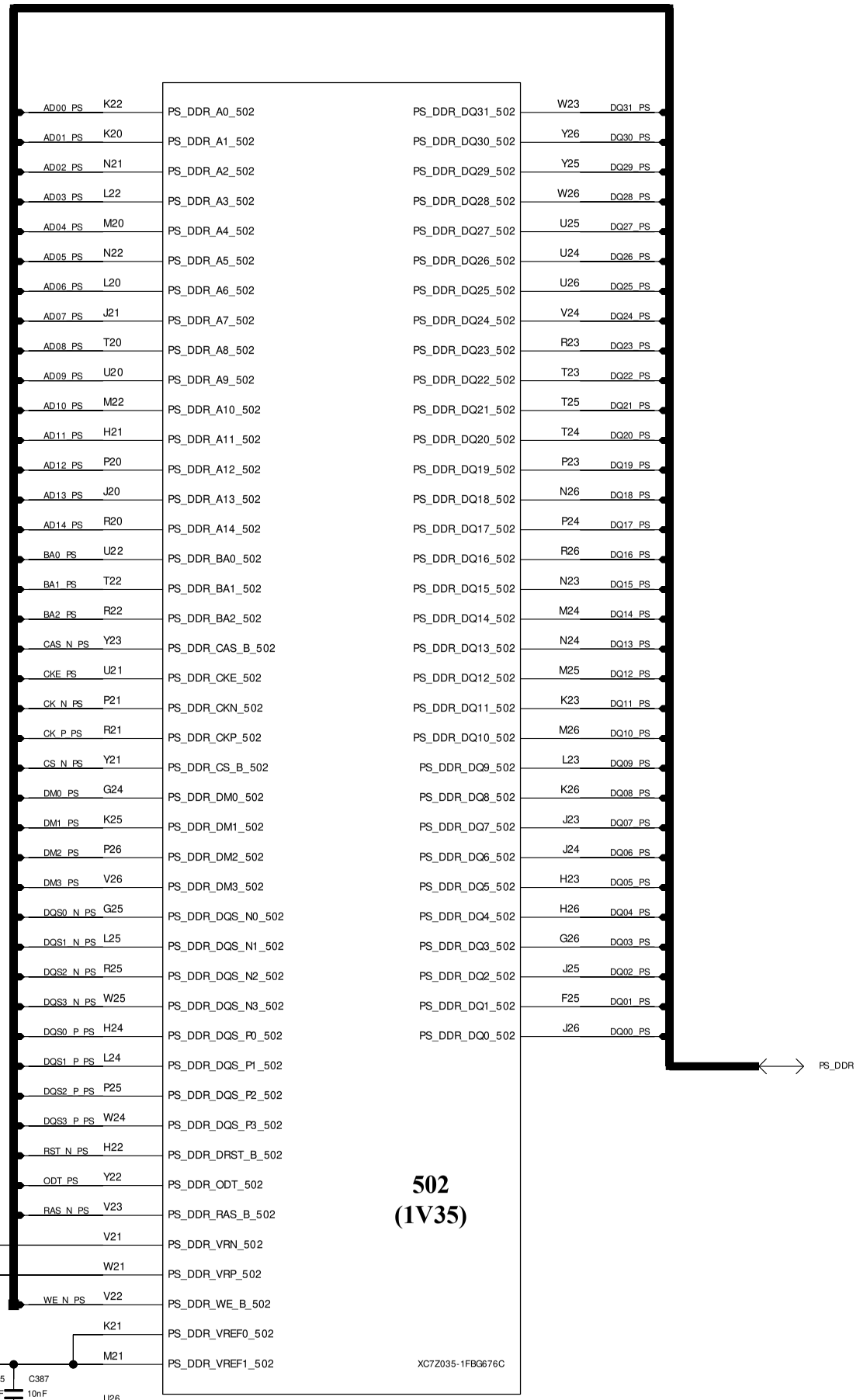
Drawn by	G. Visser & P. Bos & P. Jansweijer
Size	420 x 297mm
Sheet	10 of 35 A3
Date	2020-01-31



rev.	by	notes

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Project : WRITE

Sheetname : ZYNQ_PS_BANK_502_DDR

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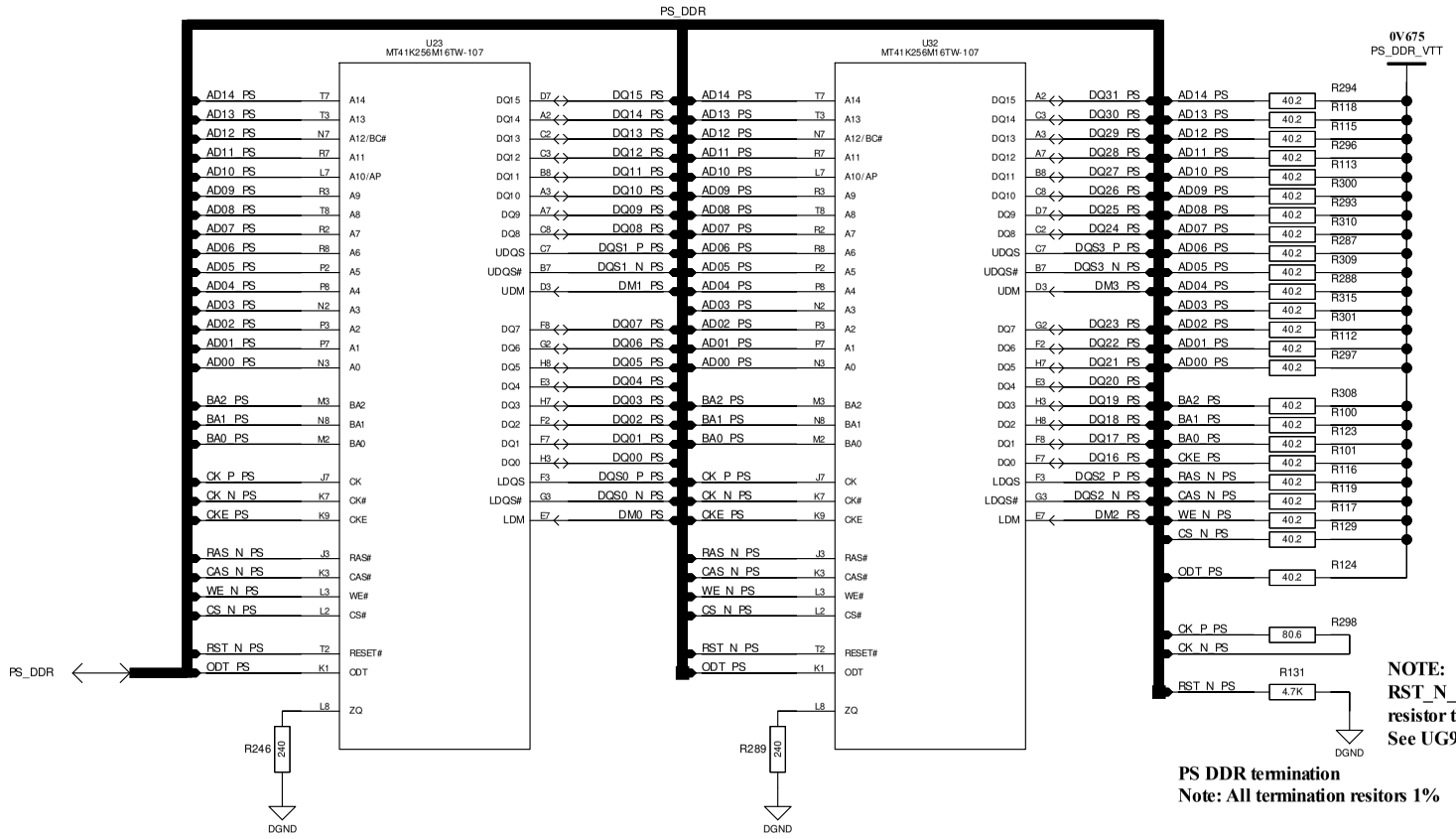
Drawn by
G. Visser & P. Bos & P. Janseweijer

Size 420 x 297mm

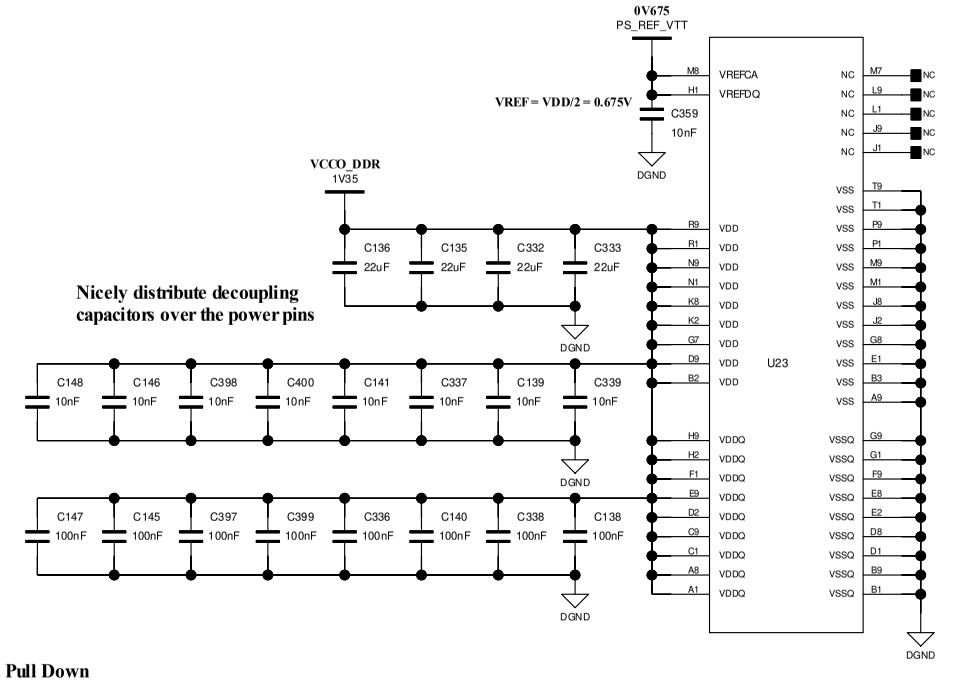
Sheet 11 of 35 A3

Date 2020-01-31



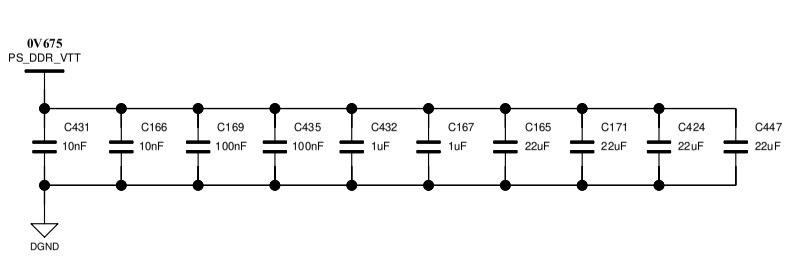
PS DDR termination
Note: All termination resitors 1%

NOTE:
RST_N_PL requires a Pull Down resistor through FPGA Configuration.
See UG93 Chapter 5 "DDR Termination"

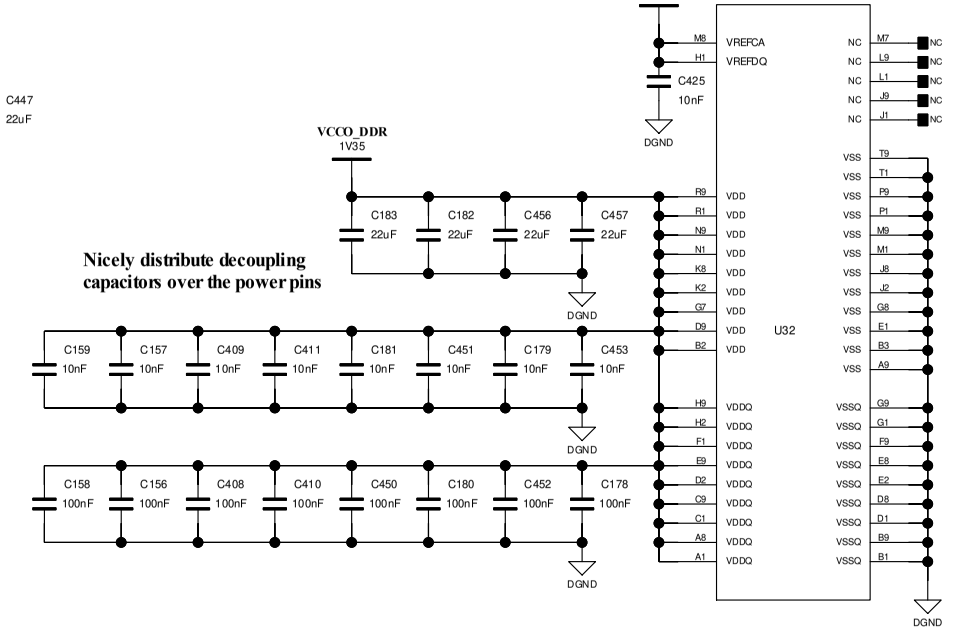


Nicely distribute decoupling capacitors over the power pins

Worst Case IDD per DDR device = 274 mA (datasheet Tabe 20, Idd7)

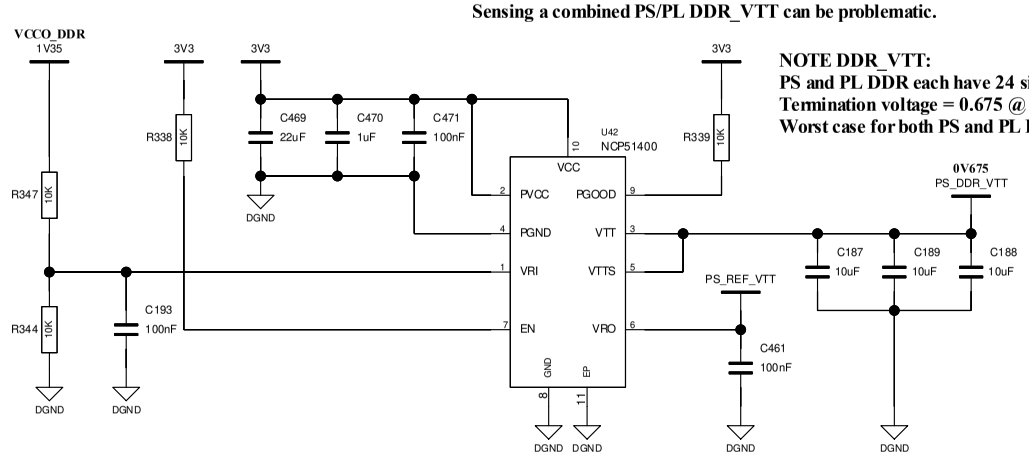


DDR PCB layout
See also UG933 Chapter 5.



Nicely distribute decoupling capacitors over the power pins

Separate DDR_VTT for PS
Note: Sense input VTTS needs to be connected to remote DDR termination bypass capacitors (see datasheet NCP51400).
Sensing a combined PS/PL DDR_VTT can be problematic.



NOTE DDR_VTT:
PS and PL DDR each have 24 signals to terminate.
Termination voltage = 0.675 @ 40.2 ohm = 16.8 mA per signal
Worst case for both PS and PL DDR: 2*24*16.8 mA = 806 mA

rev.	by	notes

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Project : WRITE

Sheetname : PS_DDR

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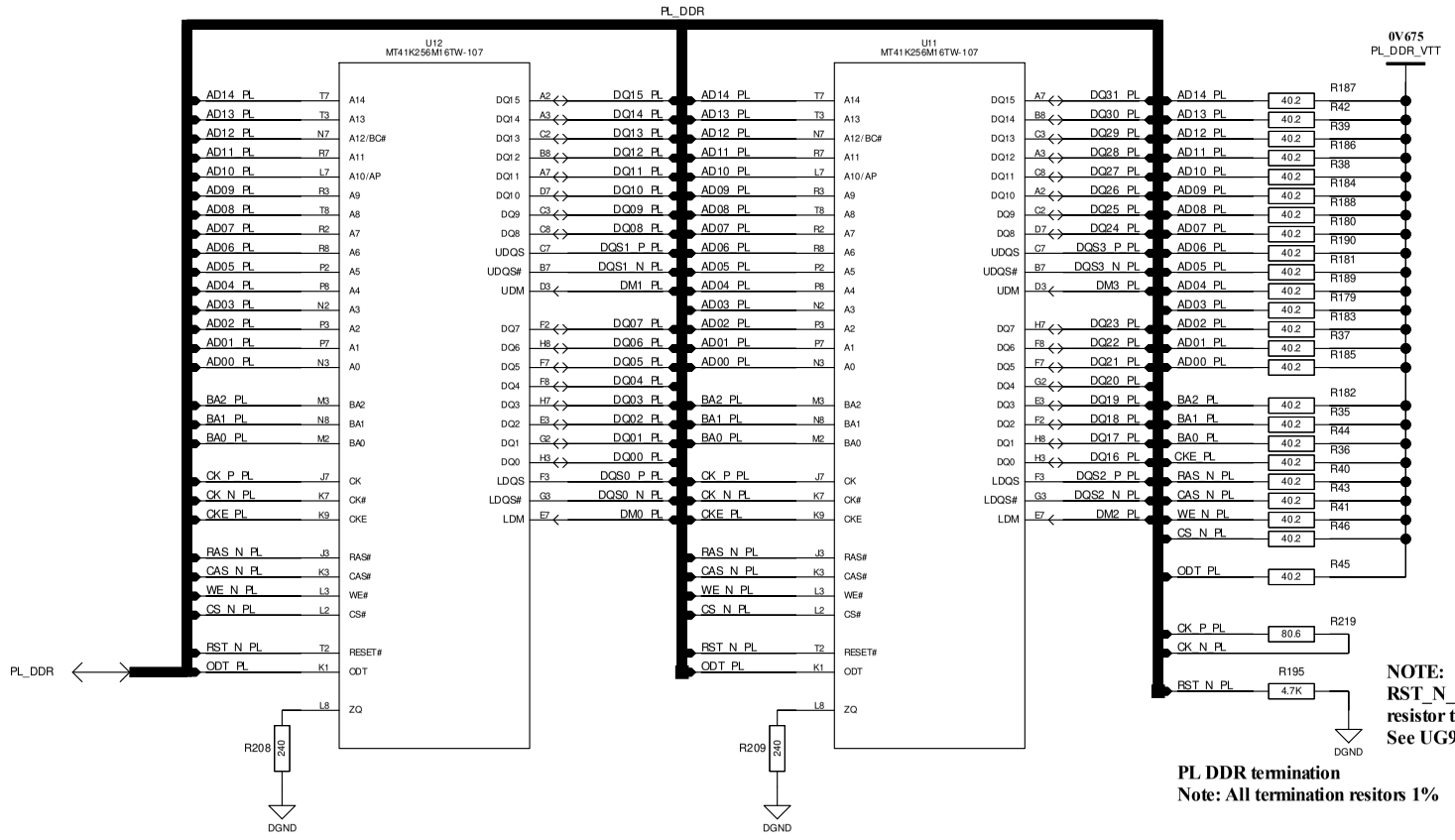
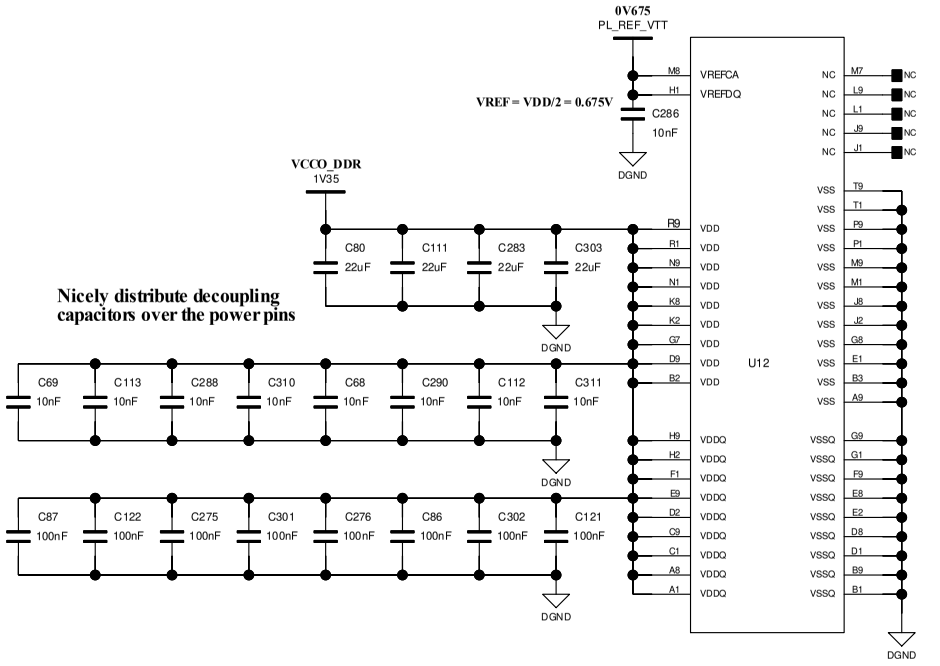
Sheet: 12 of 35 A3

Date: 2020-01-31

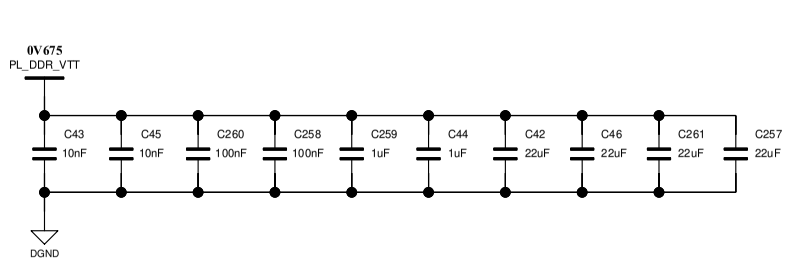


PL DDR termination
Note: All termination resitors 1%

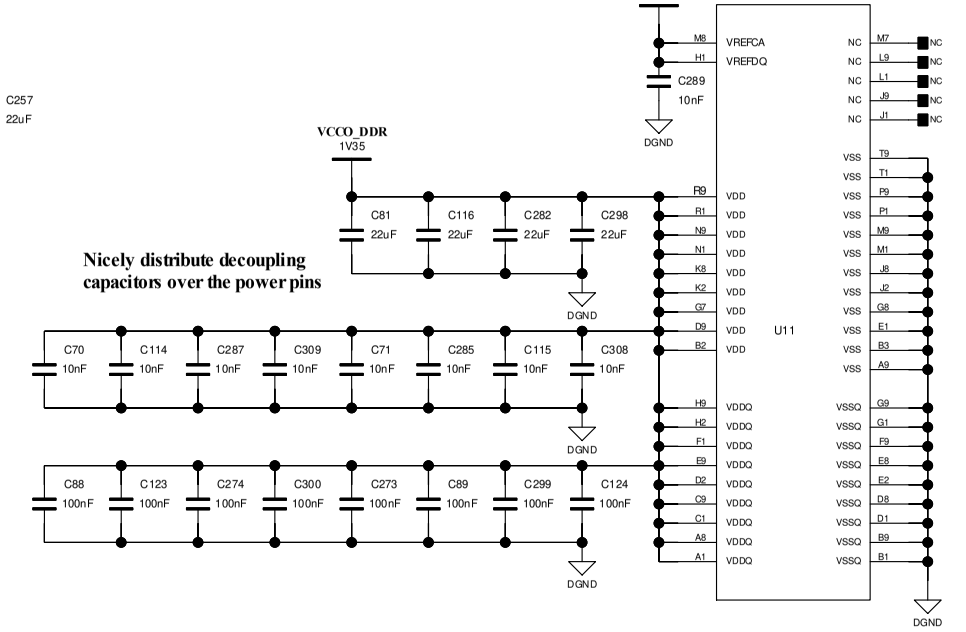
NOTE:
RST_N_PL requires a Pull Down resistor through FPGA Configuration.
See UG93 Chapter 5 "DDR Termination"



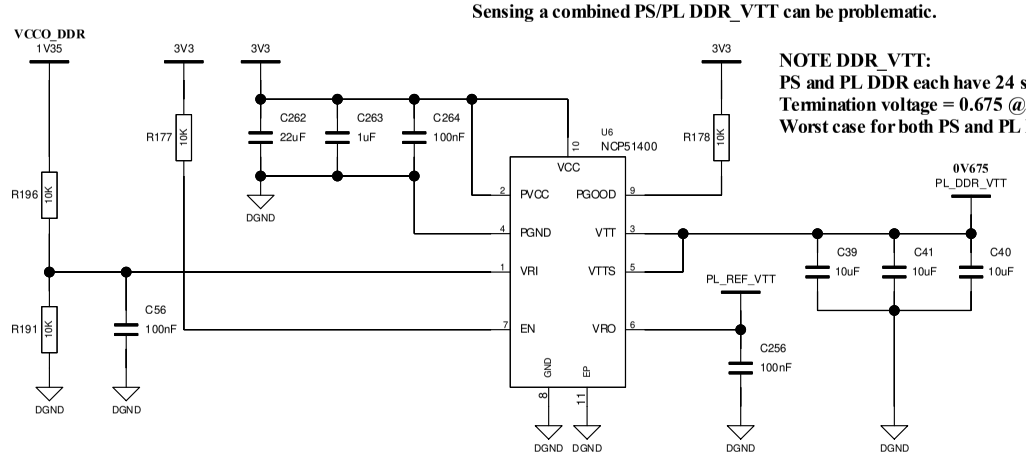
Worst Case IDD per DDR device = 274 mA
(datasheet Tabe 20, Idd7)



DDR PCB layout
See also UG933 Chapter 5.



Separate DDR_VTT for PL
Note: Sense input VTTS needs to be connected to remote DDR termination bypass capacitors (see datasheet NCP51400).
Sensing a combined PS/PL DDR_VTT can be problematic.



NOTE DDR_VTT:
PS and PL DDR each have 24 signals to terminate.
Termination voltage = 0.675 @ 40.2 ohm = 16.8 mA per signal
Worst case for both PS and PL DDR: 2*24*16.8 mA = 806 mA

rev.	by	notes

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Project : WRITE

Sheetname : PL_DDR

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Sheet: 13 of 35 A3

Date: 2020-01-31

Notes

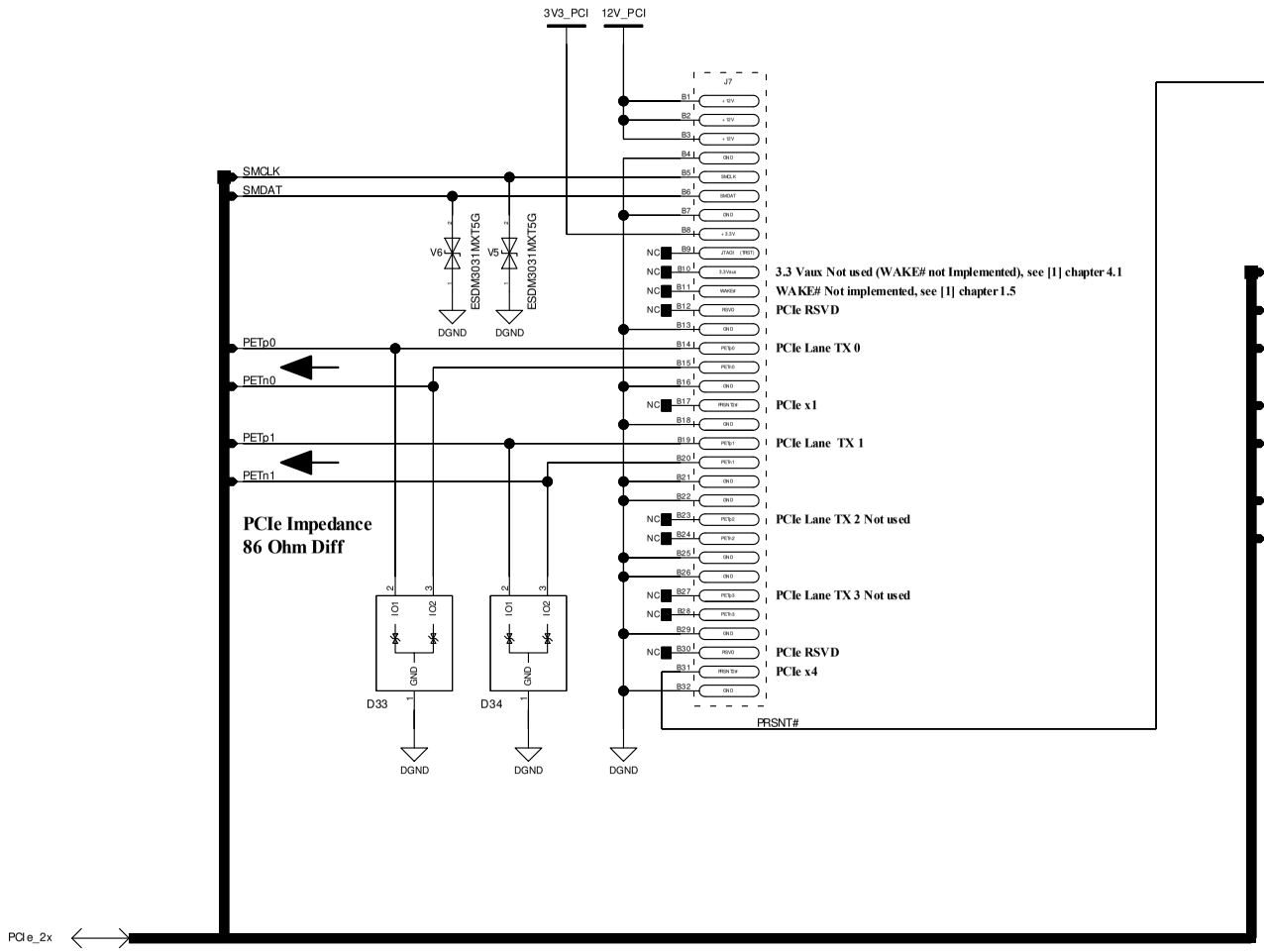
PCI_REFCLK PCIe 100MHz or 250 Mhz
PERpX/PERnX PCIe RX Datalane (Card 2 Motherboard, see 5.1 notes of referencce [1])
PETpX/PETnX PCIe TX Datalane (Motherboard 2 Card, see 5.1 notes of referencce [1])
12V_PCI: 25W Slot (2.1A max, [1] Table 4-1)
3V3_PCI: 25W Slot (3A max, [1] Table 4-1)

Precense detect, see [1] chapter 3.2
"PRSNT1# signal to the farthest-apart PRSNT2# signal with a single trace".
=> i.e. PCIe x4
PCIe x2 is possible see [1] chapter 6.3 "All PCI Express add-in cards must be able to negotiate and operate in all smaller Link widths from the full Link width down to x1. The x2 and x12 Link widths are optional."

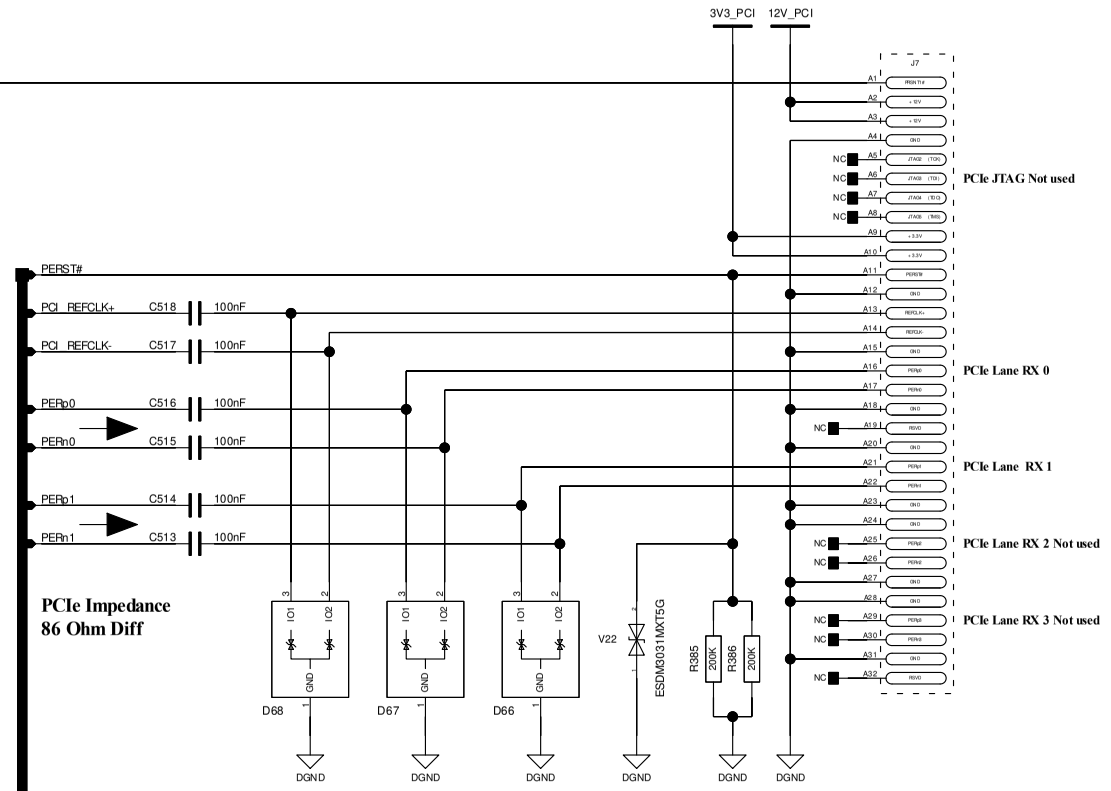
AC Coupling Capacitors (See 4.6.1 of reference [1])
Differential Data Trace Impedance 68-105 ohm (See 4.6.8. of reference [1])
Differential Data Trace Propagation Delay must not exceed 750 ps (See 4.6.9. of reference [1])
PCI connector mechanical dimensions see figure 5.3 of reference [1]
i.e. PCB thickness @ connector 1.57 [0.062]
PCI connector 30 u-inches Gold plating over 50 u-inches of nickel
(see 5.4.1 Environmental Requirements of reference [1])

[1] PCI Express Card Electromechanical Specification Revision 2.0

B Side edge connector



A Side edge connector



rev.	by	notes

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Project : WRITE
Sheetname : PL_PCIe_2x_Edge_Con

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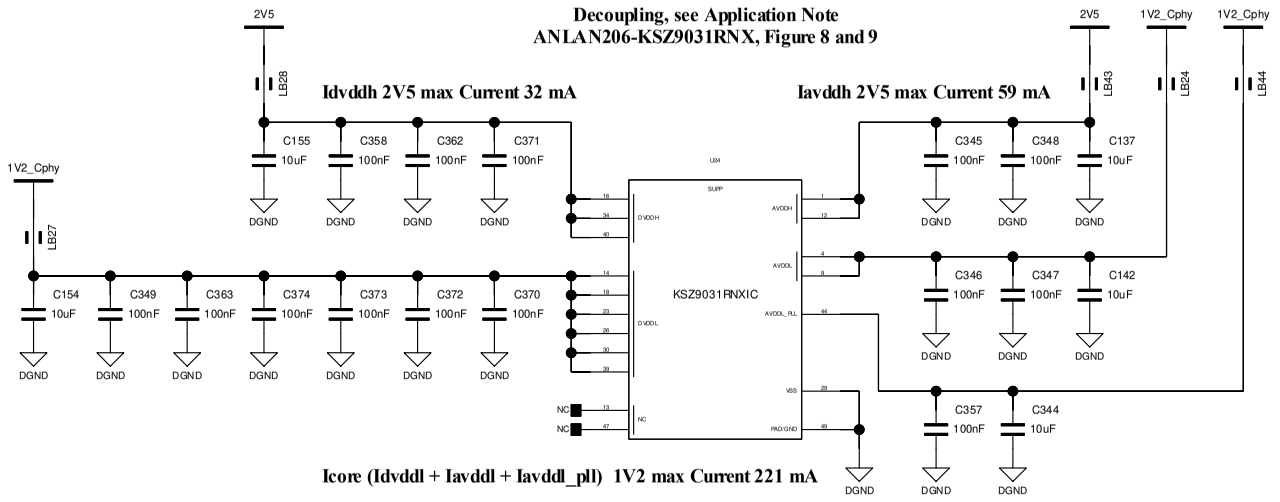

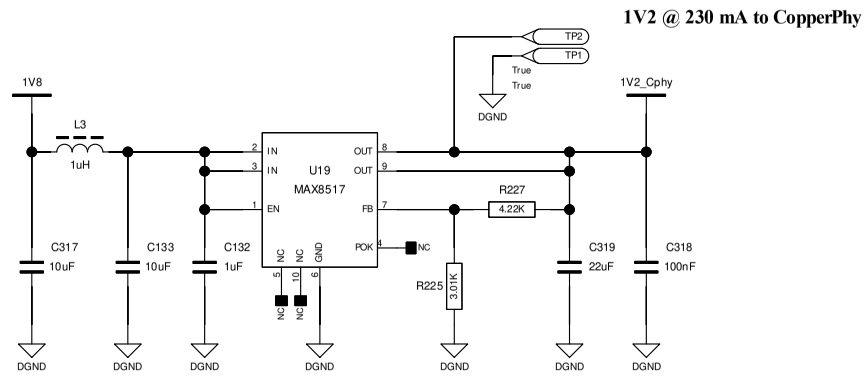

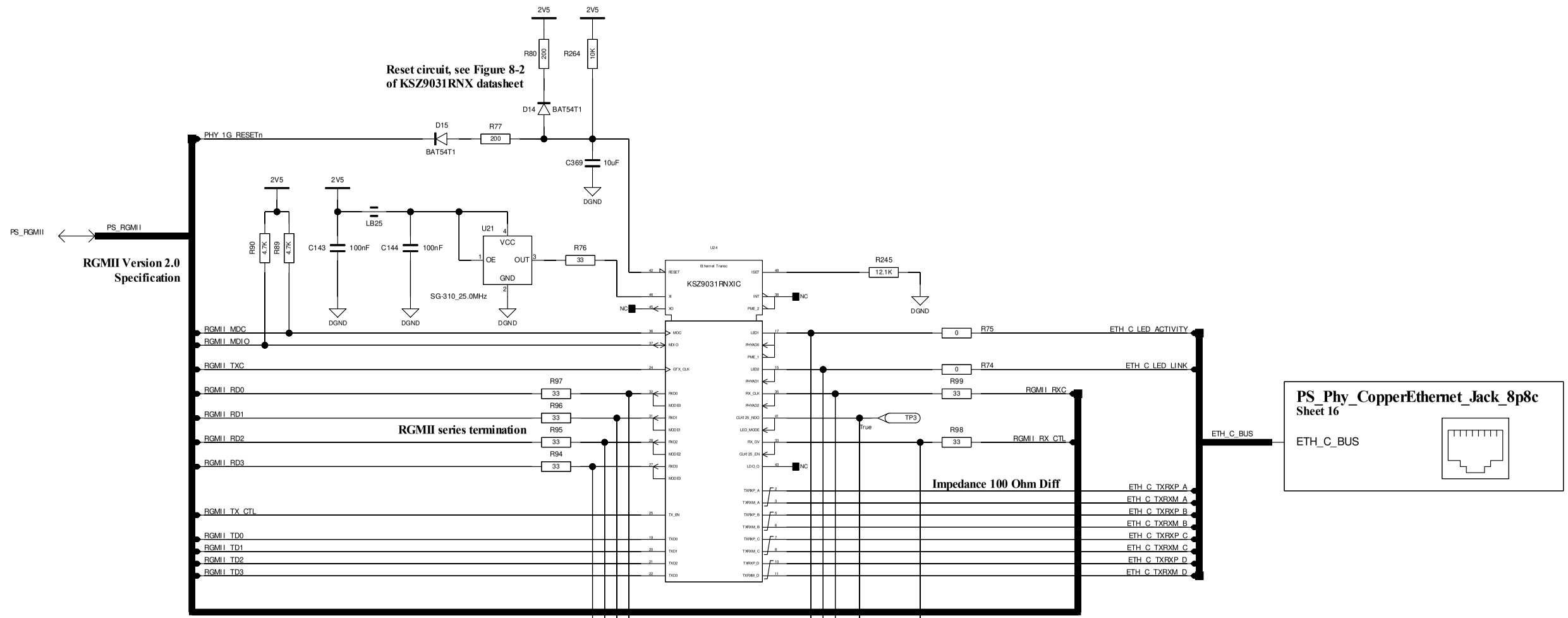

See KSZ9031RNX datasheet and KSZ9031RNX-EVAL schematics

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Project : WRITE
Sheetname : PS_Phy_CopperEthernet

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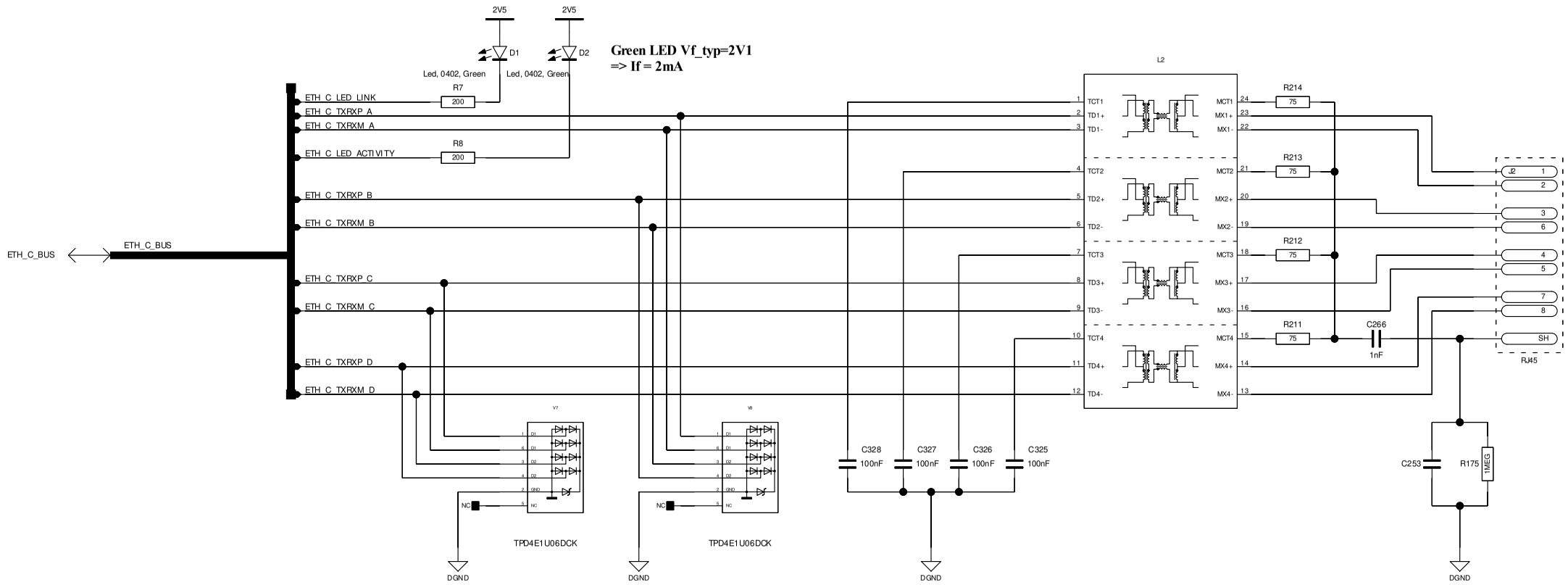

rev.	by	notes

SPEC7 v2 crystek Powered

Project : WRITE

Sheetname : PS_Phy_CopperEthernet_Jack_8p8c

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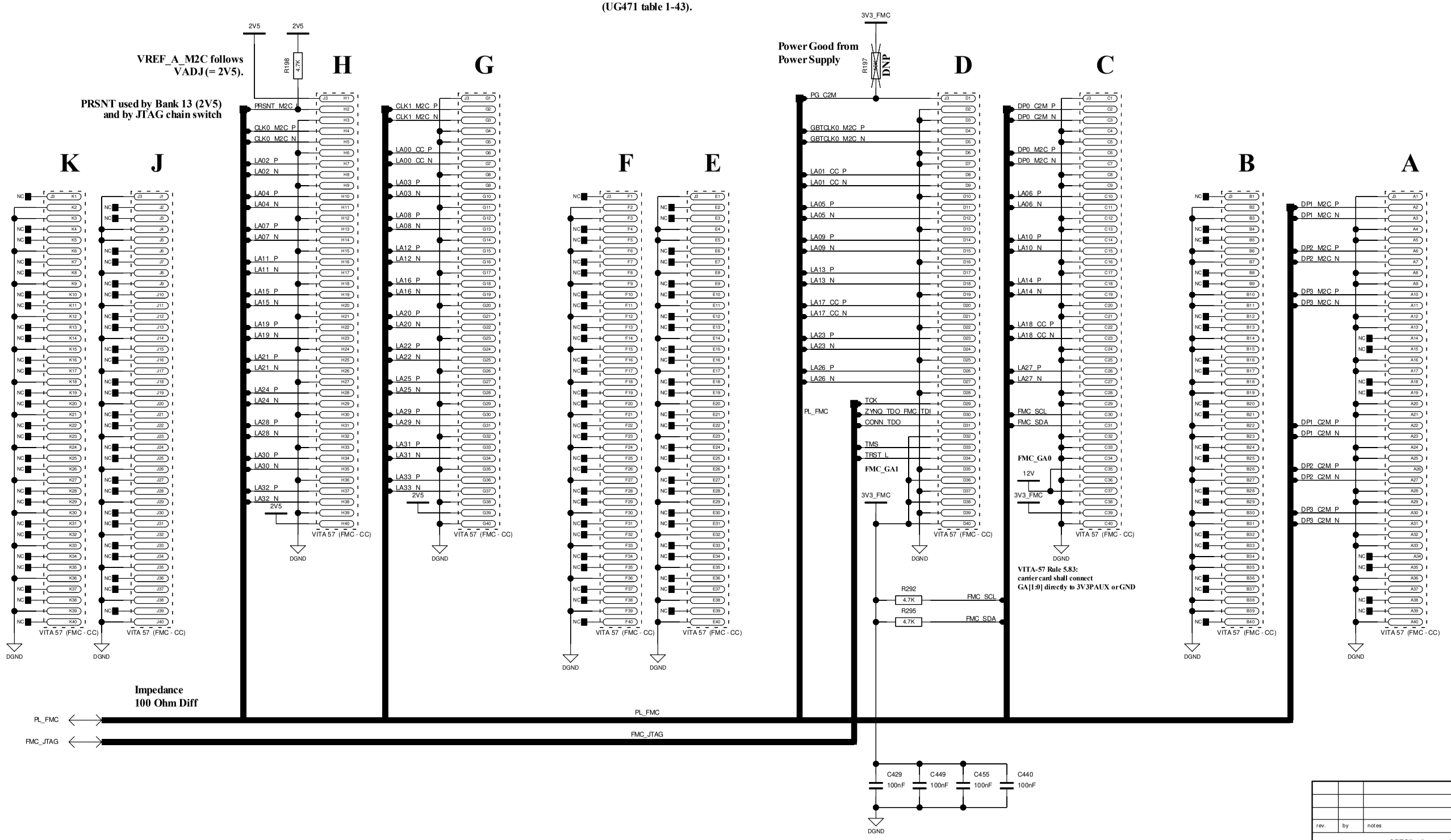
Date: 2020-01-31

LPC FMC

Note that only LPC FMC signals are implemented!
In addition, partial HPC multi-gigabit transceiver data pairs and all HPC grounds implemented.

Vadj fixed 2V5

The HR bank of the ZYNQ only allows LVDS_25 at VCCO 2V5
(UG471 table 1-43).



rev.	by	notes

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Project : WRITE
Sheetname : PL_FMC_Connector

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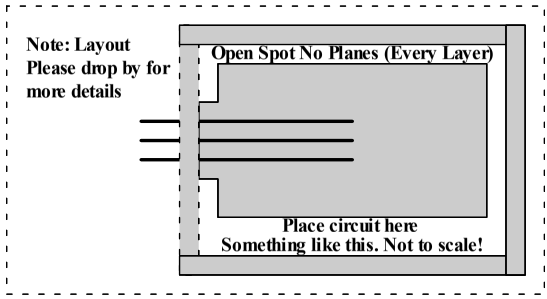
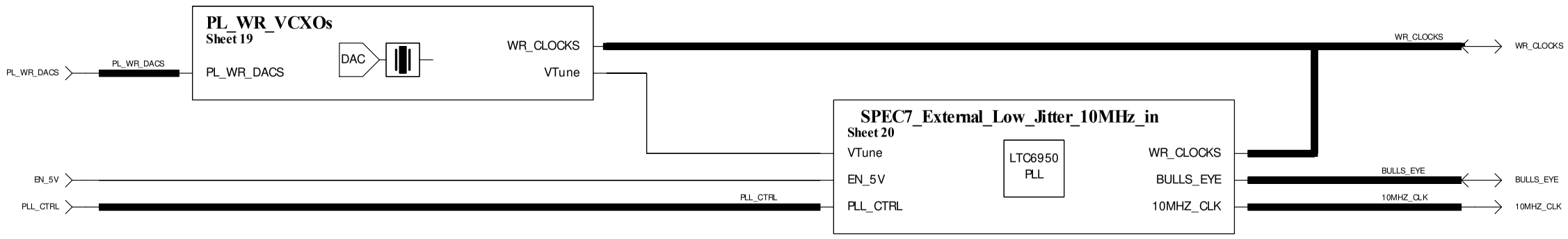
Date: 2020-01-31





rev.	by	notes

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Project	:	WRITE
Sheetname	:	PL_WR_Oscillators

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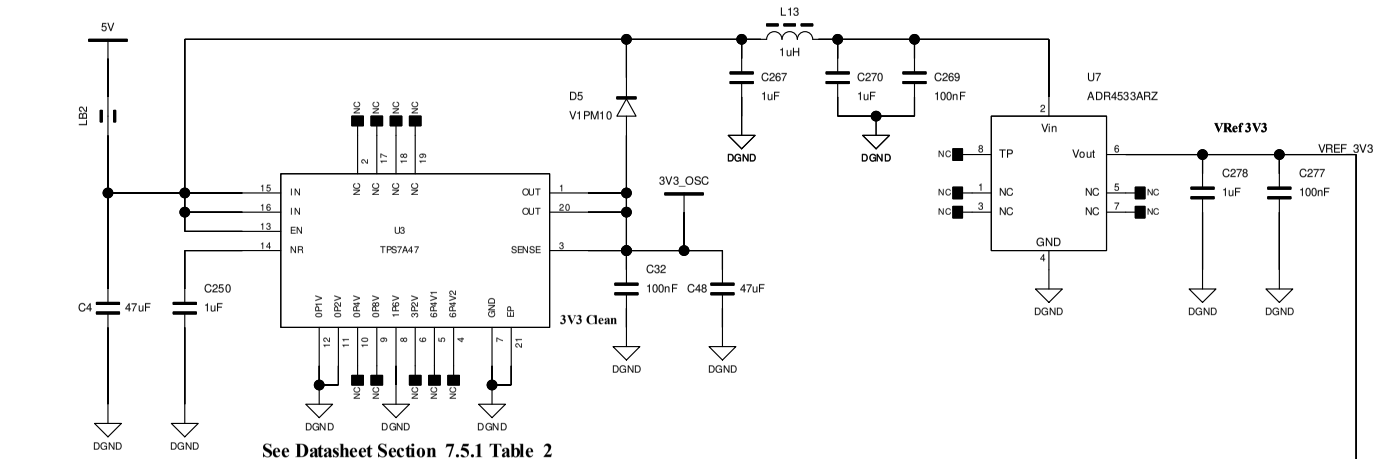
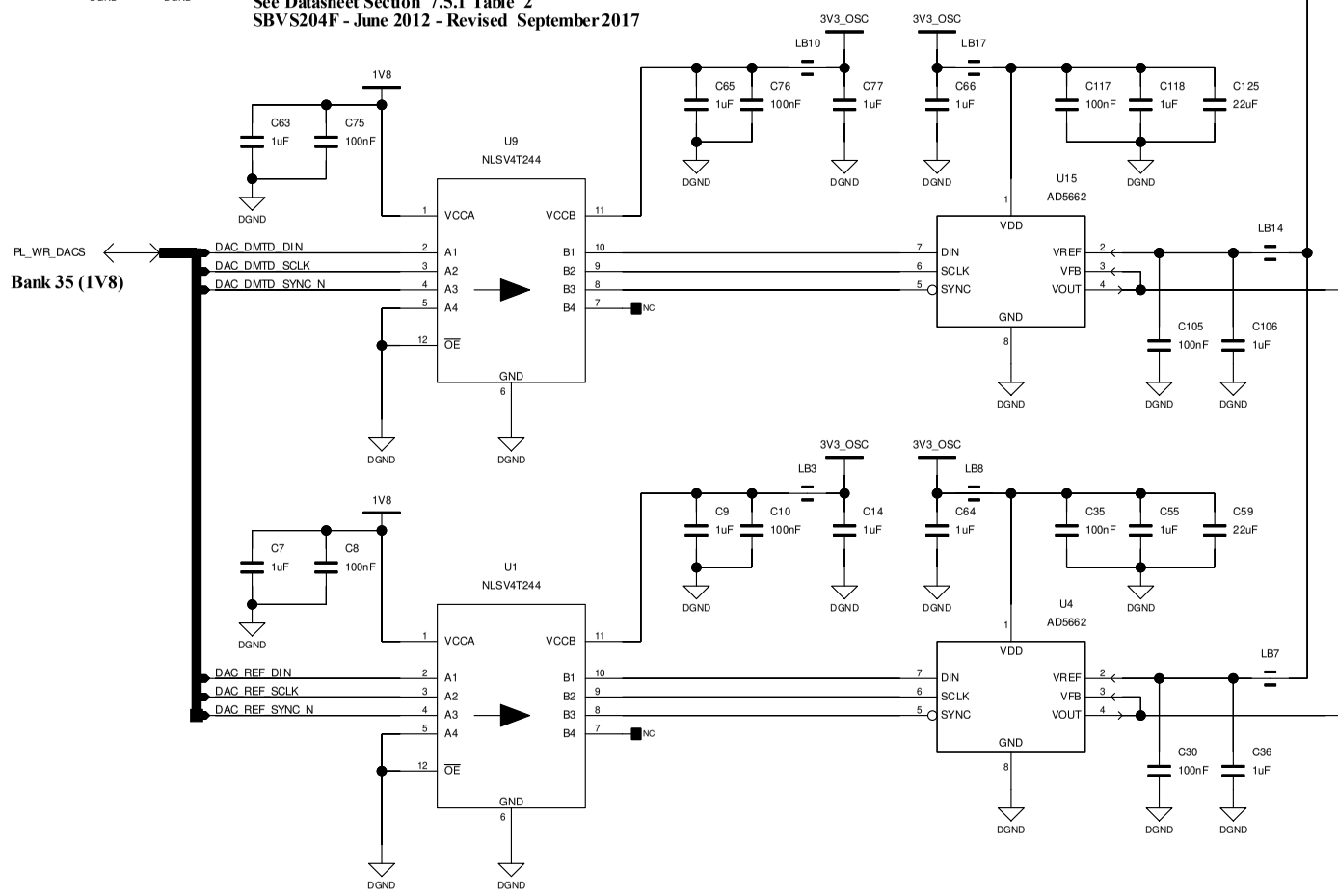
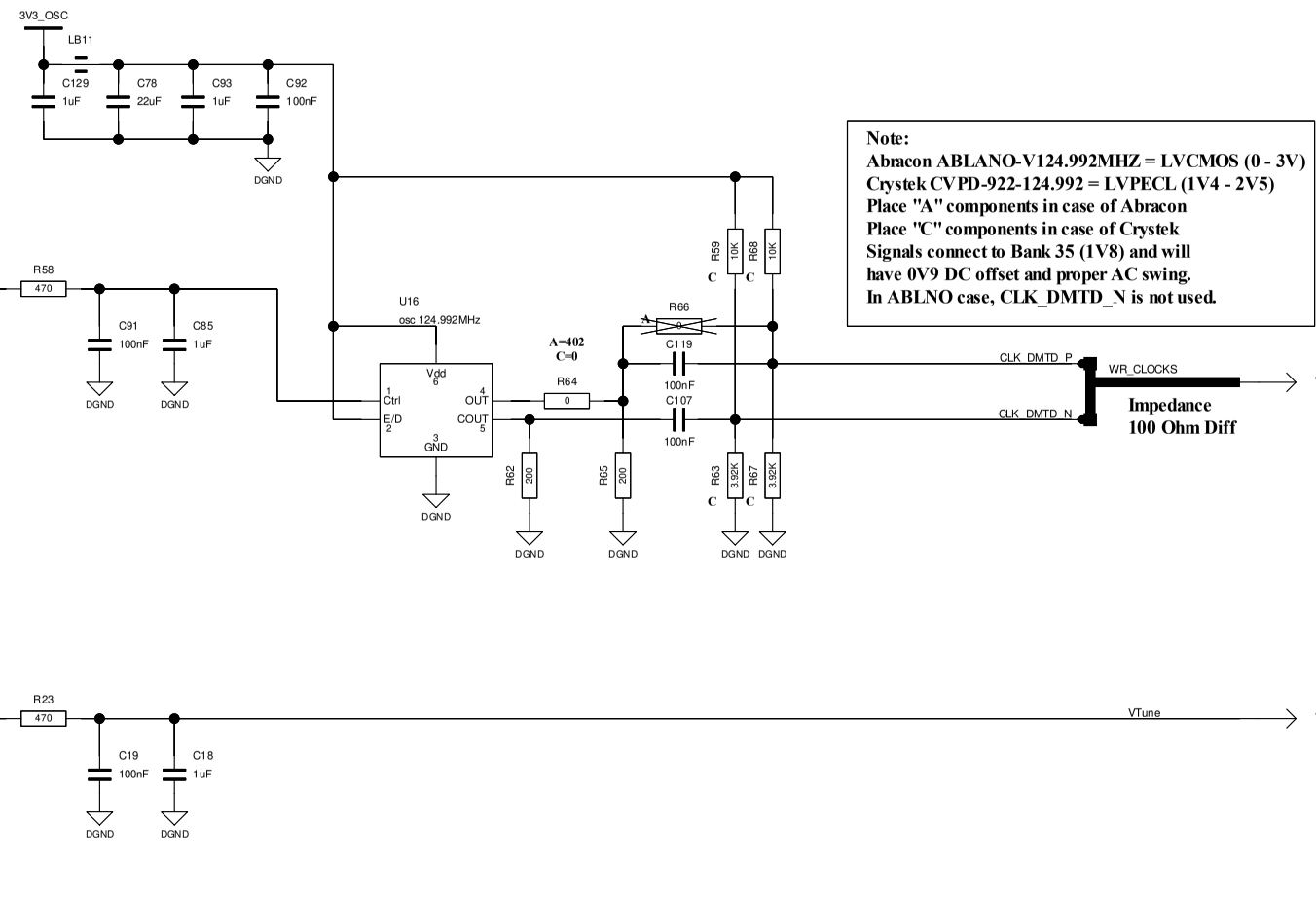
Size	420 x 297mm
Sheet	18 of 35 A3
Date	2020-01-31

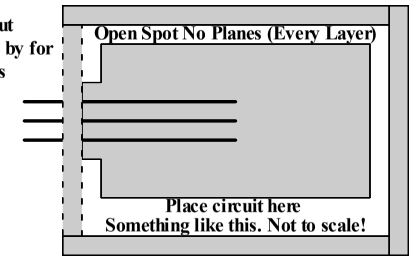


See Datasheet Section 7.5.1 Table 2
SBVS204F - June 2012 - Revised September 2017





Note: Layout
Please drop by for
more details



Note:
Abracon ABLANO-V124.992MHZ = LVCMOS (0 - 3V)
Crystek CVPD-922-124.992 = LVPECL (1V4 - 2V5)
Place "A" components in case of Abracon
Place "C" components in case of Crystek
Signals connect to Bank 35 (1V8) and will have 0V9 DC offset and proper AC swing.
In ABLNO case, CLK_DMTD_N is not used.

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Project : WRITE
Sheetname : PL_WR_VCXOs

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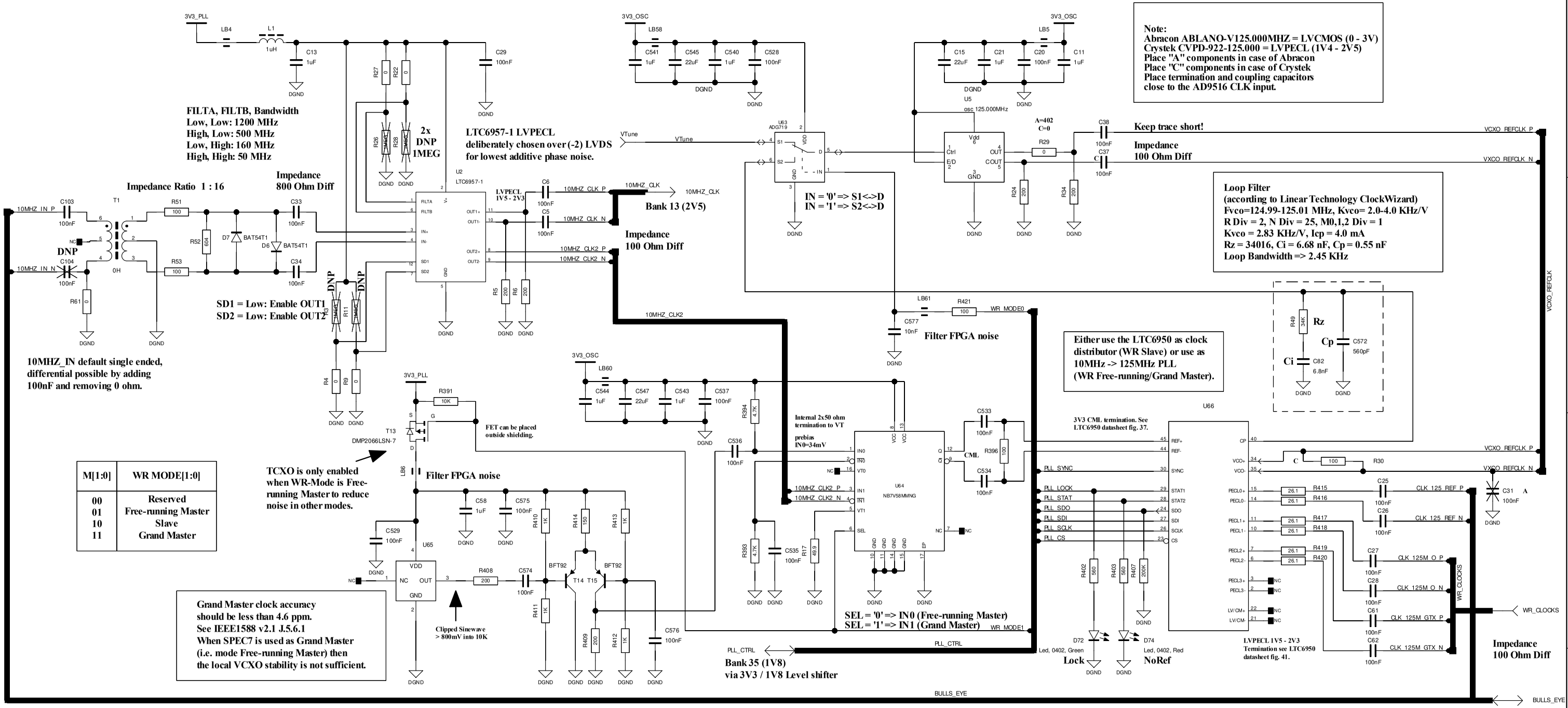
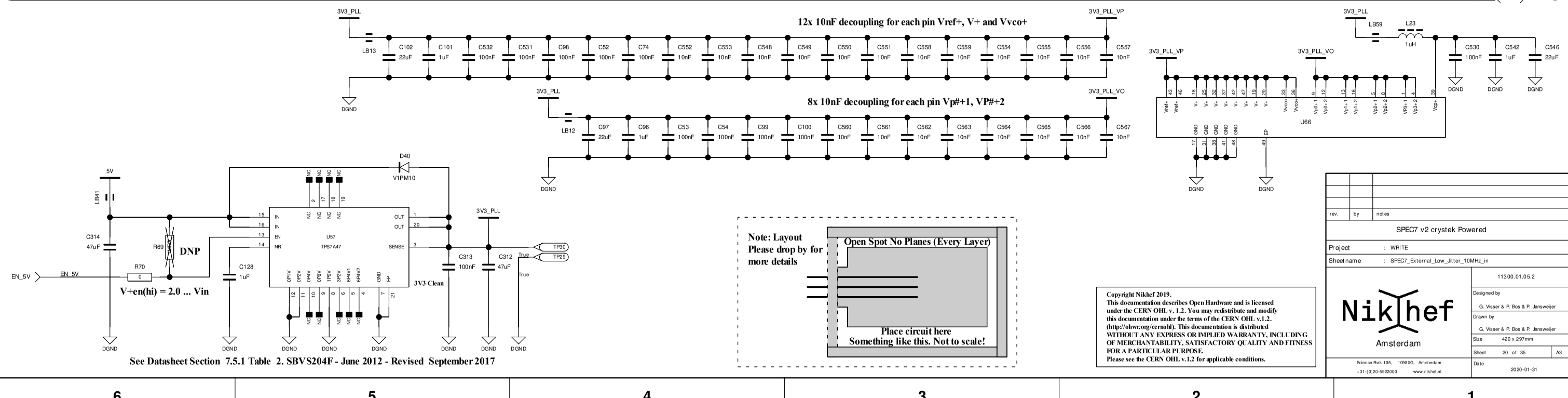
Size: 420 x 297mm
Sheet: 19 of 35 A3
Date: 2020-01-31


Note:
Abracon ABLANO-V125.000MHZ = LVCMOS (0 - 3V)
Crystek CVPD-922-125.000 = LVPECL (1V4 - 2V5)
Place "A" components in case of Abracon
Place "C" components in case of Crystek
Place termination and coupling capacitors close to the AD9516 CLK input.
FILTA, FILTB, Bandwidth
Low, Low: 1200 MHz
High, Low: 500 MHz
Low, High: 160 MHz
High, High: 50 MHz
LTC6957-1 LVPECL deliberately chosen over (-2) LVDS for lowest additive phase noise.
Impedance Ratio 1 : 16
Impedance 800 Ohm Diff
2x DNP 1MEG
SD1 = Low: Enable OUT1
SD2 = Low: Enable OUT2
10MHZ_IN default single ended, differential possible by adding 100nF and removing 0 ohm.
IN = '0' => S1<->D
IN = '1' => S2<->D
Keep trace short!
Impedance 100 Ohm Diff
Bank 13 (2V5)
Loop Filter
(according to Linear Technology ClockWizard)
Fvco=124.99-125.01 MHz, Kvco= 2.0-4.0 KHz/V
R Div = 2, N Div = 25, M0,1,2 Div = 1
Kvco = 2.83 KHz/V, Icp = 4.0 mA
Rz = 34016, Ci = 6.68 nF, Cp = 0.55 nF
Loop Bandwidth => 2.45 KHz
Filter FPGA noise
Either use the LTC6950 as clock distributor (WR Slave) or use as 10MHz -> 125MHz PLL (WR Free-running/Grand Master).
3V3 CML termination. See LTC6950 datasheet fig. 37.
FET can be placed outside shielding.
TCXO is only enabled when WR-Mode is Free-running Master to reduce noise in other modes.
Internal 2x50 ohm termination to VT prebias IN0=34mV
SEL = '0' => IN0 (Free-running Master)
SEL = '1' => IN1 (Grand Master)
Grand Master clock accuracy should be less than 4.6 ppm.
See IEEE1588 v2.1 J.5.6.1
When SPEC7 is used as Grand Master (i.e. mode Free-running Master) then the local VCXO stability is not sufficient.
Clipped Sinewave > 800mV into 10K
Bank 35 (1V8) via 3V3 / 1V8 Level shifter
Lock
NoRef
LVPECL 1V5 - 2V3 Termination see LTC6950 datasheet fig. 41.
Impedance 100 Ohm Diff
M[1:0]
WR MODE[1:0]
00 Reserved
01 Free-running Master
10 Slave
11 Grand Master


12x 10nF decoupling for each pin Vref+, V+ and Vvco+
8x 10nF decoupling for each pin Vp#+1, VP#+2
See Datasheet Section 7.5.1 Table 2. SBVS204F - June 2012 - Revised September 2017
Note: Layout Please drop by for more details
Open Spot No Planes (Every Layer)
Place circuit here
Something like this. Not to scale!
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Project : WRITE
Sheetname : SPEC7_External_Low_Jitter_10MHz_in
11300.01.05.2
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Drawn by G. Visser & P. Bos & P. Jansweijer
Size 420 x 297mm
Sheet 20 of 35
A3
Date 2020-01-31
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Bulles-Eye land pattern must be FILLED VIA-IN-PAD
plated with 30 u-inches Gold plating over 50 u-inches of nickel,
same as defined for the PCIe connector (see 5.4.1 Environmental
Requirements (PCI Express Card Electromechanical Specification Revision 2.0)

BULLS_EYE

AC coupled LVDS =
Bank 35 (HP)

PPS_OUT_P
PPS_OUT_N
10MHZ_OUT_P
10MHZ_OUT_N
CLK_125_REF_P
CLK_125_REF_N
BE_TXP — C331 100nF
BE_TXN — C330 100nF
ABSCAL_TXTS_P
ABSCAL_TXTS_N
SPARE_P
SPARE_N
PPS_IN_P
PPS_IN_N
10MHZ_IN_P — C385 100nF
10MHZ_IN_N — C384 100nF
BE_REFCLK_P
BE_REFCLK_N
BE_RXP — C381 100nF
BE_RXN — C380 100nF
BE_DMTD_P — C519 100nF
BE_DMTD_N — C520 100nF

J4
BDR-J-24

P PPS_OUT
N
P 10MHZ_OUT
N
P 125MHz Reference Clock OUT
N
P TX Spare GTX OUT
N
P ABSCAL_TXTS OUT
N
P General Purpose Spare OUT
N
P PPS_IN (used in Grand Master mode)
N
P 10MHZ_IN (used in Grand Master mode)
N
P Reference Clock IN, Spare GTX
N
P RX Spare GTX IN
N
P DMTD Spare IN
N
PPS_IN Single Ended

General Purpose Spare OUT
(Non-re-clocked PPS when external
high performance Oscillator is used
and re-clocking is done there).
Reference Clock IN, Spare GTX
(Also 125 MHz Reference Clock
Input used for external high
performance oscillator)

Drawing on the board for pinname
overview of the BullsEye
A-side are OUT
B-side are IN

TIMING_SIGNALS

LVDS =>
Bank 35 (HP, 1V8)

ABSCAL_TXTS_P_O
ABSCAL_TXTS_N_O
Impedance 100 Ohm Diff
SPARE_O_P
SPARE_O_N

2V5 LB29 C162 1uF DGND
C163 22uF, C395 1uF, C394 100nF

U28
CDCLVD2102
VCC
Vac_ref
INP0
INN0
INP1
INN1
EN
GND PAD
OUTP0 OUTN0 OUTP1 OUTN1 OUTP2 OUTN2 OUTP3 OUTN3

LVDS
ABSCAL_TXTS_P
ABSCAL_TXTS_N
SPARE_P
SPARE_N

R282 100, R280 100

EN = '1' => two buffers enabled
See CDCLVD2102 datasheet Table 1

Impedance 100 Ohm Diff

D46 D45 D44 D47 D43 D42 D51 D50 D49 D48 D69

FILTA, FILTB, Bandwidth
Low, High: 160 MHz

3V3 LB56 L22 1uH C538 1uF DGND
C521 100nF DGND

U60
LTC6957-1
FILTA FILTB IN+ IN- SD1 SD2 V+ GND OUT1+ OUT1- OUT2+ OUT2-

Impedance
100 Ohm Diff

LVDS =>
Bank 35 (HP, 1V8)

10MHZ_P_O — C524 100nF — 10MHZ_OUT_P
10MHZ_N_O — C525 100nF — 10MHZ_OUT_N
R395 100
C522 100nF, C523 100nF

LVPECL
1V5 - 2V3

TP34 TP35 True
R389 200, R390 200, R387 200, R388 200

SD1 = Low: Enable OUT1
SD2 = Low: Enable OUT2

5V 3V3 LB57
D71 CMYD4448
C526 100nF, C539 1uF
R397 470
U61 NC7SZ125
D71 CMYD4448
D70 VBUS05L1-DD1
R401 100, R400 100

PPS_I

Bank 13 (HR, 2V5)

2V5 LB26
C153 1uF
C152 22uF, C151 1uF, C407 100nF
U30
CDCLVD2102

LVDS =>
Bank 35 (HP, 1V8)

BE_DMTD_P
BE_DMTD_N
PPS_IN_P
PPS_IN_N

DMTD_P_I
DMTD_N_I
PPS_P_I
PPS_N_I

EN = Open =>
two buffers enabled
See Table 1

R82 49.9, R81 49.9, R107 49.9, R106 49.9
C150 1uF, C161 100nF

2V5 LB47
C415 1uF, R102 10K
C396 22uF, C149 1uF, C160 100nF

LVDS =>
Bank 35 (HP, 1V8)

PPS_P_O
PPS_N_O
R92 100
U29
MAX9381
VCC D D CLK CLK VEE Q Q

LVPECL
PPS_OUT_P
PPS_OUT_N

CLK_125M_O_P
CLK_125M_O_N
Impedance 100 Ohm Diff
R104 100
no internal termination
R105 91, R93 91

Bias and Termination
must be put at the
end of the line.
R103 10K

WR_CLOCKS

Reclock PPS with
clean Reference Clock

Note:
10 MHz can not be re-clocked with 125 MHz.
For 50% duty Cycle a 500 MHz re-clock is needed.
SPEC7 forwards the 10MHz ouput clock from the FPGA to the Bulls-Eye.
For low jitter this 10 MHz ouput needs to be re-clocked with the
external high performance oscillator.

TIMING_SIGNALS

rev.	by	notes

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Project : WRITE
Sheetname : PL_BullsEye

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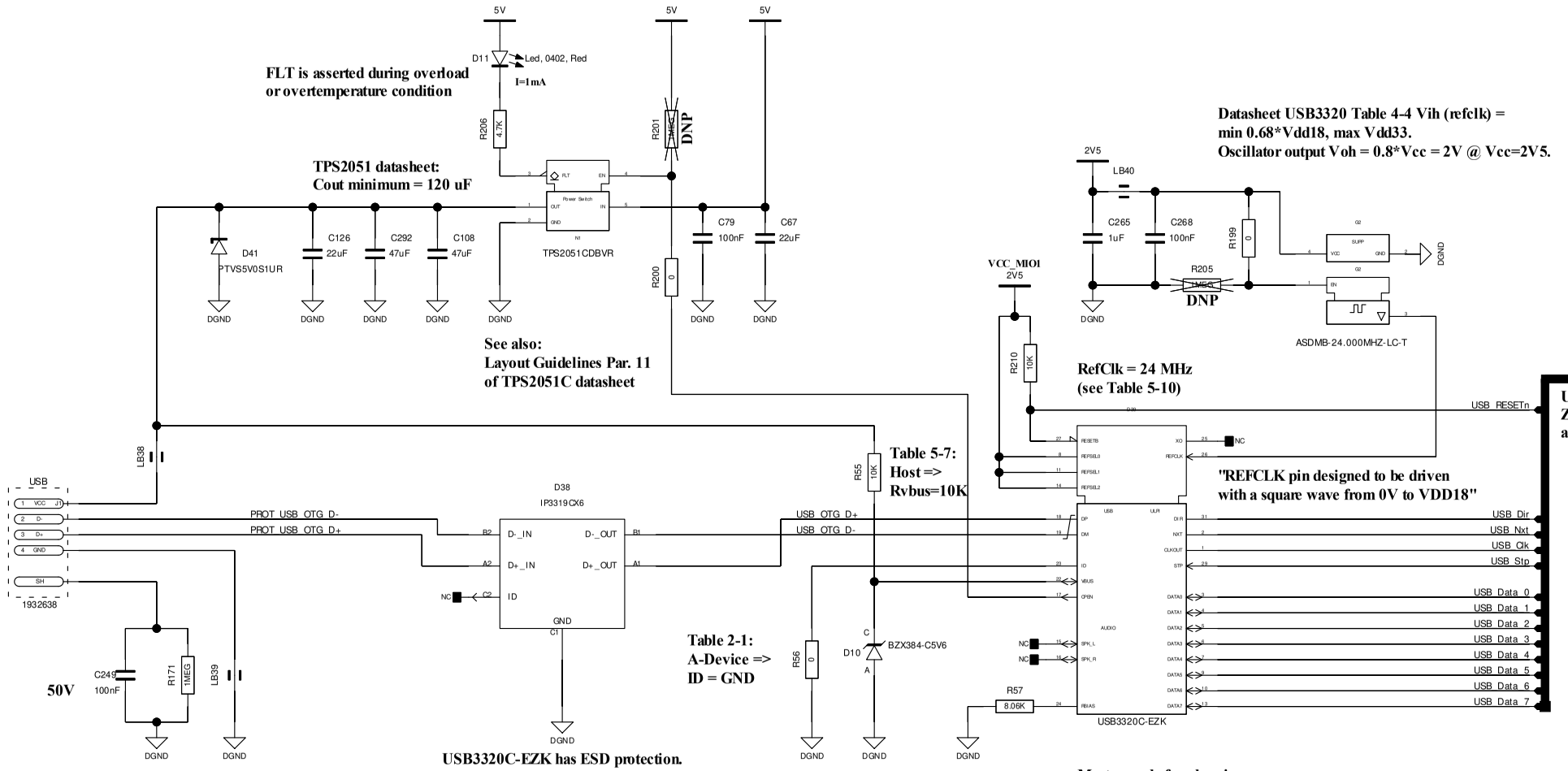
Sheet: 21 of 35 A3
Date: 2020-01-31

USB 2.0 A-Device (i.e. host)



rev.	by	notes

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Project : WRITE
Sheetname : PS_USB_OTG

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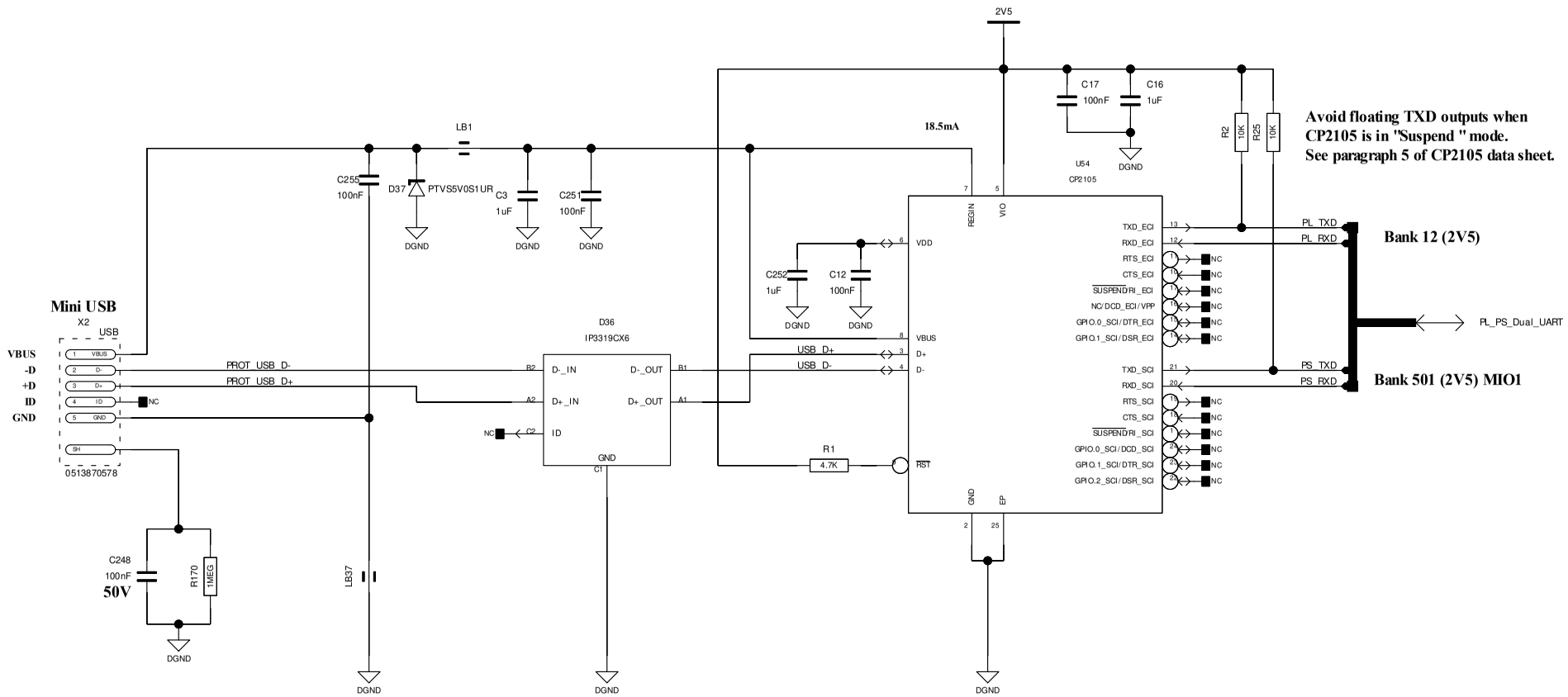
PL_USB
PS_USB



Diffrential impedance must 90 Ohm,See Universal Serial Bus Specification Revision 2.0 chapter 7.1

rev.	by	notes

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Project : WRITE

Sheetname : PL_PS_Uart

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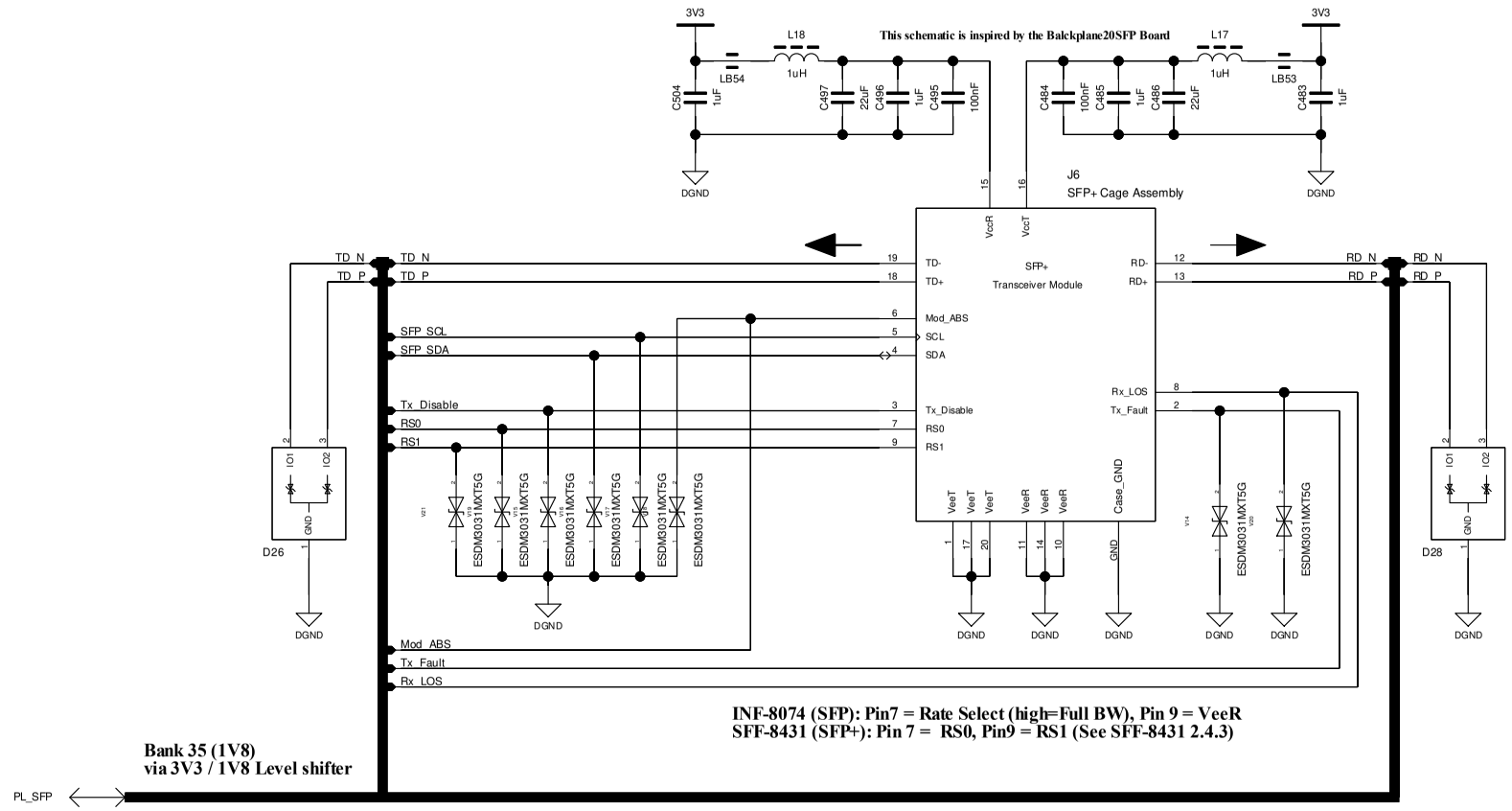

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Project : WRITE

Sheetname : PL_SFP_Connector

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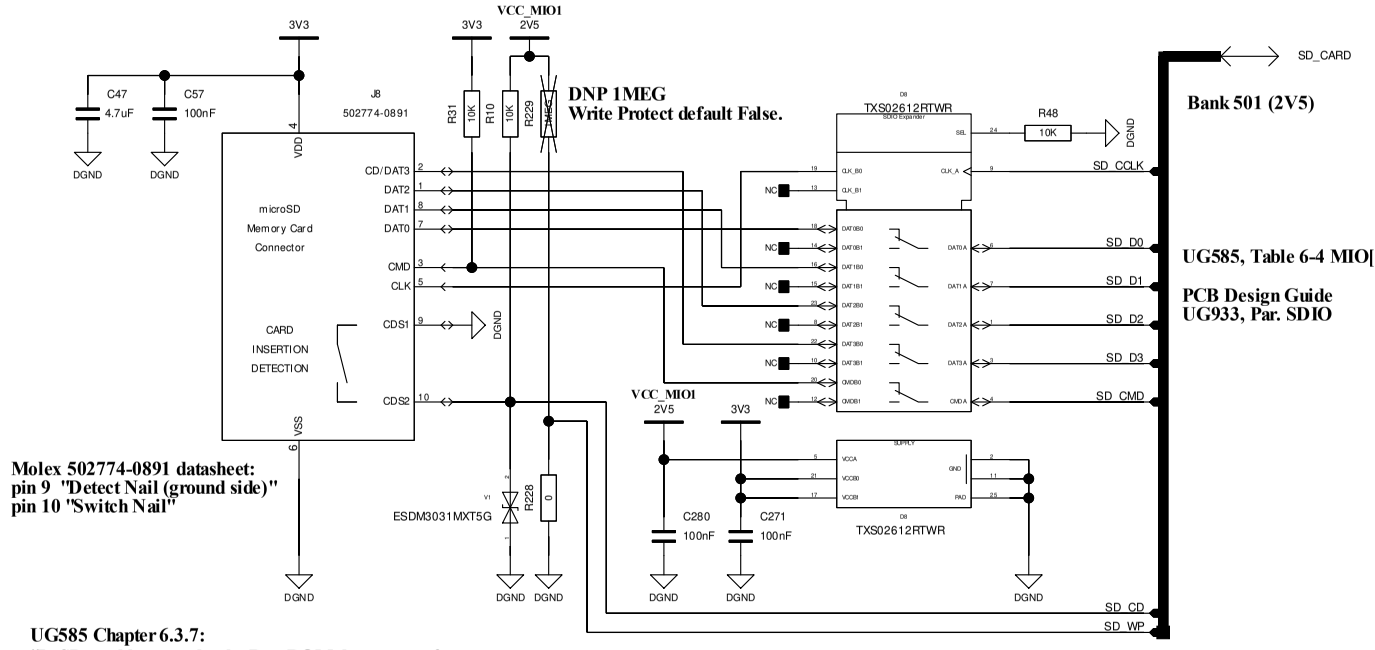
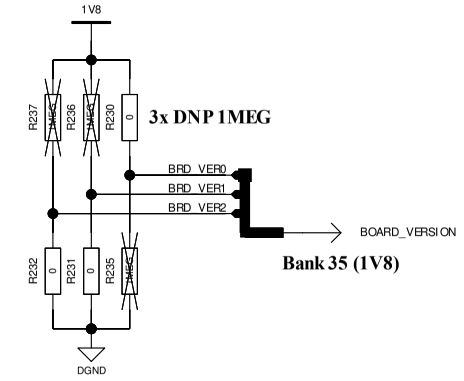
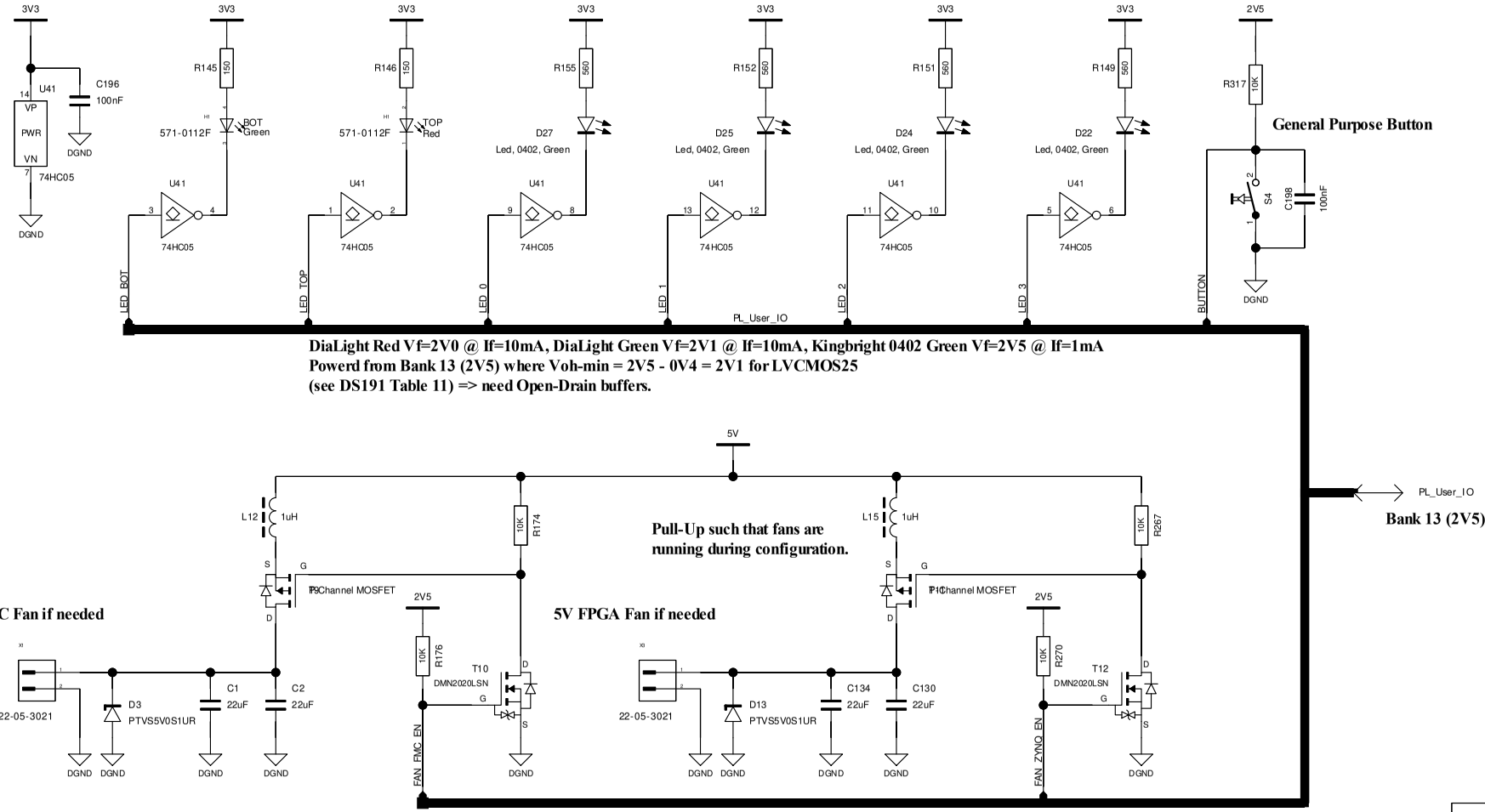


UG585 Chapter 6.3.7:
"In SD card boot mode, the BootROM does not perform a header search and does not support multiboot."

The Board Version can be hardcoded with this register array and readback via the FPGA.
Current version = 1





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Project : WRITE
Sheetname : PL_User_IO

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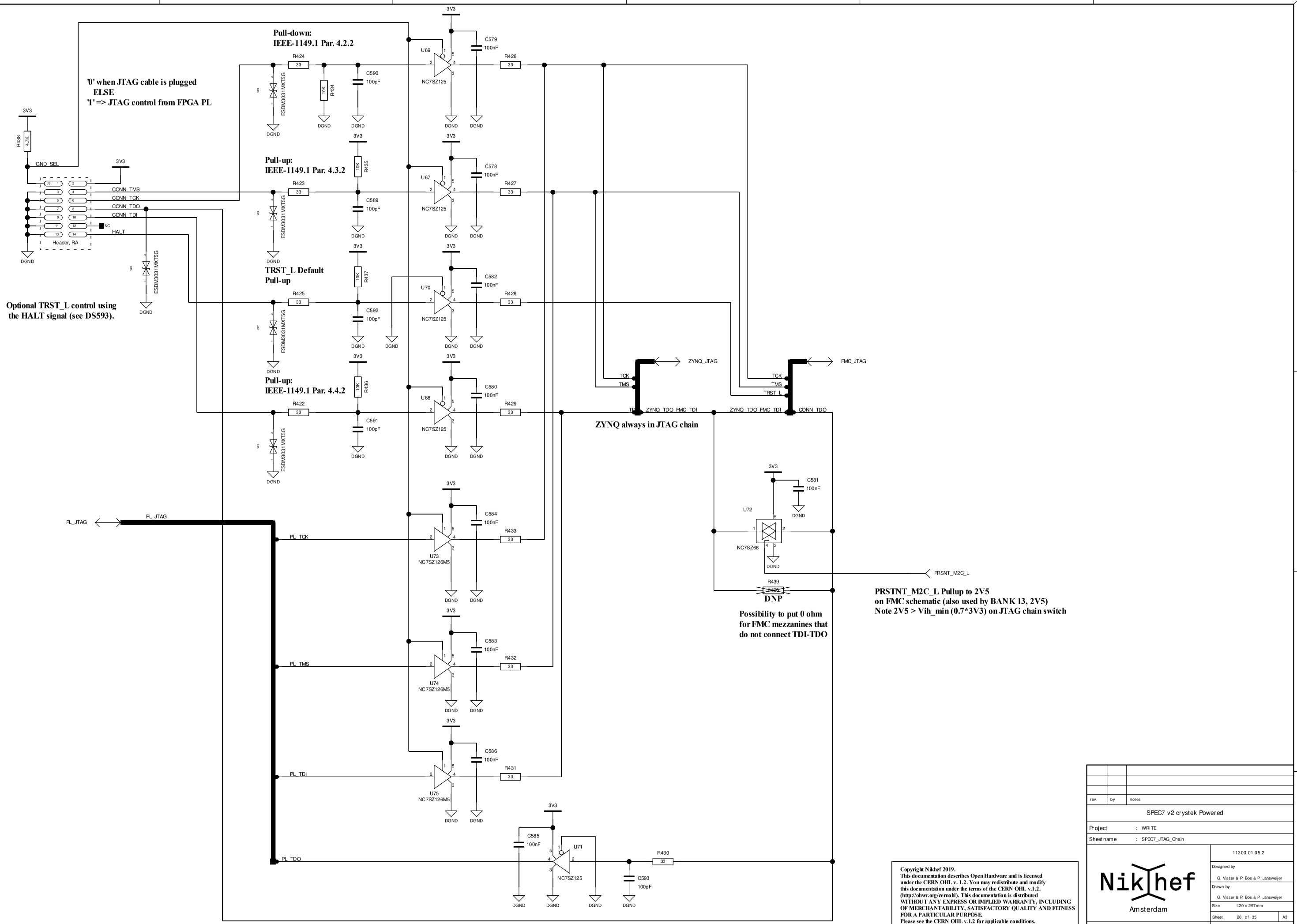

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Project : WRITE

Sheetname : SPEC7_JTAG_Chain

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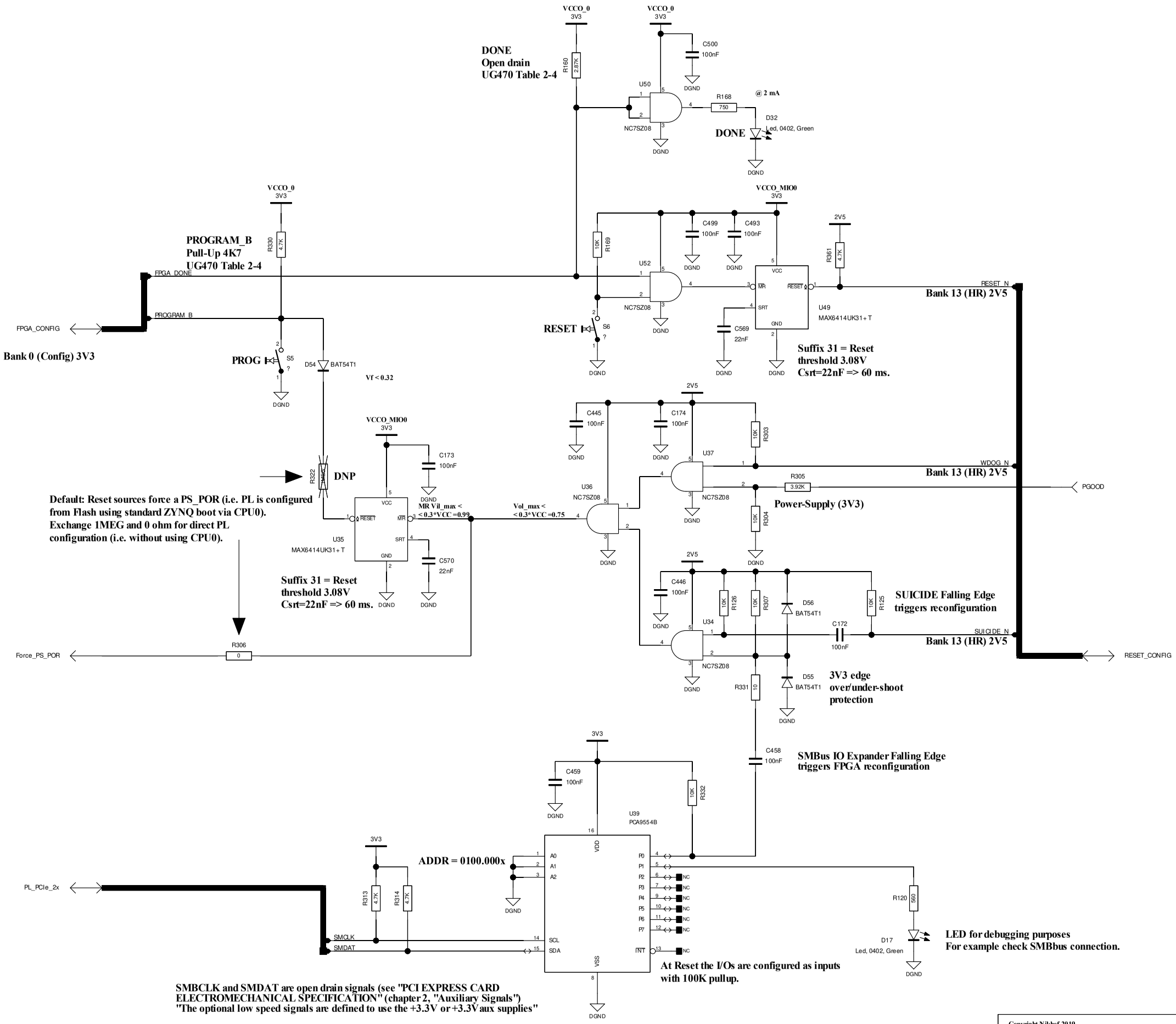

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Project : WRITE

Sheetname : SPEC7_Reset_Config

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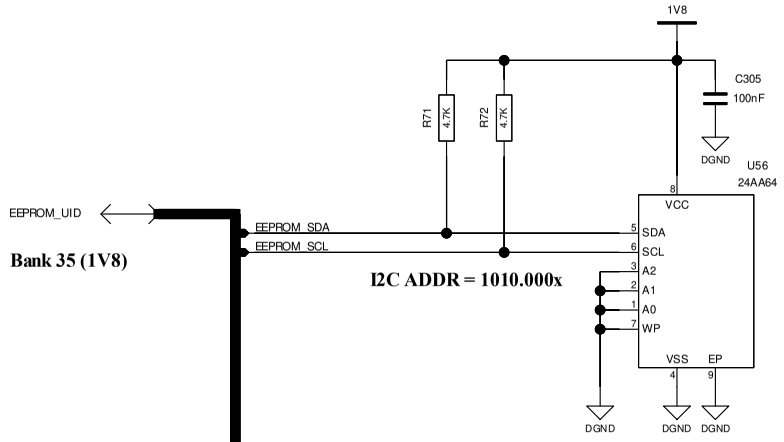

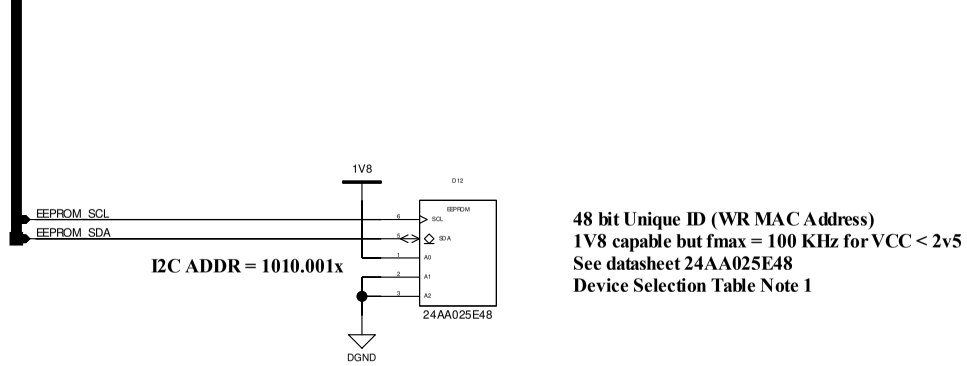

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Project : WRITE

Sheetname : PL_EEPROM_Unique_ID

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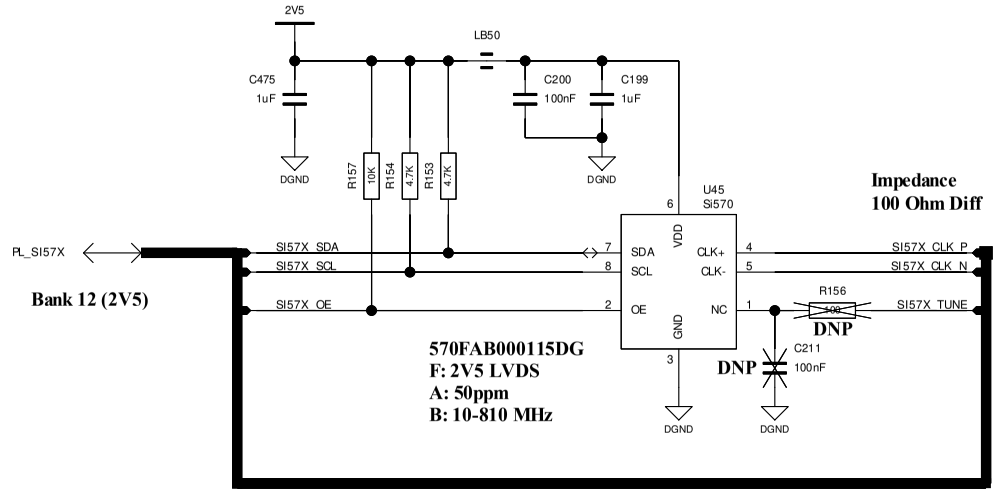

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Project : WRITE

Sheetname : PL_SI570

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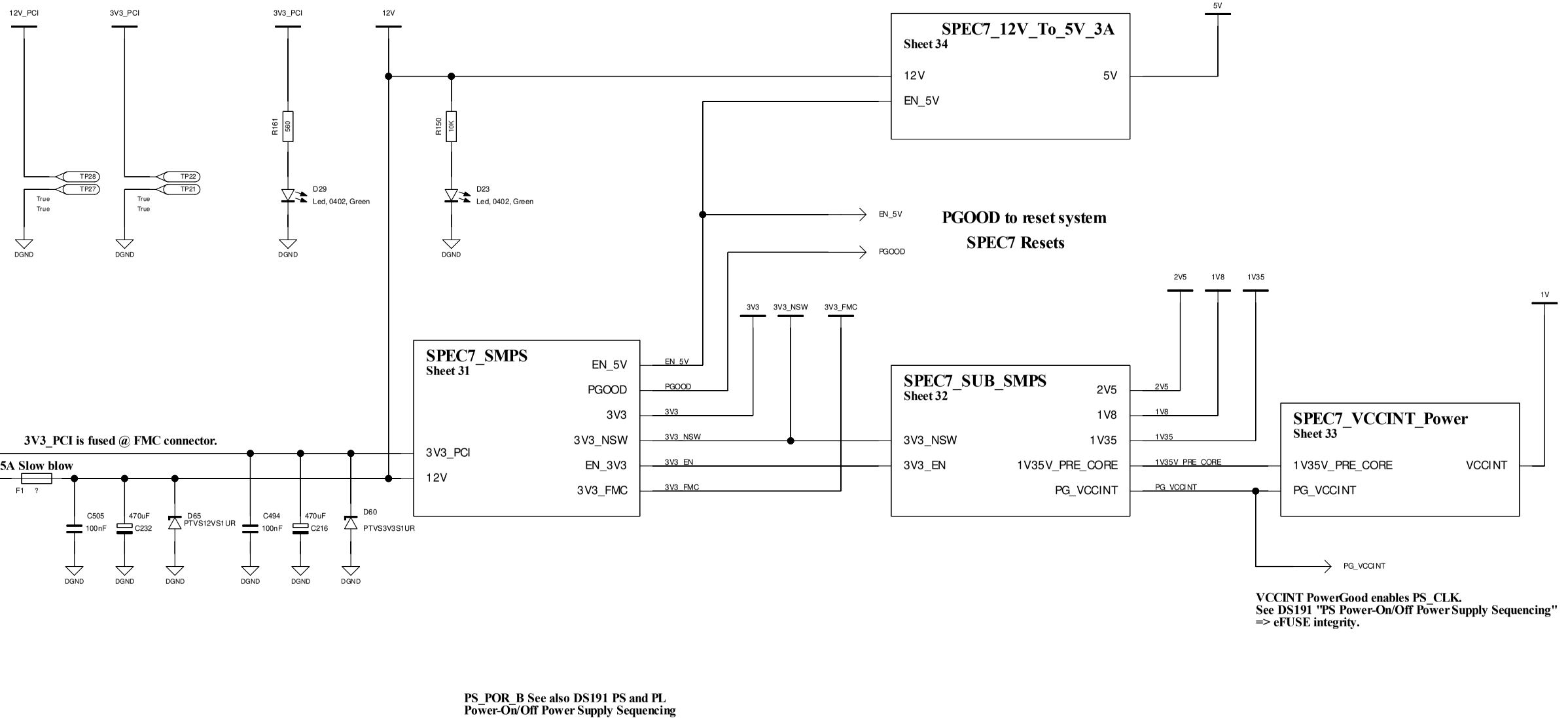

PS_POR_B See also DS191 PS and PL
Power-On/Off Power Supply Sequencing

UG585 Par. 6.1
Immediately after the PS_POR_B reset pin deasserts, the hardware samples the boot strap pins and optionally enables the PS clock PLLs. Then, the PS begins executing the BootROM code in the on-chip ROM to boot the system.

UG585 Par. 6.2.4. "External Reset Signal Pins" eFUSE integrity
uPC supervisory circuit ensures that PS_POR_B assreted low before VCCINT reaches 0.80V.

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SPEC7 v2 crystek Powered

Project : WRITE

Sheetname : SPEC7_Power_System

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3V3 @ 10A

Ven max = 3.6 V
Enabled when Ven > 1V2

Make the current loop so small as possible
47uF cap should be a 1210 package see datasheet

Place close as possible to switcher

N2
EN29A0QI

Compesation network Type III
See EN29A0Q1 datasheet
Figure 7 and Table 9

feedback network

Over Voltage Protection
set to 3V45.

Feedback network is referenced
to GNDSNS (Ground Ref point)

Note :

POK = Power is oke when Vout is +/- 10%
POK = Open Drain, High is oke.
POK = POK_3V3,Controls. 1V35 SMPS

Switch Freq set to 2 MHz.
Softstart 200 ms.
Output Overvoltage set to 3.45V.

Slowly turn on FET V3 to reduce inrush current.

Vgs protection.

Vgs protection

Note:

SPEC7 Resets
PGOOD to reset system

Dual MOSFETs eliminate current flow from V3_FMC_F to 3V3_NSW or 3V3_PCI or vice versa via MOSFET body diode.

PIN 1 - 19 (NC) may be connected to Vout
See EN29A0QI Table 2

PIN 87 (NC) May be connected to PVIN,VOUT,GDNG Planes
See EN29A0QI Table2

See also figure 9 Typical Appliction Circuit

When EN_3V3 And PCI_3V3 then route 3V3_PCI to 3V3_FMC
When EN_3V3 And NOT PCI_3V3 then route 3V3_NSW to 3V3_FMC

rev.	by	notes

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Project : WRITE
Sheetname : SPEC7_SMPS

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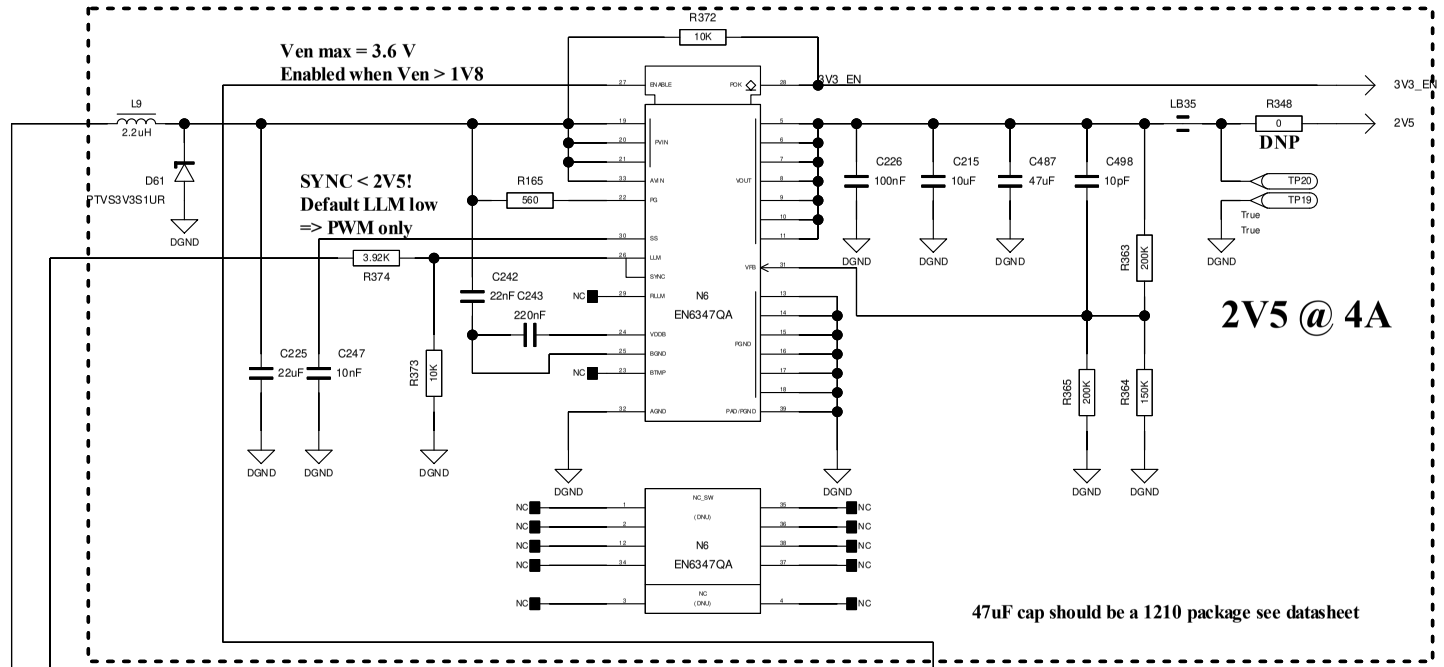

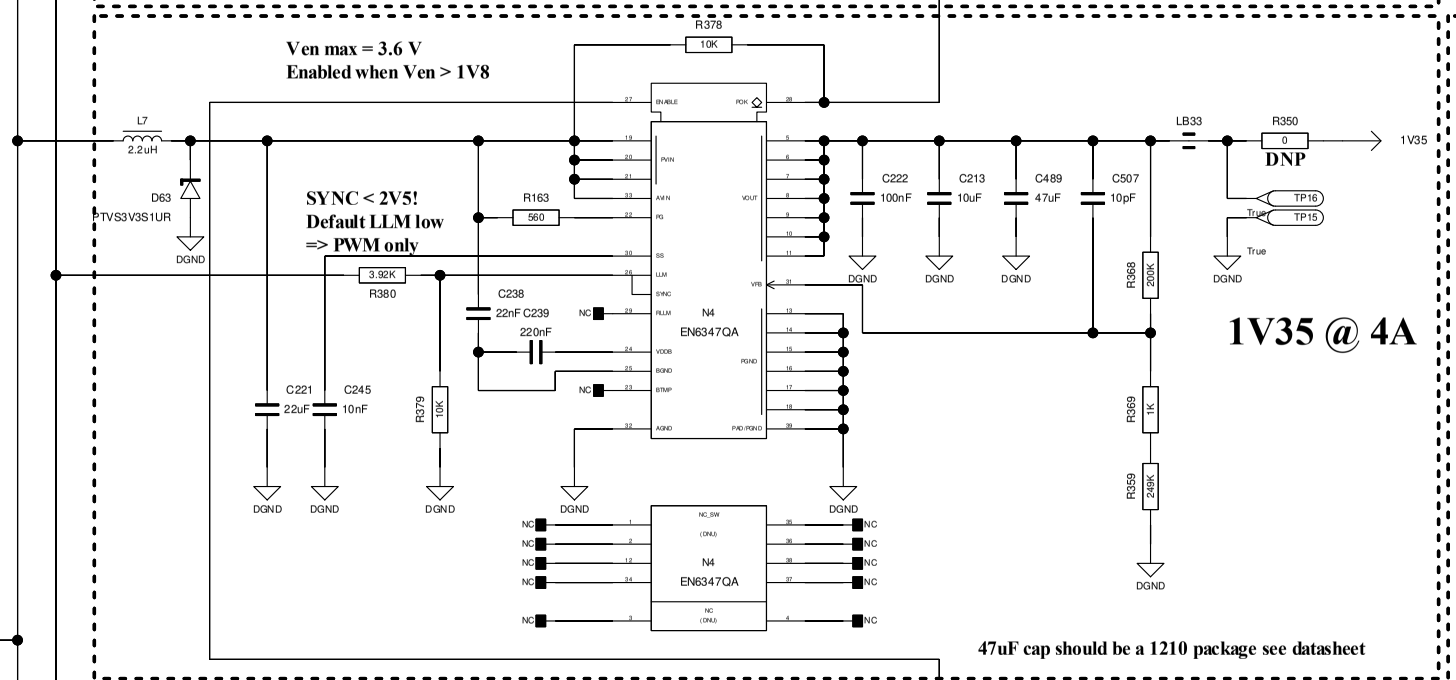

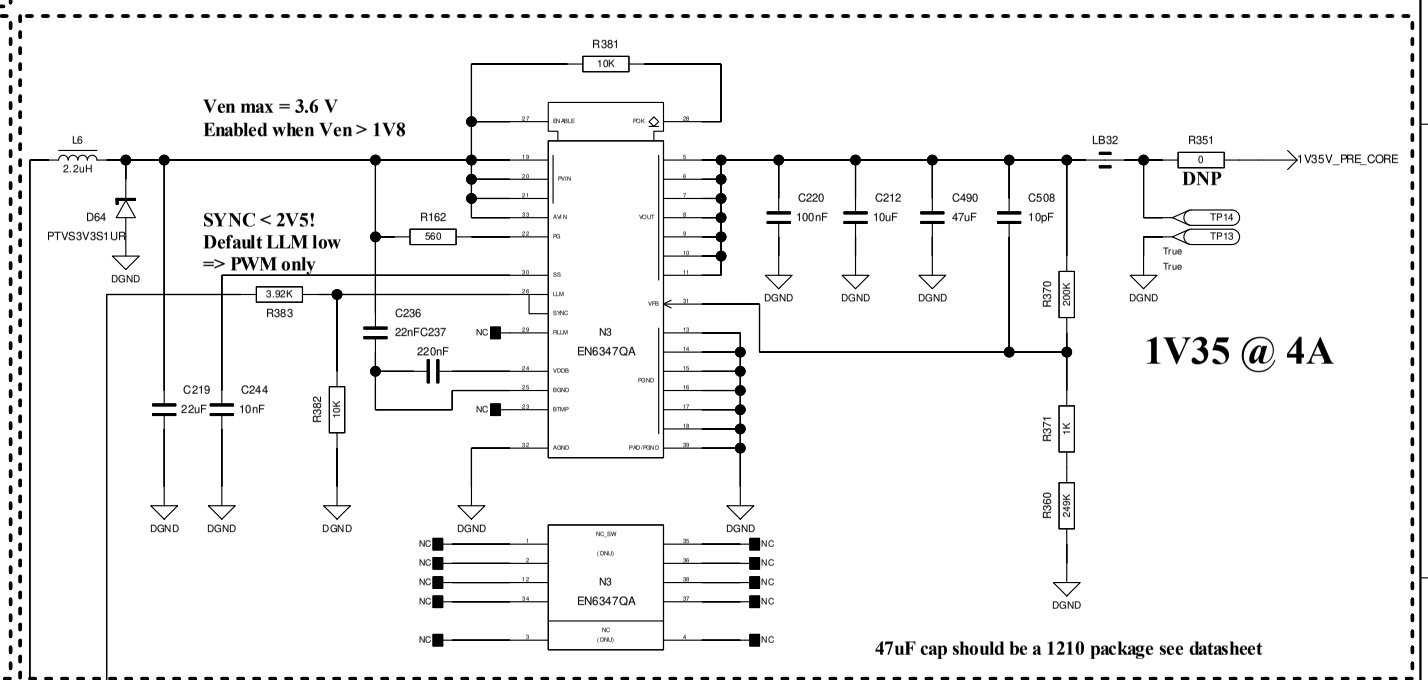

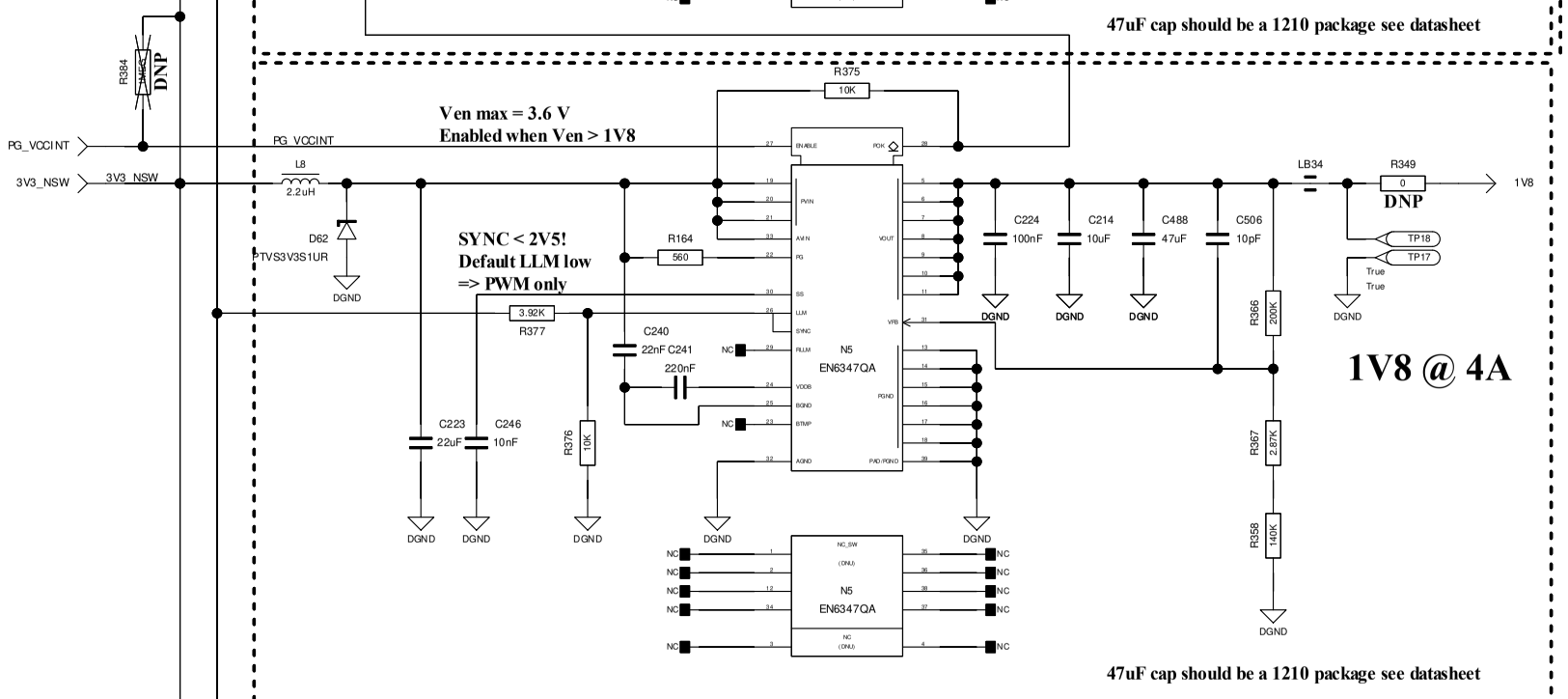

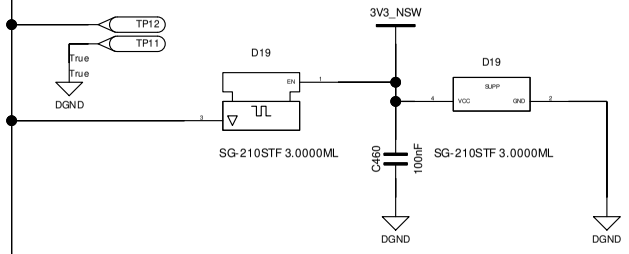

Power Sequence:

1V0 VCCINT/VCCBRAM (due to 1V35 Pre_Core)
1V8 VCCAUX, 1V0 MGTAVCC, 1V2 MGTAVTT, VCCO (Bank 35)
1V35 VCCO_DDR (Bank 33, 34, 502)
2V5 VCCO (Bank 12, 13, 501)
3V3 VCCO (Bank 0, 500)

rev.	by	notes

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Project : WRITE
Sheetname : SPEC7_SUB_SMPS

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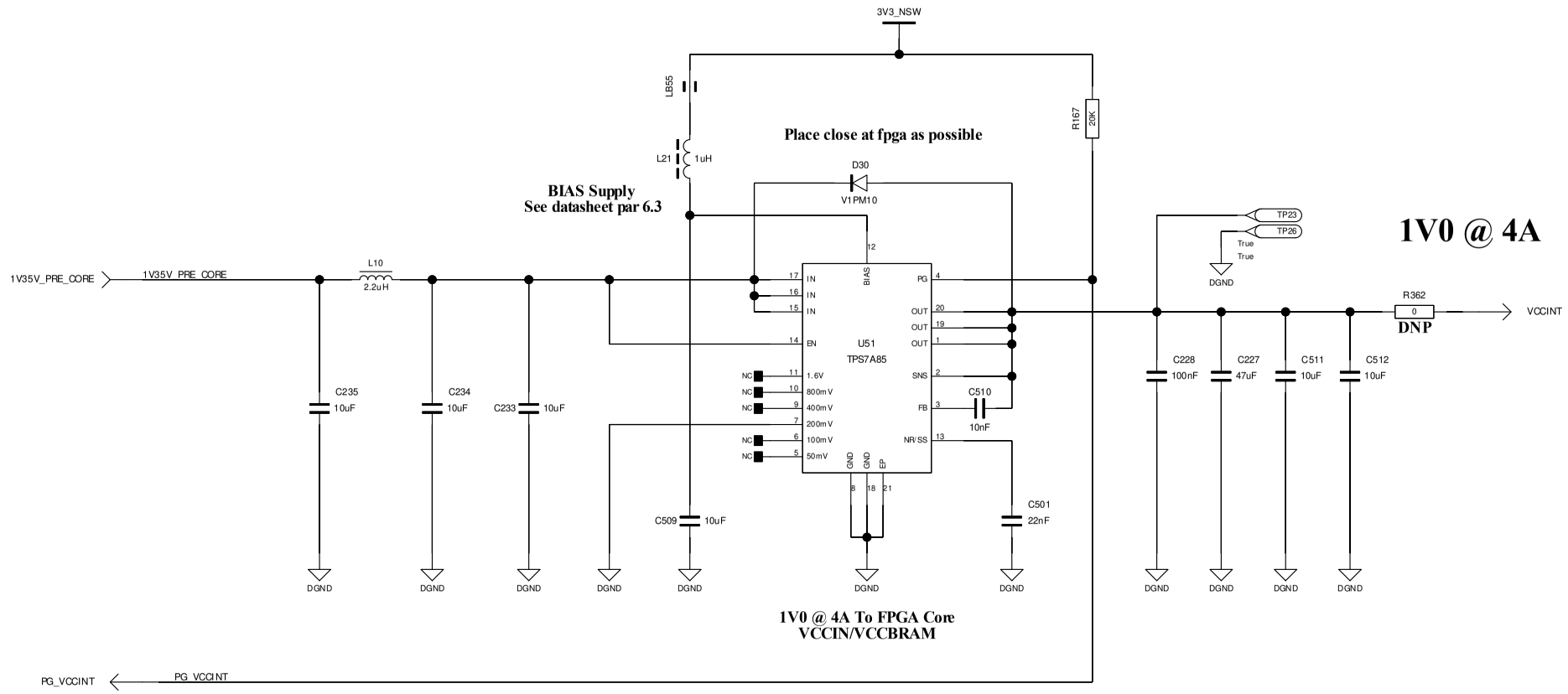

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Project : WRITE

Sheetname : SPEC7_VCCINT_POWER

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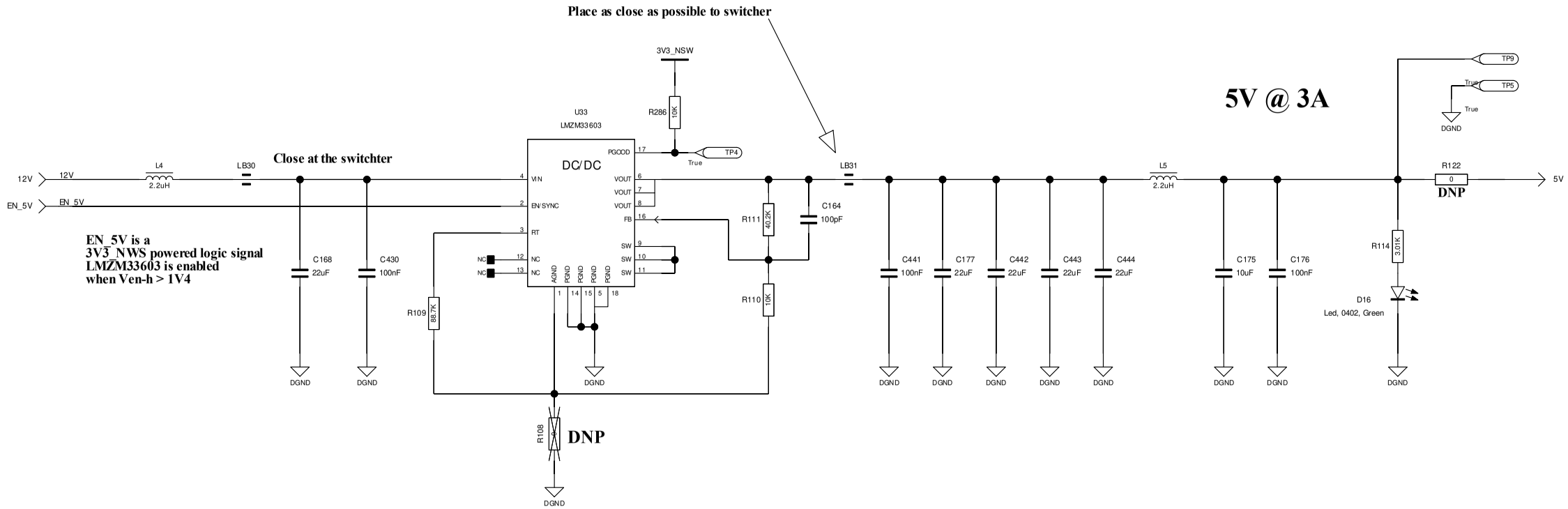

LMZM33603 datasheet Table 1:
Vin = 12V, Vout = 5V
RT = 88.7 K (fsw=450 Khz)
Rfbt = 40.2 K
Cff = 100 pF
66 uF < Cout <200 uF

rev.	by	notes

SPEC7 v2 crystek Powered

Project : WRITE

Sheetname : SPEC7_12V_To_5V_3A

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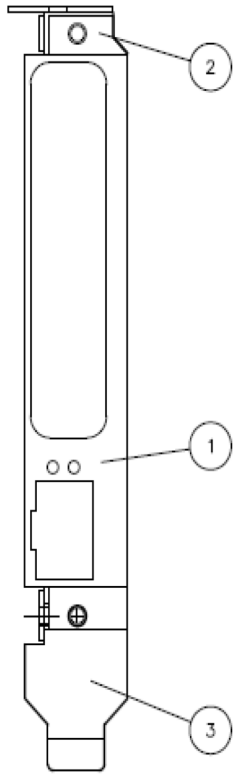
Mechanical Parts



1	NC	MP13	3200-0478	Frontpanel for SPEC Card
2	NC	MP14	3200-0476LC	Steel Bracket for SPEC Card, Up
3	NC	MP15	3200-0477LC	Steel Bracket for SPEC Card, Down
	NC	MP16	BN-330-1123238	M2.5-6 Screw, Slotted Cheese Head, Zinc Coated Steel, Passivated
	NC	MP17	BN-330-1123238	M2.5-6 Screw, Slotted Cheese Head, Zinc Coated Steel, Passivated
	NC	MP18	BN-330-1123238	M2.5-6 Screw, Slotted Cheese Head, Zinc Coated Steel, Passivated
	NC	MP19	BN-330-1123238	M2.5-6 Screw, Slotted Cheese Head, Zinc Coated Steel, Passivated
	NC	MP20	11300.01.01.2	SPEC7 v2 PCB, PCIe, 14Layers
	NC	MP11	AAVID 342943	FPGA Heatsink

Shielding for PL WR VCXO's

MP5	S1711-46R	RFI Shield Clip, Midi	
MP8	S1711-46R	RFI Shield Clip, Midi	
MP1	S1711-46R	RFI Shield Clip, Midi	
MP4	S1711-46R	RFI Shield Clip, Midi	
MP9	S1711-46R	RFI Shield Clip, Midi	
MP12	S1711-46R	RFI Shield Clip, Midi	
MP3	S1711-46R	RFI Shield Clip, Midi	
MP2	S1711-46R	RFI Shield Clip, Midi	
MP7	S1711-46R	RFI Shield Clip, Midi	
MP10	S1711-46R	RFI Shield Clip, Midi	
MP6	1500-35-50-10-TS0.20	Clip-On EMI Shielding Can, 35x50mm, Height=10mm	

DGND

NC	MP21	UB5U3-700	DC Fan, 30x30x3mm, 5V/0.35A, 9500RPM
NC	MP22	M1.7x? Pan Head Screw	
NC	MP23	M1.7x? Pan Head Screw	
NC	MP24	M1.7x? Pan Head Screw	
NC	MP25	M1.7 Washer	
NC	MP26	M1.7 Washer	
NC	MP27	M1.7 Washer	
NC	MP28	M1.7 Nut	
NC	MP29	M1.7 Nut	
NC	MP30	M1.7 Nut	

rev.	by	notes

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Project : WRITE

Sheetname : SPEC7_Mechanical_Parts

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