TimIQ-CPU

Project

Beamlines synchronization system
Laser IQ modulator

TimIQ – CPU and FPGA board

Schematics

Description

This is the CPU board of the IQ modulator project.
It contains the CPU interface and the FPGA to
control the RF board.

Revision

Rev 0.1 – Jun 20, 2016 : Prototype
Rev 1.0 – September 20, 2016 :
  * P. 11 : changed fixation size from 2.8 mm to 3.1 mm
Rev 1.1 – April 19, 2017
  * P. 5 : added comment for additional wire connection between BBB and the FPGA

Designed by	Jean-Paul Ricaud	June 20, 2016
Checked by		
Approved by		

Sheet: TOP

File: top.sch

Jean-Paul Ricaud
TimIQ
–
Cover Sheet

Sheet: /
File: TimIQ-CPU_sch.sch

Title: TimIQ-CPU

Size: A3	Date: 2017-04-20	**Rev: 1.1**
KiCad E.D.A. eeschema 4.0.2-stable		Id: 1/11

Digital Interface to CPU Board

Sheet: Reset
/RST_FPGA
/BBB_RST
/CF_FPGA
/PROG_B_FPGA
/BBB_SYS_RESETn
File: reset.sch

Sheet: FPGA configuration
/CF_FPGA
/PROG_B_FPGA
EEPROM_CS
EEPROM_IO0
EEPROM_IO2
EEPROM_IO3
File: FPGA_config.sch

Sheet: BeagleBone connectors
/BBB_SYS_RESETn
BBB_CLKOUT2
BBB_I2C1_SCL
BBB_I2C1_SDA
BBB_I2C2_SCL
BBB_I2C2_SDA
BBB_SPI1_CS0
BBB_SPI1_CLK
BBB_SPI1_D0
BBB_SPI1_D1
BBB_UART1_TxD
BBB_UART1_RxD
File: BeagleBone.sch

Sheet: Ethernet PHY
PHY_TXD0
PHY_TXD1
PHY_TXD2
PHY_TXD3
PHY_TXD4
PHY_TXD5
PHY_TXD6
PHY_TXD7
PHY_TXEN
PHY_TXCLK
PHY_GTXCLK
PHY_TXER
PHY_RXD0
PHY_RXD1
PHY_RXD2
PHY_RXD3
PHY_RXD4
PHY_RXD5
PHY_RXD6
PHY_RXD7
PHY_RXDV
PHY_RXER
PHY_RXCLK
PHY_COL
PHY_CRS
PHY_MDC
PHY_MDIO
PHY_INT
/PHY_RST
PHY_HPD
PHY
File: Ethernet_PHY.sch

Sheet: input
inTTL0
outTTL0
File: input.sch

Sheet: outputs
inTTL1
inTTL2
inTTL3
inTTL4
outTTL1
outTTL2
outTTL3
outTTL4
File: outputs.sch

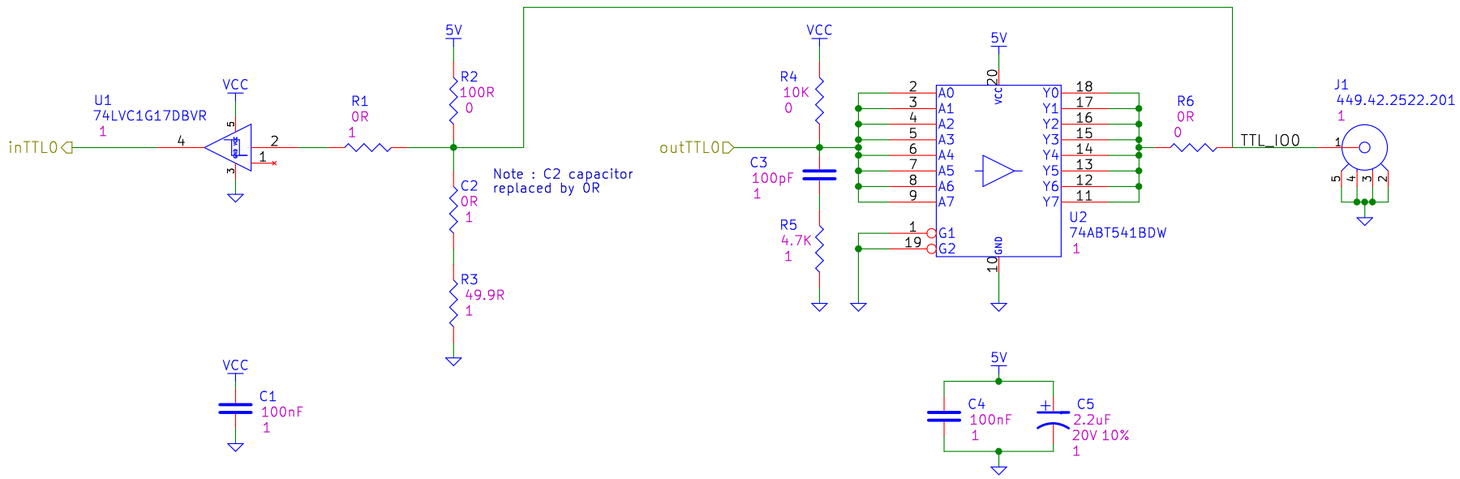
Sheet: Spartan6 FPGA
/RST_FPGA
/BBB_RST
EEPROM_CS
EEPROM_IO0
EEPROM_IO2
EEPROM_IO3
BBB_CLKOUT2
BBB_I2C1_SCL
BBB_I2C1_SDA
BBB_I2C2_SCL
BBB_I2C2_SDA
BBB_SPI1_CS0
BBB_SPI1_CLK
BBB_SPI1_D0
BBB_SPI1_D1
BBB_UART1_TxD
BBB_UART1_RxD
PHY_TXD0
PHY_TXD1
PHY_TXD2
PHY_TXD3
PHY_TXD4
PHY_TXD5
PHY_TXD6
PHY_TXD7
PHY_TXEN
PHY_TXCLK
PHY_GTXCLK
PHY_TXER
PHY_RXD0
PHY_RXD1
PHY_RXD2
PHY_RXD3
PHY_RXD4
PHY_RXD5
PHY_RXD6
PHY_RXD7
PHY_RXDV
PHY_RXER
PHY_RXCLK
PHY_COL
PHY_CRS
PHY_MDC
PHY_MDIO
PHY_INT
/PHY_RST
PHY_HPD
inTTL0
outTTL0
inTTL1
inTTL2
inTTL3
inTTL4
outTTL1
outTTL2
outTTL3
outTTL4
FPGA
File: fpga.sch

Sheet: Digital interface
/ADC_RST
/ADC_CS
ADC_SCK
ADC_MOSI
ADC_MISO
ADC_ALARM
ADC_ENA
ADC_ENB
/DAC_CS
DAC_SCK
DAC_MOSI
DAC_MISO
DAC_ENA
DAC_ENB
DAC_ENC
DAC_END
PLL_CE
PLL_CLK
PLL_DATA
PLL_LE
PLL_ENout
PLL_LOCKED
PLL_ENA
PLL_ENB
PLL_ENC
PLL_END
FD0_BYP
FD0_N0
FD0_N1
FD1_BYP
FD1_N0
FD1_N1
FD2_BYP
FD2_DIV1
FD_ENA
FD_ENB
FD_ENC
FD_END
SPARE0
SPARE1
SPARE2
SPARE3
SPARE4
SPARE5
SPARE6
SPARE7
RS485_R
/RS485_RE
RS485_D
RS485_DE
File: digital.sch

Sheet: PSU
Power Supplies
File: PSU.sch

Jean-Paul Ricaud	
TimIQ	
-	
-	
Sheet: /TOP/	
File: top.sch	
Title: TimIQ-CPU	
Size: A3	Date: 2017-04-20
KiCad E.D.A. eeschema 4.0.2-stable	Id: 2/11

Rev: 1.1



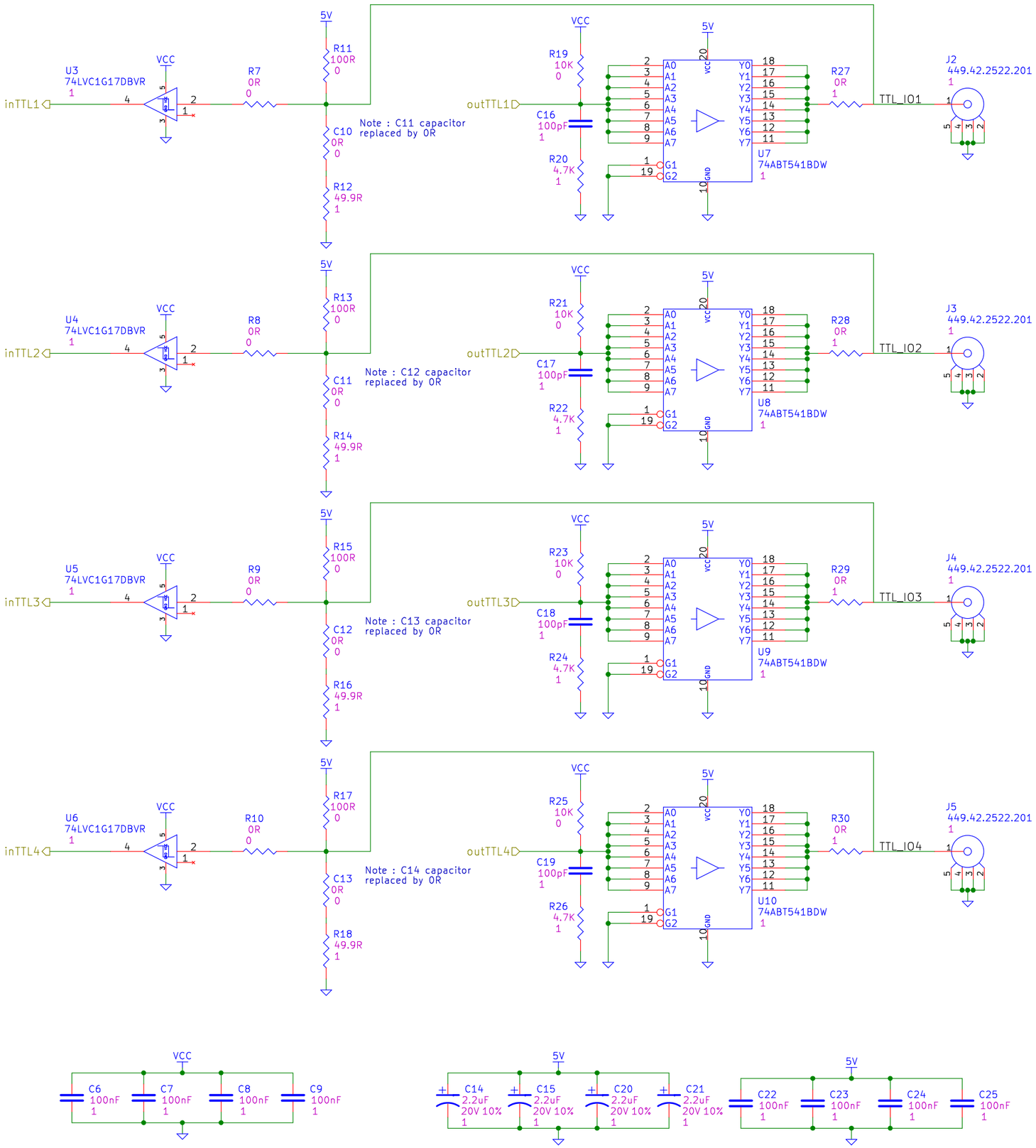
Jean-Paul Ricaud
TimIQ

Default TTL input

Sheet: /TOP/input/
File: input.sch

Title: TimIQ-CPU

Size: A3	Date: 2017-04-20	**Rev: 1.1**
KiCad E.D.A. eeschema 4.0.2-stable		Id: 3/11



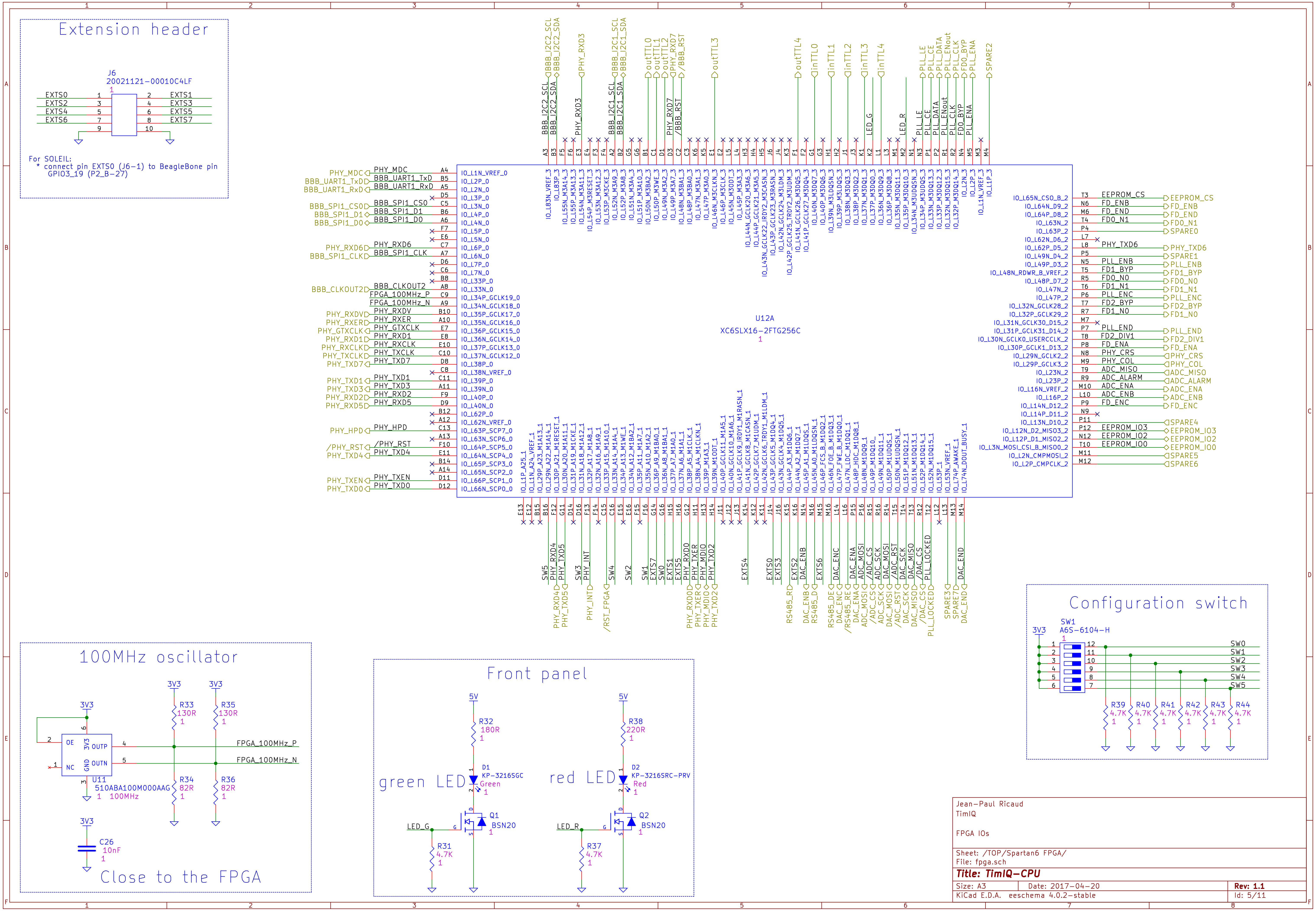
Jean-Paul Ricaud
TimIQ

Outputs

Sheet: /TOP/outputs/
File: outputs.sch

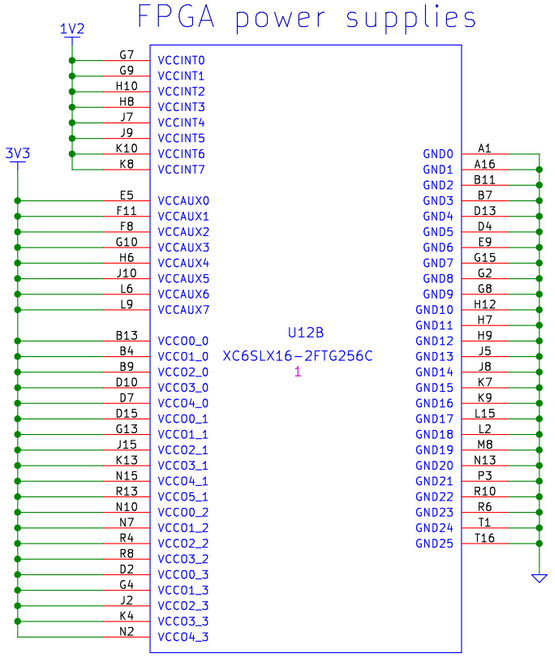
Title: TimIQ-CPU

Size: A3	Date: 2017-04-20	**Rev: 1.1**
KiCad E.D.A. eeschema 4.0.2-stable		Id: 4/11

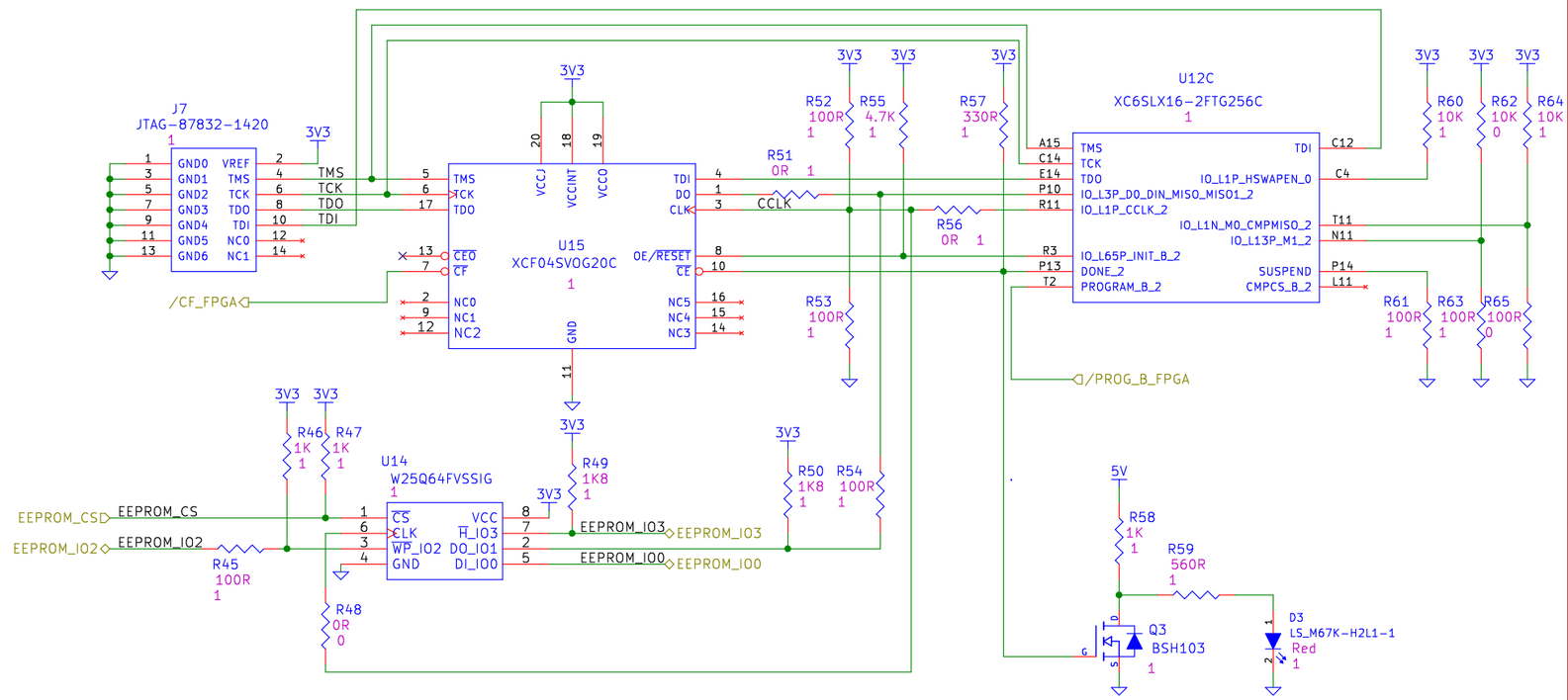


Extension header
J6
20021121-00010C4LF
EXTS0
EXTS1
EXTS2
EXTS3
EXTS4
EXTS5
EXTS6
EXTS7
For SOLEIL:
* connect pin EXTS0 (J6-1) to BeagleBone pin GPIO3_19 (P2_B-27)
U12A
XC6SLX16-2FTG256C
100MHz oscillator
U11
510ABA100M000AAG
100MHz
FPGA_100MHz_P
FPGA_100MHz_N
C26
10nF
Close to the FPGA
Front panel
green LED
red LED
D1
KP-3216SGC
Green
D2
KP-3216SRC-PRV
Red
Q1
BSN20
Q2
BSN20
LED_G
LED_R
Configuration switch
SW1
A6S-6104-H
SW0
SW1
SW2
SW3
SW4
SW5
Jean-Paul Ricaud
TimIQ
FPGA IOs
Sheet: /TOP/Spartan6 FPGA/
File: fpga.sch
Title: TimIQ-CPU
Size: A3
Date: 2017-04-20
Rev: 1.1
KiCad E.D.A. eeschema 4.0.2-stable
Id: 5/11

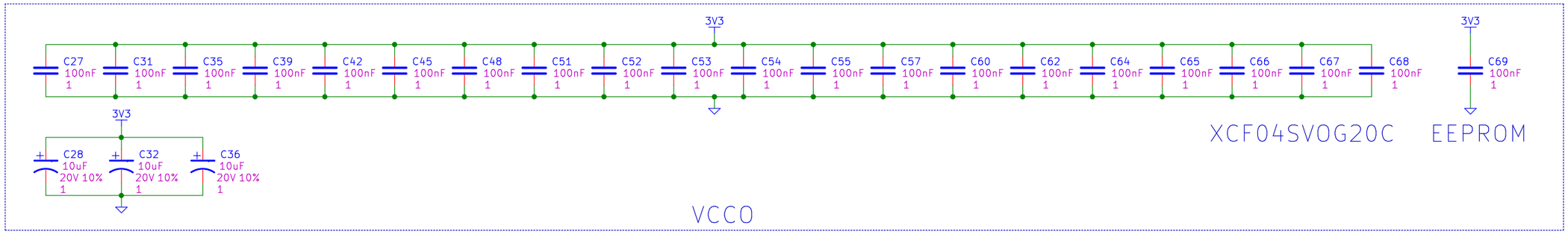
FPGA power supplies

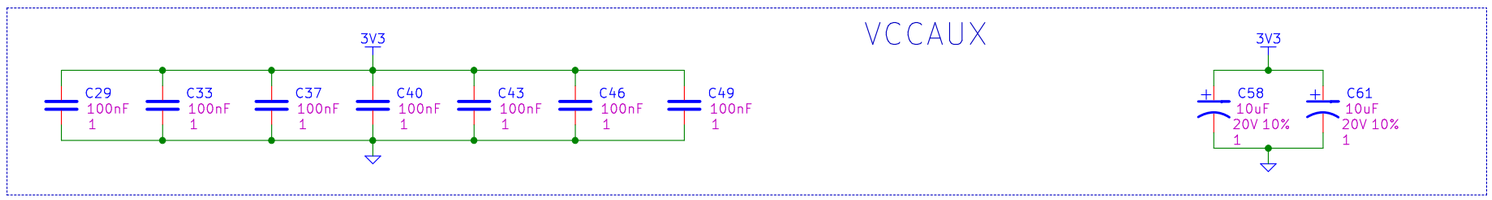


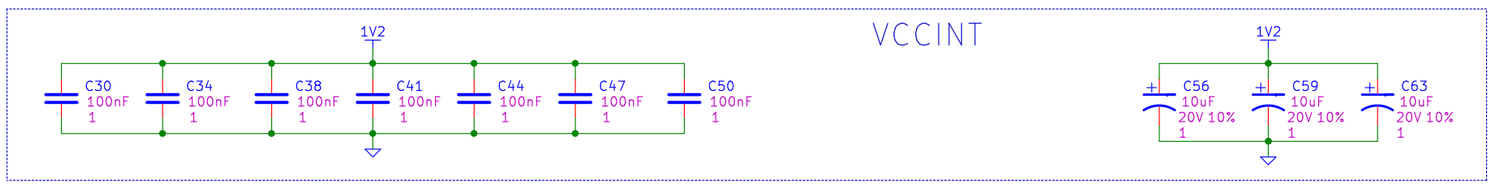
FPGA configuration – Master Serial Mode



FPGA power supplies decoupling







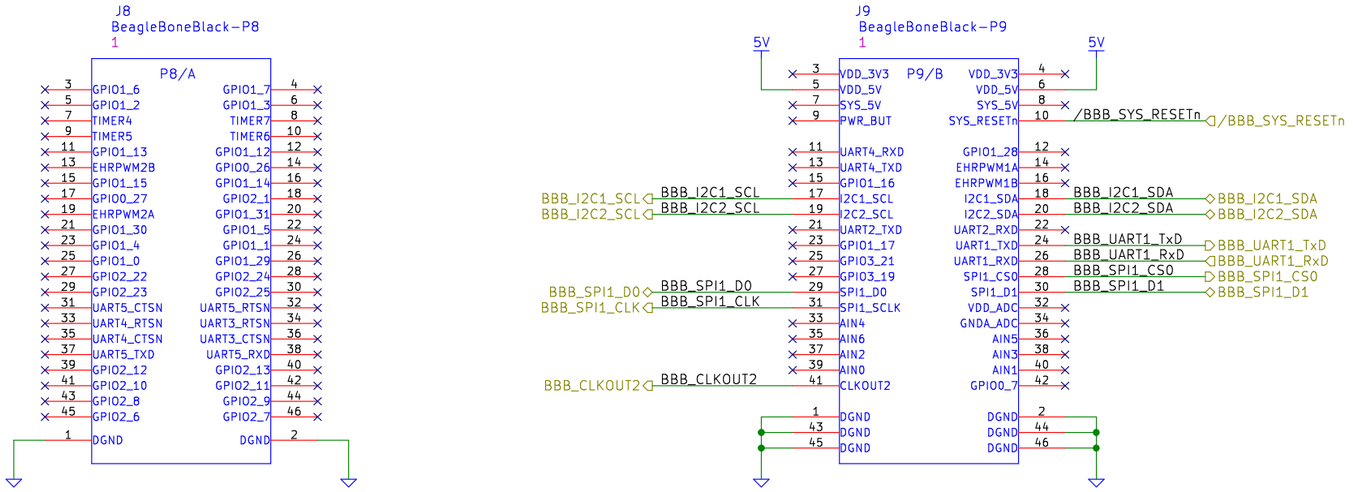
Jean-Paul Ricaud
TimIQ

FPGA config and power supply

Sheet: /TOP/FPGA configuration/
File: FPGA_config.sch

Title: TimIQ-CPU

Size: A3	Date: 2017-04-20	**Rev: 1.1**
KiCad E.D.A. eeschema 4.0.2-stable		Id: 6/11



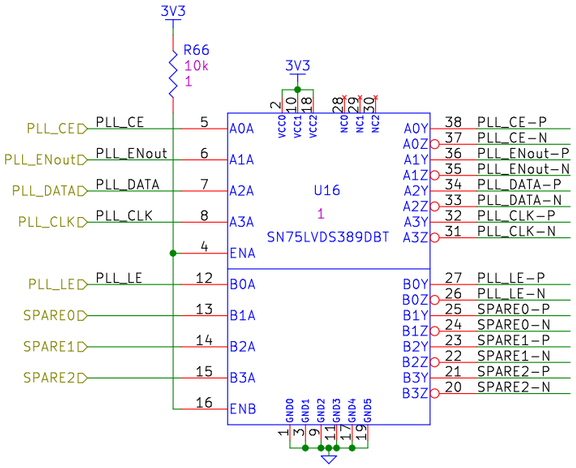
Jean-Paul Ricaud
TimIQ

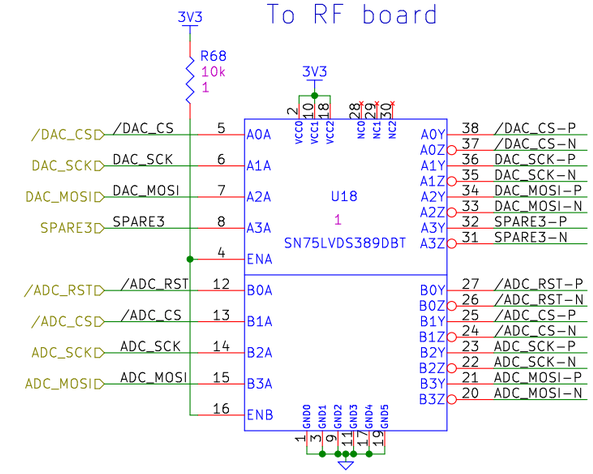
BeagleBone connectors

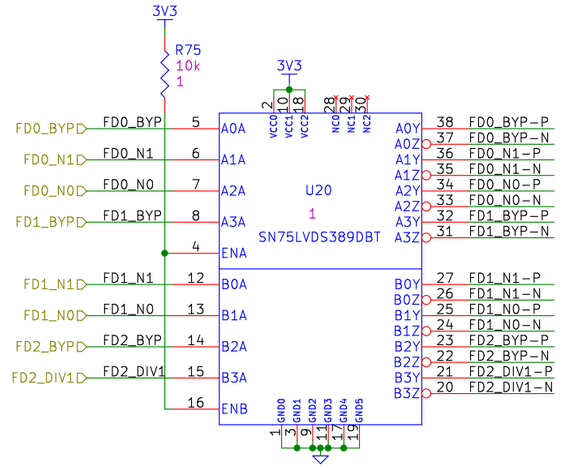
Sheet: /TOP/BeagleBone connectors/
File: BeagleBone.sch

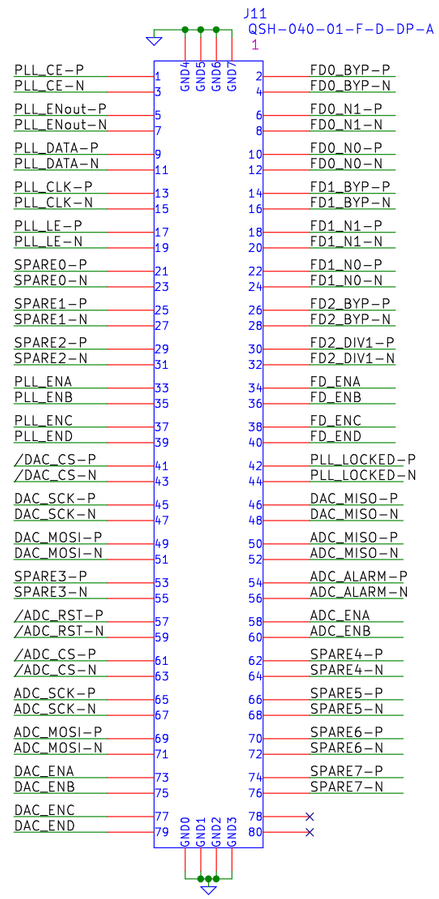
Title: TimIQ-CPU

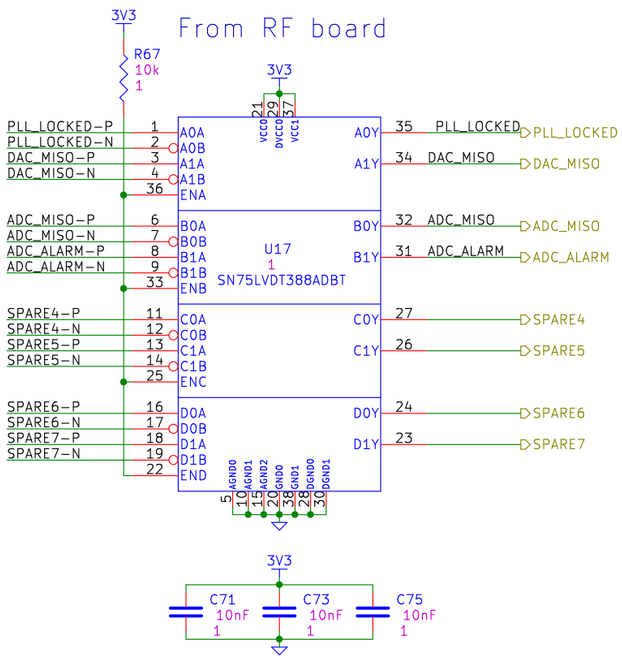
Size: A3	Date: 2017-04-20	**Rev: 1.1**
KiCad E.D.A. eeschema 4.0.2-stable		Id: 7/11

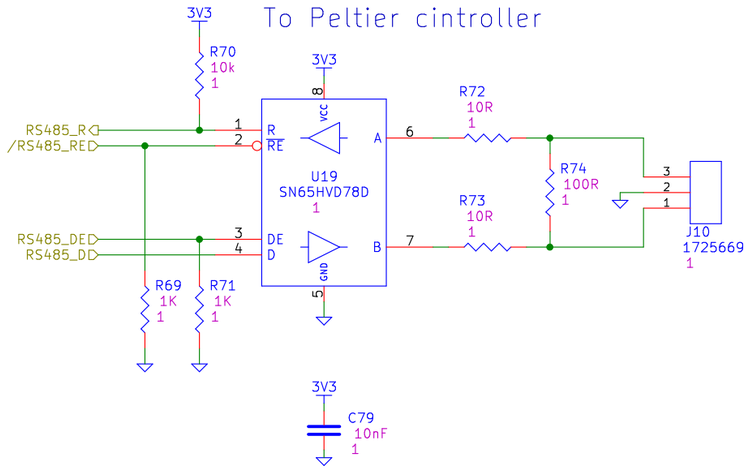


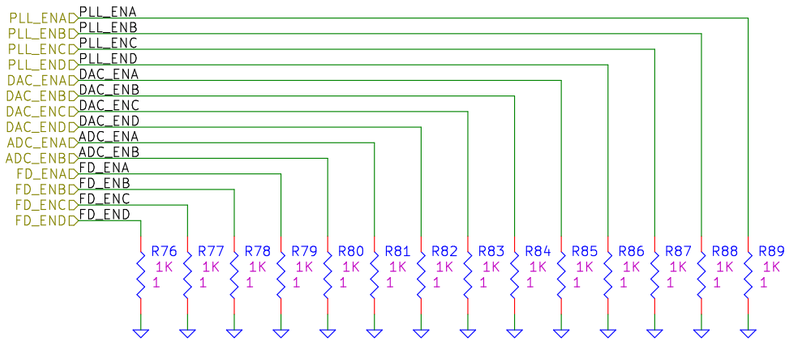










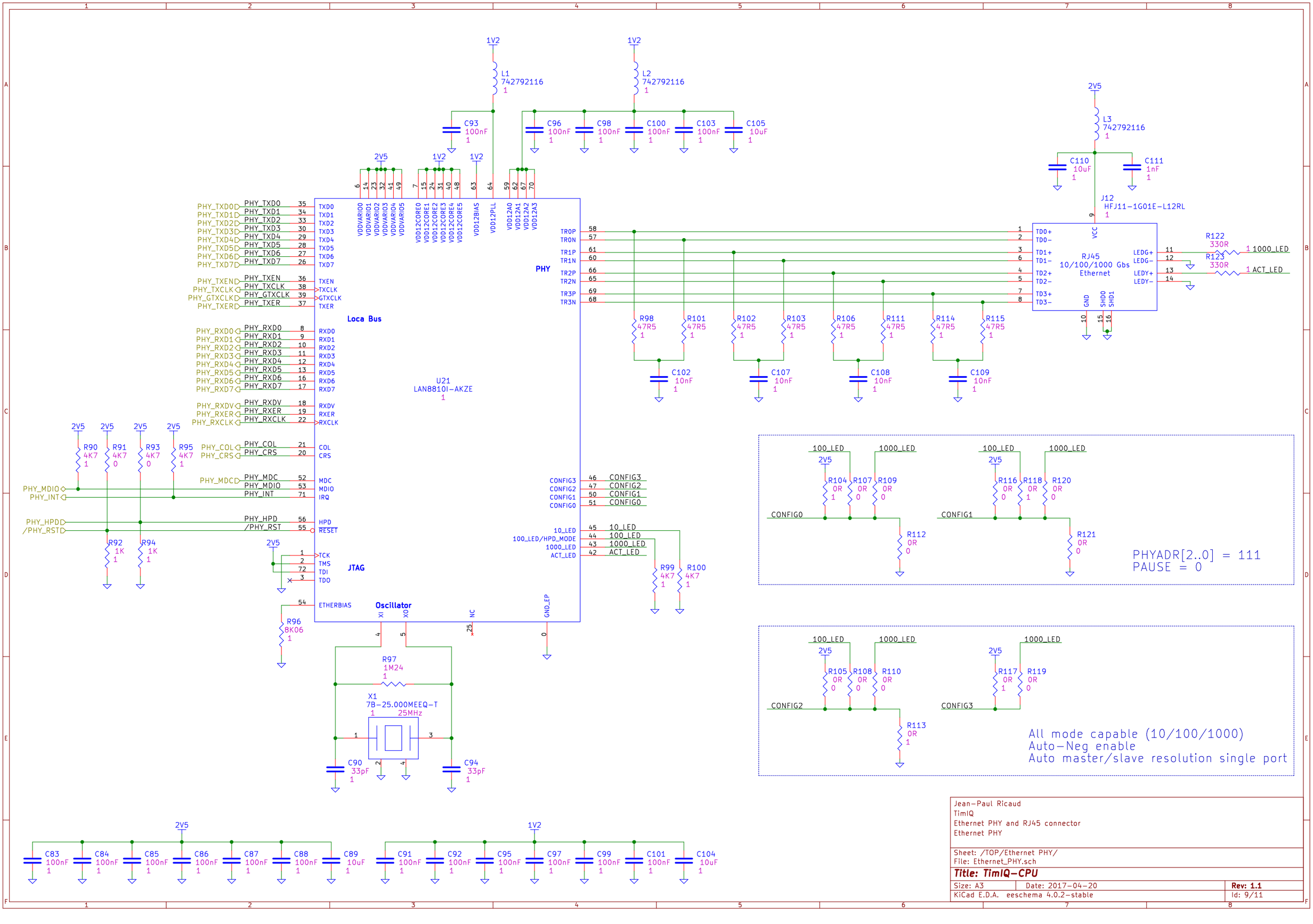


Jean-Paul Ricaud
TimIQ
the DAC and the ADC
digital interface of the PLL,

Sheet: /TOP/Digital interface/
File: digital.sch

Title: TimIQ-CPU

Size: A3	Date: 2017-04-20	**Rev: 1.1**
KiCad E.D.A. eeschema 4.0.2-stable		Id: 8/11



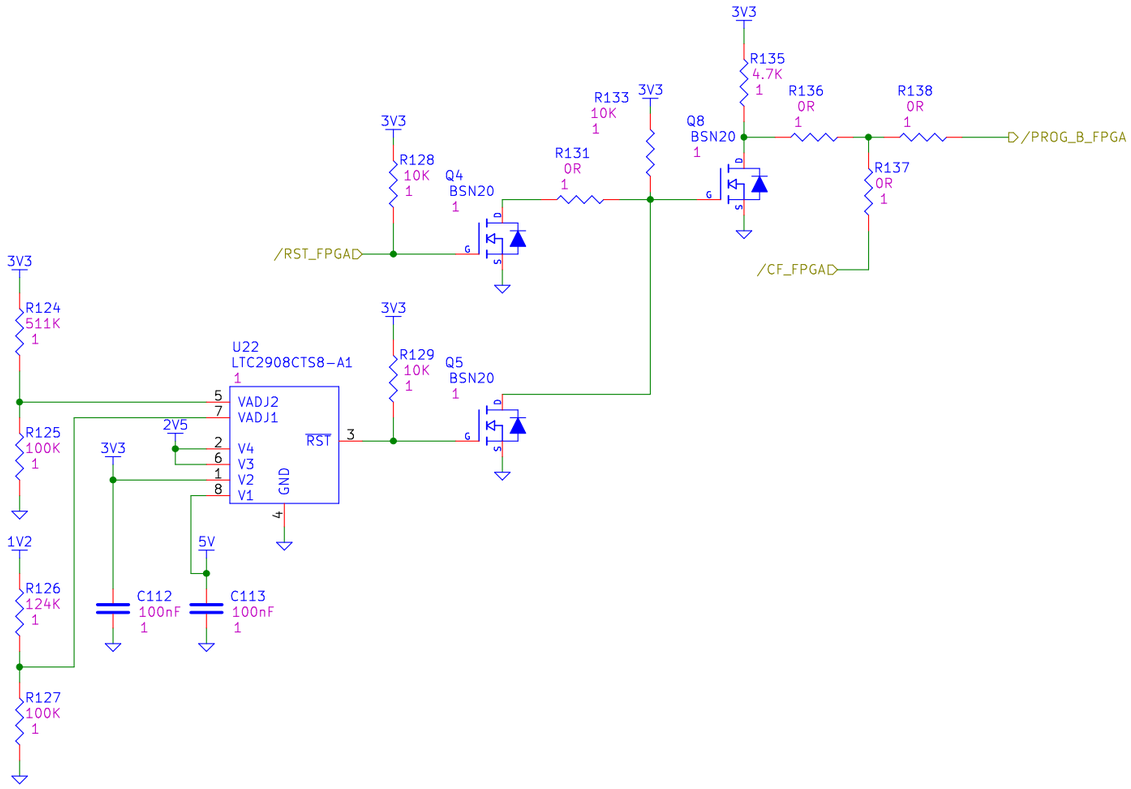
Jean-Paul Ricaud
TimIQ
Ethernet PHY and RJ45 connector
Ethernet PHY

Sheet: /TOP/Ethernet PHY/
File: Ethernet_PHY.sch

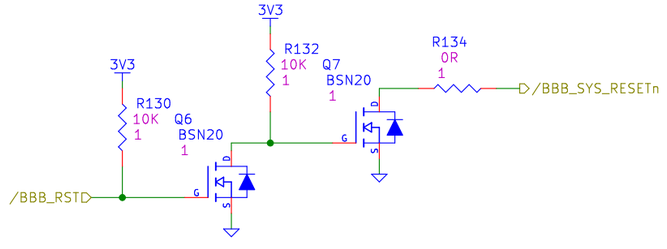
Title: TimIQ-CPU

Size: A3	Date: 2017-04-20	**Rev: 1.1**
KiCad E.D.A. eeschema 4.0.2-stable		Id: 9/11

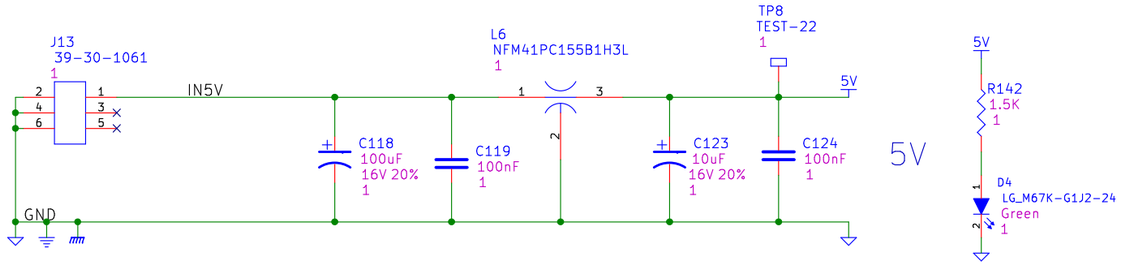
Power monitor & FPGA reset



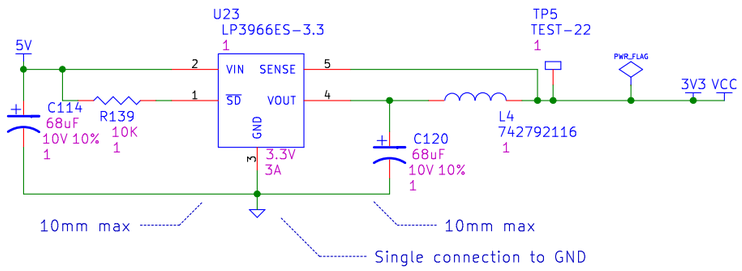
BeagleBone reset



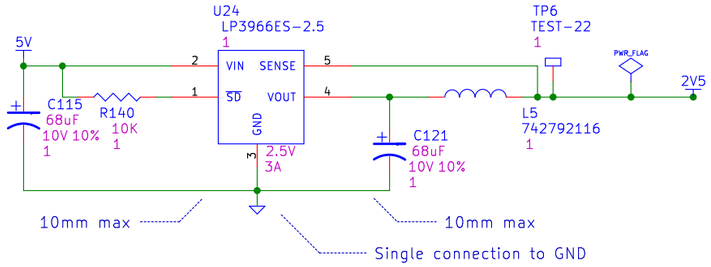
Jean-Paul Ricaud TimIQ Reset & power monitor		
Sheet: /TOP/Reset/ File: reset.sch		
Title: TimIQ-CPU		
Size: A3	Date: 2017-04-20	**Rev: 1.1**
KiCad E.D.A. eeschema 4.0.2-stable		Id: 10/11



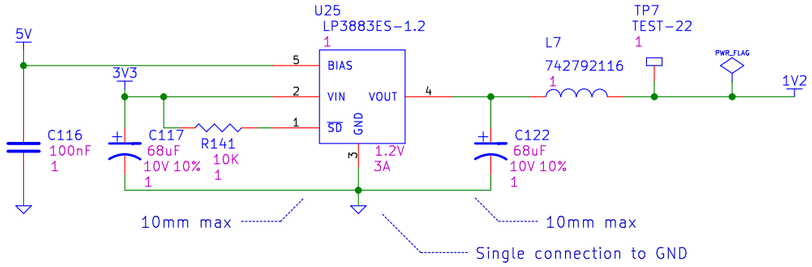
5V



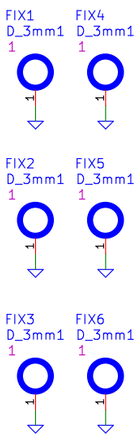
3.3V

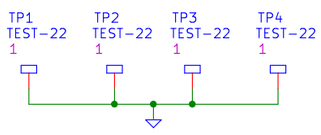


2.5V



1.2V





Jean-Paul Ricaud TimIQ PSU		
Sheet: /TOP/PSU/ File: PSU.sch		
Title: TimIQ-CPU		
Size: A3	Date: 2017-04-20	**Rev: 1.1**
KiCad E.D.A. eeschema 4.0.2-stable		Id: 11/11