FAIR Timing Receiver AMC form factor - CSL_FTRN_AMC

Single width, mid-height

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3	Power Tree
4	POWER DC-DC
5	POWER LDOs, FPGA BYPASS
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14	AMC BACKPLANE PLUG
15	Backplane buffers - MTCA.4 TCLK A-D, Libera B triggers
16	Backplane buffers - MTCA.4 PORTs 17-20
17	Backplane buffers - MTCA.4 PORTs 12-15

DATE	REVISION DESCRIPTION	DRAWN	REV
01.09.2014	Initial version	dslavinec	A
19.09.2014	Flattened IO blocks	dslavinec	A
02.12.2014	Updates after QA review	dslavinec	A
16.04.2015	Added ADC clock generation and trigger signals to backplane, moved LVTTL_CLK, nRES and FPGA_RES to different FPGA pins	dslavinec	A
23.07.2015	removed ADC clocking page, only one set of triggers to backplane kept, incorporated changes from PMC (LED driving), added power mux for MMC	dslavinec	A
17.08.2015	added sheet 15 with MTCA.4 triggers and clocks to/from backplane	dslavinec	A
01.10.2015	MTCA.4 out clocks not connected to clk outputs, backplane buffers enable signals connected only to FPGA	dslavinec	A
27.11.2015	MTCA.4 connections to backplane finished, MMC PGOOD modified, relevant updates from PMC, MMC reset modified	dslavinec	A
09.12.2015	MTCA.4 HSS connections (backplane ports 12-15) moved from FPGA GXB banks to LVDS IOs	dslavinec	A
16.12.2015	libera triggers, MTCA.4 tclk and mlvdios moved to top FPGA banks	dslavinec	A
16.06.2016	LTM4620 replaced with LTM4619, FPGA core voltage increased to 1.15V, different TCLK buffers, larger LED resistors, replaced IO TVS	dslavinec	A

Value	Capatitors used
12p	0402, 50V, C0G, 1%
22p	0402, 50V, C0G, 1%
10n	0402, 25V, X7R, 10%
100n	0402, 25V, X7R, 10%
1u	0603, 16V, X7R, 10%
2.2u	1210, 100V, X7R, 10%
10u	1210, 25V, X7R, 10%
22u	1210, 10V, X7R, 10%
100u	1210, 10V, X5R, 20%

All resistors are SMD 0402, 63mW, 1% except where marked differently.

Components marked DNP (Do Not Place) are foreseen for testing purposes and should NOT be placed.

TOP layer

FM1 FIDUCIAL FM2 FIDUCIAL FM3 FIDUCIAL

BOTTOM layer

FM4 FIDUCIAL FM5 FIDUCIAL FM6 FIDUCIAL

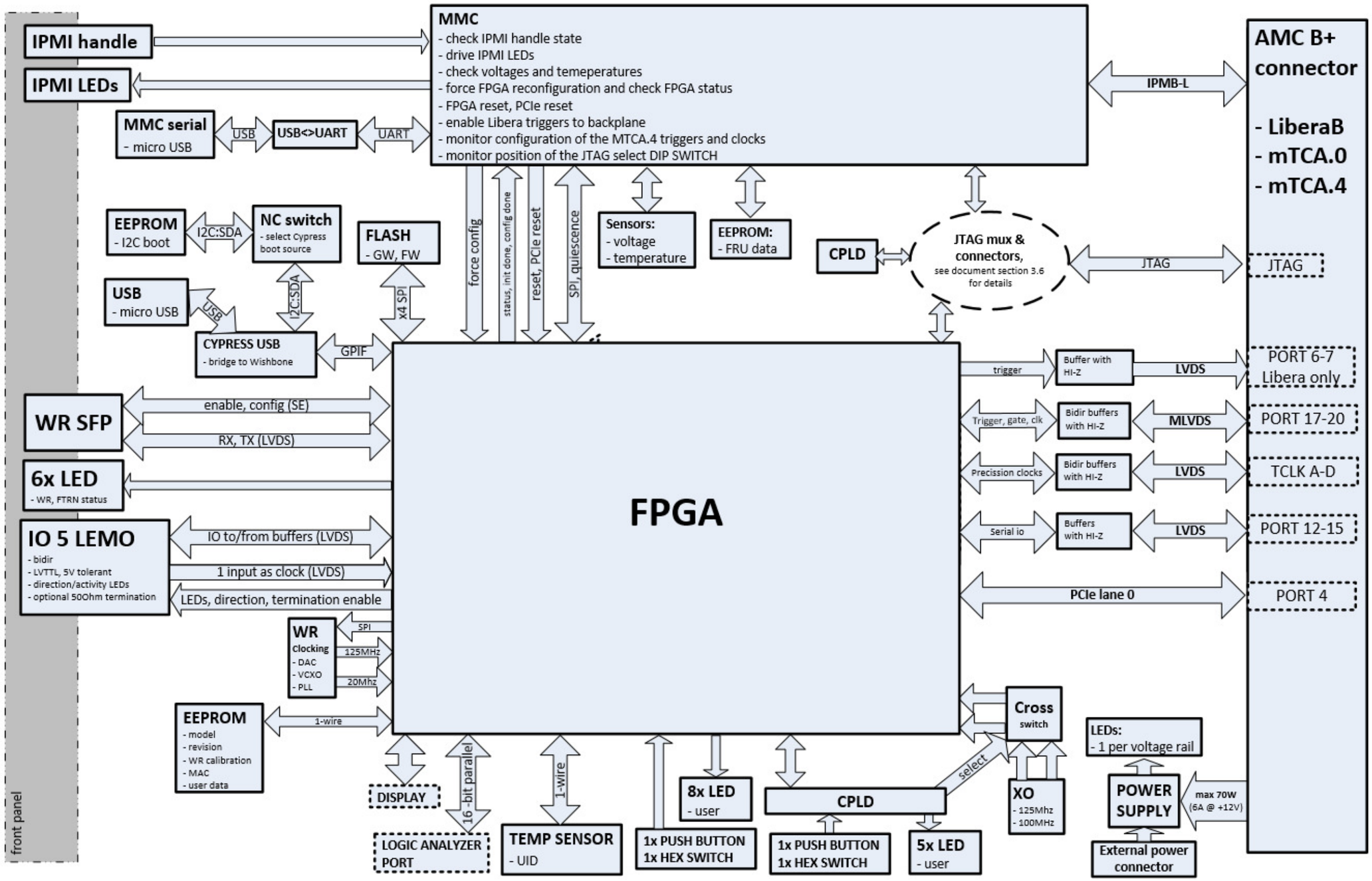
DRAWN	Dušan Slavinec		01.09.2014
CHECKED	-		
APPROVED	-		

Title

Size A3 | Type SE | DWG.NO. CSL_FTRN_AMC | REV. A

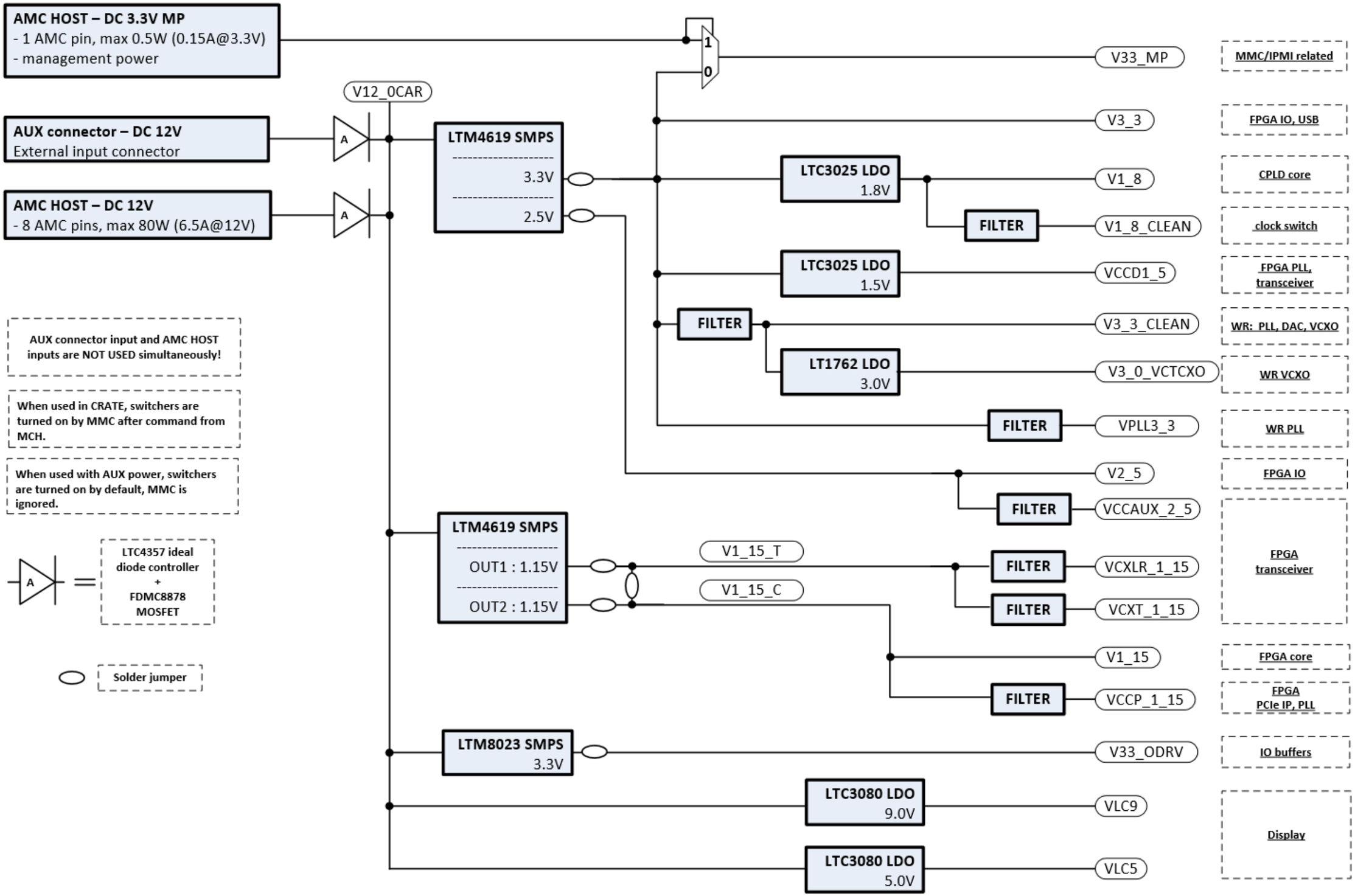
SHEET 1 OF 17

Block Diagram - FTRN, MMC



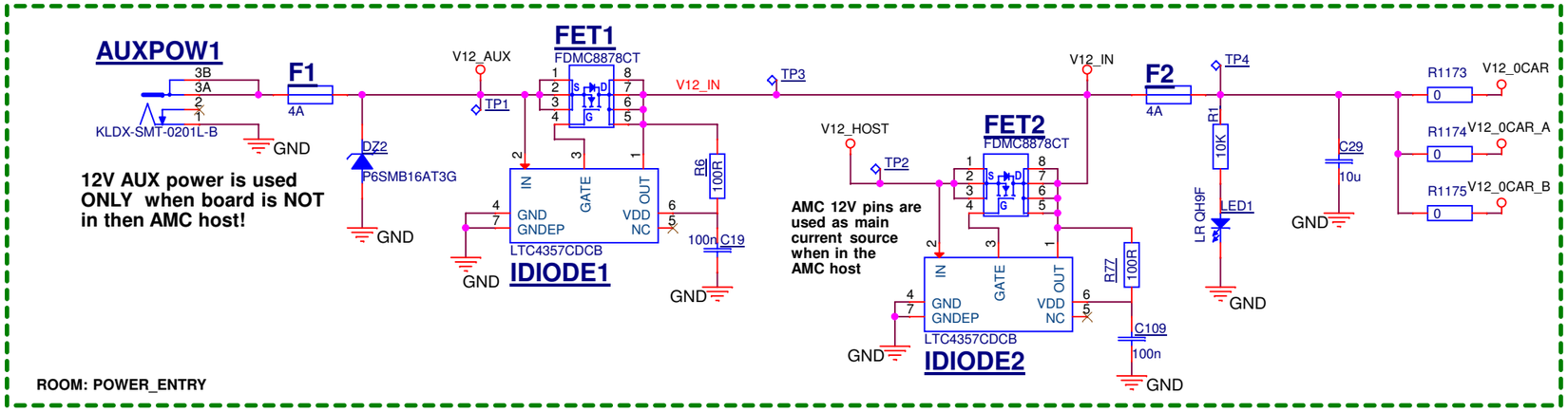
Title: Block Diagram - FTRN, MMC			
Size: A3	Type: SE	DWG.NO. CSL_FTRN_AMC	REV. A
			SHEET 2 OF 17

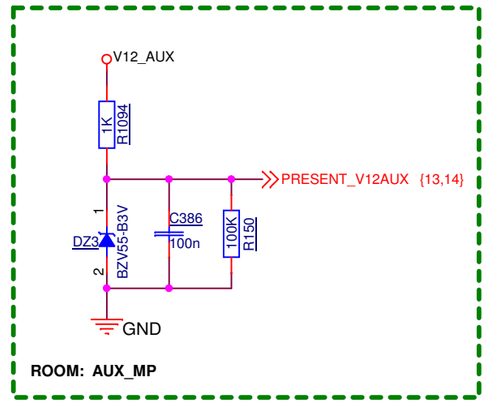
Power tree block scheme



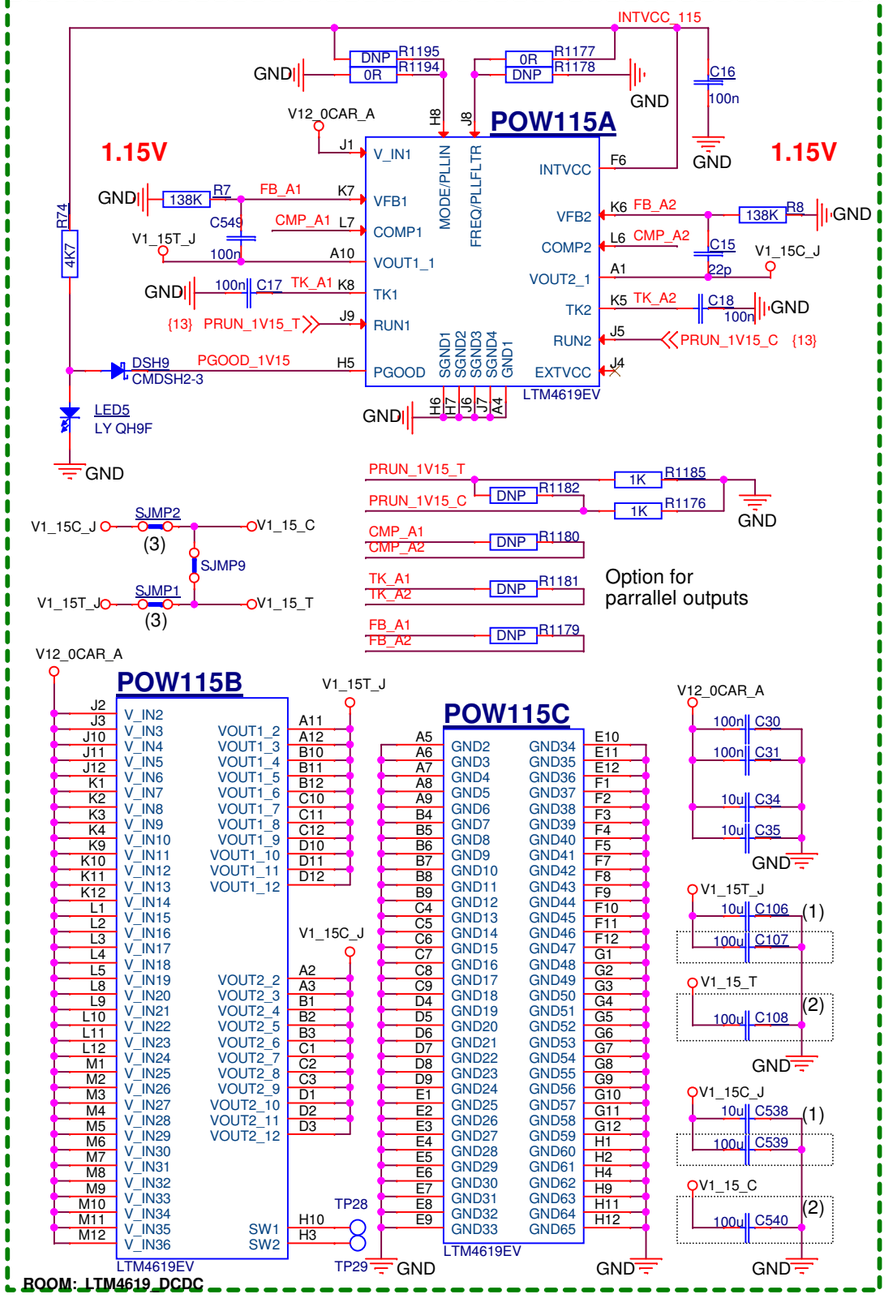
Title	Power tree block scheme		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
			SHEET 3 OF 17

Power entry and main DCDC power regulators

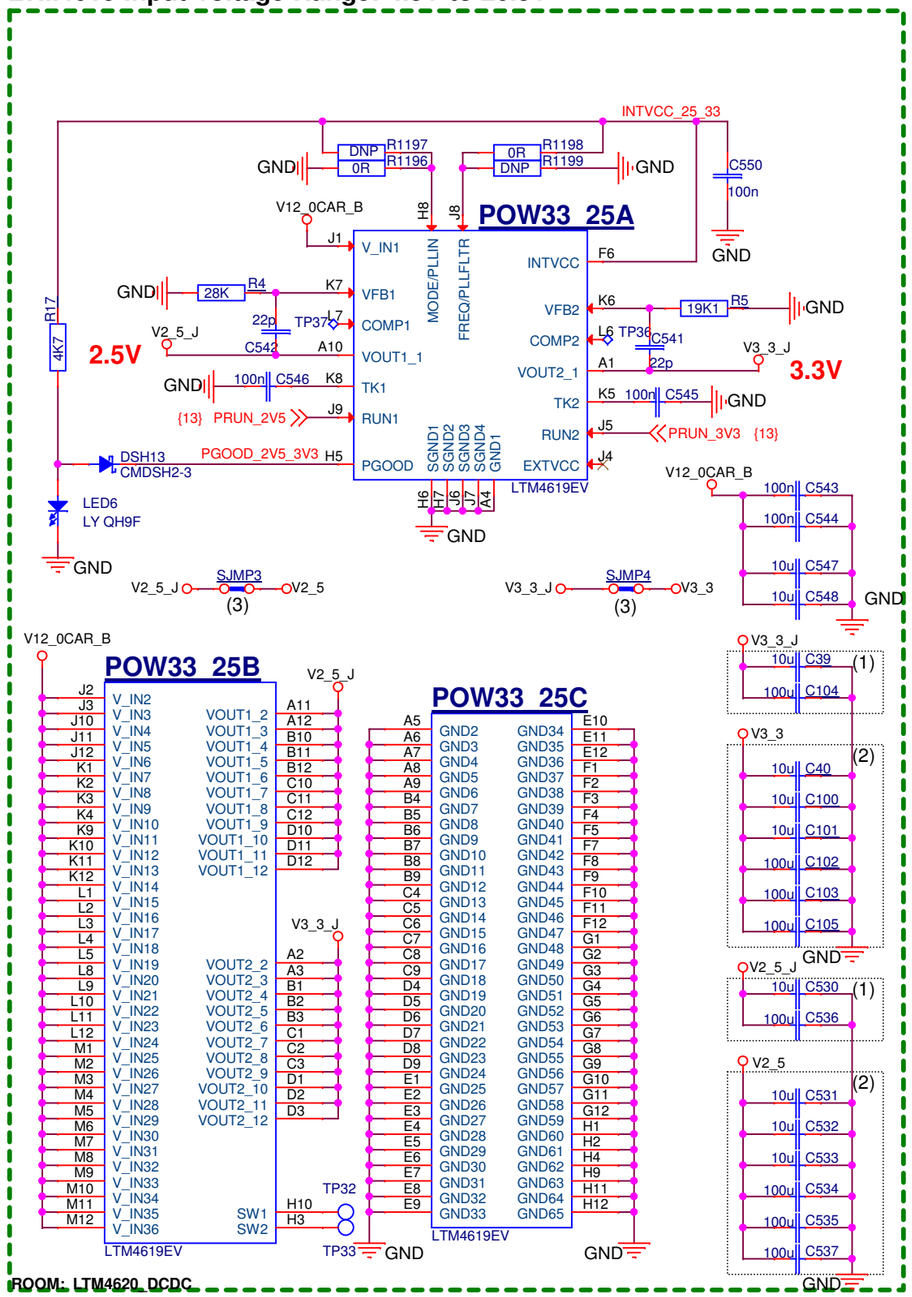


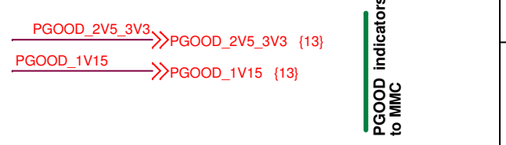


LTM4619 input Voltage Range: 4.5V to 26.5V



LTM4619 input Voltage Range: 4.5V to 26.5V





(2) - place capacitors away from the regulator outputs

(3) - 0R solder jumper, to test power regulator outputs before powering FPGA

Title: Power entry and main DCDC power regulators			
Size: A3	Type: SE	DWG.NO. CSL_FTRN_AMC	REV. A
		SHEET 4 OF 17	

FPGA decoupling, LDO regulators, power indicators

LOG1R

5AGXMA3D4F27I3N

LOG1P

5AGXMA3D4F27I3N

LOG1Q

5AGXMA3D4F27I3N

IMPORTANT! (LOG1Q)
In the PCB layout, the traces from FPGA pins D26 and AE1 to the R11 and R12 resistors need to be routed so that they avoid any aggressor signals.
R11 and R12 must be 1% or better!

IMPORTANT!
Separate VCC and VCCP planes into two different power layers on the PCB!

VCC 1.15V

ROOM: CAPS_VCC_1_1

VCCP 1.15V

ROOM: CAPS_VCCP_1

VCCT_GXB

VCCR_GXB VCCL_GXB

ROOM: CAPS_VCC_GX_1_15

VCCD_FPLL VCCH_GXBL VCCBAT

ROOM: CAPS_VCC_1_5

VCCIO 2.5V

ROOM: CAPS_VCC_2_5

VCCPD 2.5V

VCCAUX 2.5V VCCA_FPLL VCCA_GXB

ROOM: CAPS_VCCAUX_2_5

VCCIO 3.3V

ROOM: CAPS_VCCIO_3_3

VCCPD 3.3V

ROOM: CAPS_VCCPD_3_3

POWcpld18 — LDO 1.8V for CPLD, WR CLOCK SWITCH

LTC3025EDC

POW_1_5 — LDO 1.5V for VCCH_GXB VCCD_FPLL, VCC_BAT

LTC3025EDC

ROOM: POWER_LDO

POWVLC5 — LDO 5.0V for LCD

LT3080EDD

POWVLC9 — LDO 9.0V for LCD

LT3080EDD

ROOM: POWER_LCD_LDO

IND1 / IND2 / IND3 / IND4

BLM31PG121SN1L

ROOM: POWER_FILTERS

LED_5 / LED_33 / LED_18 / LED_115 / LED_11 / LED_15

LR QH9F, MMBT3904

ROOM: POWER_INDICATORS

(1) - 0R solder connection, to test regulator outputs before connecting to load

Title	FPGA decoupling, LDO regulators, power indicators
Size	A3
Type	SE
DWG.NO.	CSL_FTRN_AMC
REV.	A
SHEET	5 OF 17

FPGA and CPLD JTAG, FPGA gateware FLASH, User Flash

USB connector JTAG signals flow : C (connector) > R (resistor) > B (buffer) > P (PROG - CPLD) > F (FPGA) > B > C

JTAG connector
(on the front panel if possible)

JTAGCON1
S1 S2 S3 S4 S5 S6 — MICRO-B — ZX62-B-5PA(11)
GND

DTV1
TPD6E05U06RVZR
GND

VCC_TRGT — DSH1 CMDSH2-3 — V3_3

JTDI_CR — 100R R47 — JTDI_RB
JTMS_CR — 100R R48 — JTMS_RB
JTDO_RC — 100R R49 — JTDO_BR
JTCK_CR — 100R R51 — JTCK_RB

Straight-through Routing

Parallel to USB connector JTAG signals are JTAG signals from JSW1 swtich (JTAG from backplane)

JTCK_RB — JTCK_RB {14}
JTMS_RB — JTMS_RB {14}
JTDI_RB — JTDI_RB {14}
JTDO_FB — JTDO_FB {14}

JTAG buffer and protection

DRV1
SN74LVC125A
JTDI_RB → 1A 1OE → JTDI_BP
JTMS_RB → 2A 2OE → JTMS_B
JTDO_FB → 3A 3OE → JTDO_BR
JTCK_RB → 4A 4OE → JTCK_B
GND THP, VCC 14
GND — 100n C245 — V3_3

V3_3 — 10K R50 — JTMS_B
10K R53 — JTDI_BP
10K R54 — JTDO_FB
10K R55
GND — 10K R52 — JTCK_B

JTAG signal pull-ups

V3_3 — 10K R78 — JTDI_RB
10K R91 — JTMS_RB
GND — 10K R79 — JTCK_RB

ROOM: FPGA_CPLD_JTAG_INPUT

LOG1O
to/from SPIFLASHX4_1:
JTDO_PF AD24 — 3A_TDI
JTMS_B Y22 — 3A_TMS
JTCK_B AE24 — 3A_TCK
JTDO_FB AE26 — 3A_TDO
JTAG
SPI_SI_D0_FPGA AF24 — 3A_AS_DATA0_ASDO
SPI_SO_D1_FPGA AE25 — 3A_AS_DATA1
SPI_WP_D2_FPGA AF25 — 3A_AS_DATA2
SPI_HD_D3_FPGA AD25 — 3A_AS_DATA3
nSPI_CS_FPGA AD26 — 3A_nCSO_DATA4
SPI_CLK_FPGA AC23 — 3A_DCLK
CONFIG
set by PROG1:
MSEL0 A24 — 8A_MSEL0
MSEL1 K20 — 8A_MSEL1
MSEL2 A25 — 8A_MSEL2
MSEL3 B24 — 8A_MSEL3
MSEL4 B25 — 8A_MSEL4
CONF_DONE F22 — 8A_CONF_DONE
nCONFIG C24 — 8A_nCONFIG
nSTATUS J20 — 8A_nSTATUS
H22 — 8A_nCE
5AGXMA3D4F27I3N
GND

nCONFIG_PROG — #MMC_FPGA_CONFIG — 0R R193 — 0R R194 — nCONFIG

IC3
nCONFIG_PROG → IN0
{13} #MMC_FPGA_CONFIG → IN1
IN2
Y = IN0 AND IN2
Y → 4 nCONFIG
V3_3 → 5 VCC
GND → 2
SN74LVC1G97DCK
GND — 100n C322

FPGA status to MMC
CONF_DONE → CONF_DONE {13}

SPIFLASHX4_1
V3_3 — C248 100n — GND
VCC 8, EP 9, GND 4
SI/D0 5 SPI_SI_D0_FPGA
SO/D1 2 SPI_SO_D1_FPGA
WP/D2 3 SPI_WP_D2_FPGA
HD/D3 7 SPI_HD_D3_FPGA
CS 1 nSPI_CS_FPGA
CK 6 SPI_CLK_FPGA
N25Q256A13EF840

V3_3 — R143 10K DNP SPI_WP_D2_FPGA
R144 10K DNP SPI_HD_D3_FPGA

ROOM: MEMORY

{7} ROM_DATA → ROM_DATA — **1-wire**

ROM1
DS18B20U+
NC1 NC2 NC3 NC4 NC5
DQ 1 — ROM_DATA — R71 1K — V3_3
VDD 8
GND 4 — C254 100n — GND

ROM2
DS28EC20P
NC1 NC2 NC3 NC4
I/O 2 — ROM_DATA
GND 3 — GND

PROG1C
BANK 1 FB2 / BANK 2 FB1 / BANK 1 FB4 / BANK 2 FB3
XC2C64A-7CPG56C

nCONFIG_PROG G1
CONF_DONE F3
PGCLK H1
{7} HSWP_3 G3
{7} HSWP_4 J1
{8} OSCRFCK_SRC_SEL_0 K1
MSEL1 K2
K3
H3
K5
K6
{7} PLED5 H5
K7
H7
HSWP_1 K8
{7} PLED1 H10
{7} PLED2 G10
{7} PLED3 F10
{7} PLED4 E10

I/O22 F1 — MRES1
I/O23 E3
I/O24 E1 — MSEL0
I/O25 D1 — FPGA_RES
I/O26 C1 — MSEL2 — FPGA_RES {7}
I/O27 A3 — HSWP_2
I/O28 A2 — CON3 — HSWP_2 {7} CON3 {7}
I/O29 B1 — MSEL3
I/O30 A1 — MSEL4
I/O31 C3 — CONFIG_SPV
I/O32 C4 — nSTATUS — CRC_ERROR {10}
I/O33 A4
I/O34 C5
I/O35 A7 — OSCRFCK_SRC_SEL_1 {8}
I/O36 C8 — PBS_P
I/O37 A8 — CON1 — PBS_P {7} CON1 {7}
I/O38 A9 — CON5 — CON5 {7}
I/O39 A5 — CON4 — CON4 {7}
I/O40 A10 — CON2 — CON2 {7}
I/O41 B10
I/O42 C10
I/O43 D8
I/O44 E8
I/O45 D10

V3_3 — 10K R56 — CONF_DONE
10K R57 — CRC_ERROR
10K R58 — nSTATUS
10K R92 — nCONFIG
GND

XOF1
ECS-2033-500-BN
V3_3 — C271 100n — GND
VDD 4, GND 2, CLK 3 — PGCLK, OE 1 — V3_3

PROG1A
XC2C64A-7CPG56C
JTAG
JTDI_BP J10 — TDI
JTMS_B K9 — TMS
JTCK_B K10 — TCK
JTDO_PF A6 — TDO

V1_8 — 100n C59 — GND
PROG1B
XC2C64A-7CPG56C
G8 VCC
V3_3 — H6 VCCIO1
C6 VCCIO2
D3 V_AUX
GND1 C7
GND2 F8
GND3 H4
100n C60 — GND
100n C111 — GND
100n C112 — GND

ROOM: PROG_CPLD

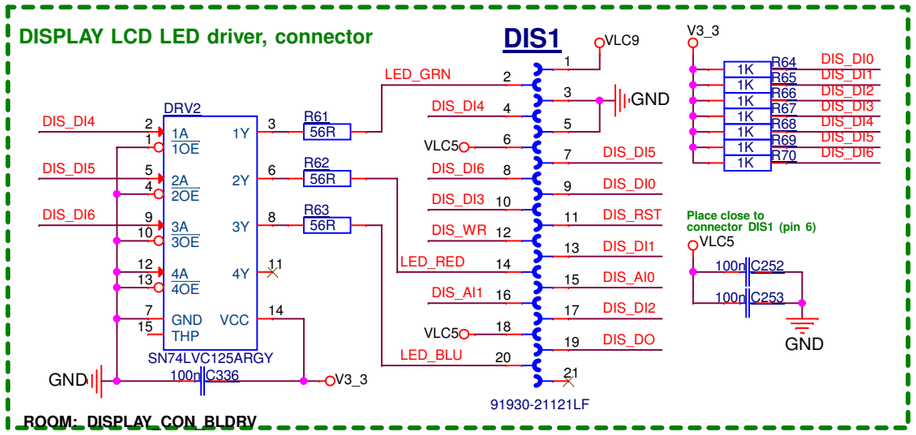
RST1 — **to PROG1C (pin F1)**
V3_3 — C244 100n — GND
VDD 5, GND 2
out RST 1 — CONFIG_SPV
in MR 3 — V3_3
WDI 4
TPS3823-33DBVT

RST2 — **to PROG1C (pin F1)**
V3_3 — C243 100n — GND
VDD 5, GND 2
out RST 1 — nRES — nRES {7}
in MR 3 — MRES1
WDI 4
TPS3823-33DBVT
from PROG1C (pin F1)

Title	FPGA and CPLD JTAG, FPGA gateware FLASH, User Flash		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
		SHEET 6 OF 17	

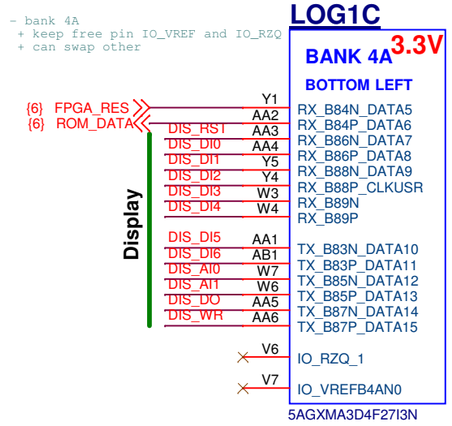
User interface - USB, Display, push buttons, HEX switch, LEDs

DISPLAY LCD LED driver, connector

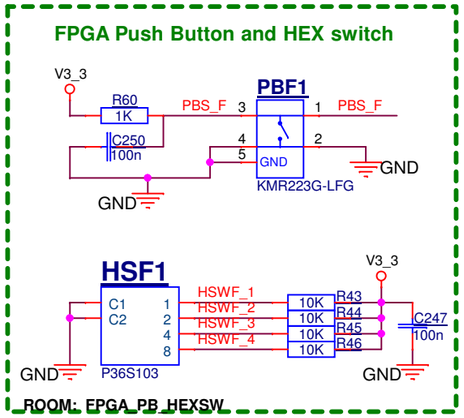


ROOM: DISPLAY_CON_BLDRV

LOG1C

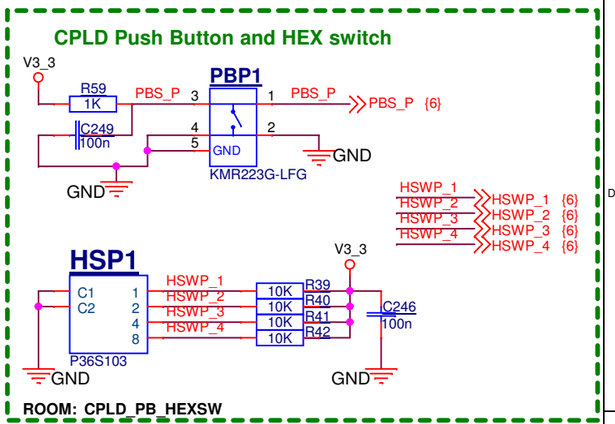


FPGA Push Button and HEX switch



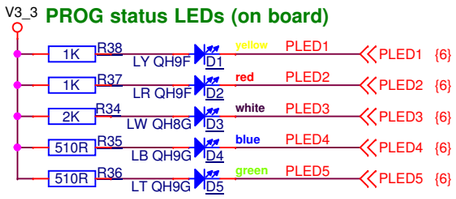
ROOM: FPGA_PB_HEXSW

CPLD Push Button and HEX switch



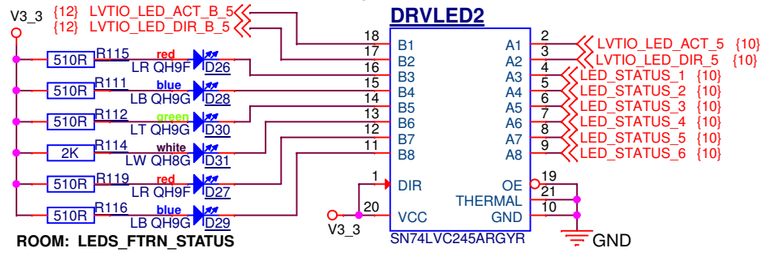
ROOM: CPLD_PB_HEXSW

PROG status LEDs (on board)



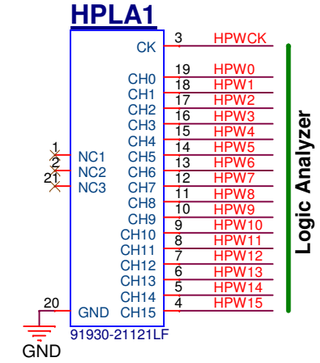
ROOM: LEDS_PROG_STATUS

WR / FTRN STATUS LEDs (on front panel from FPGA)

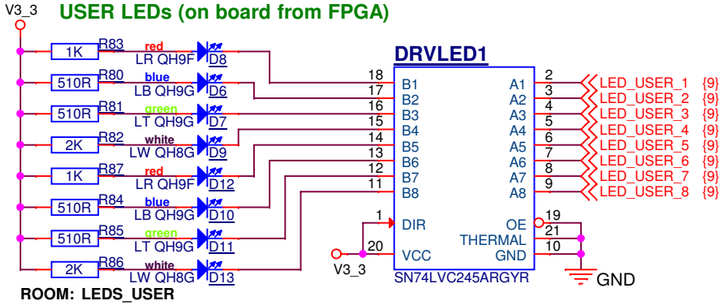


ROOM: LEDS_FTRN_STATUS

Logic analayzer connector

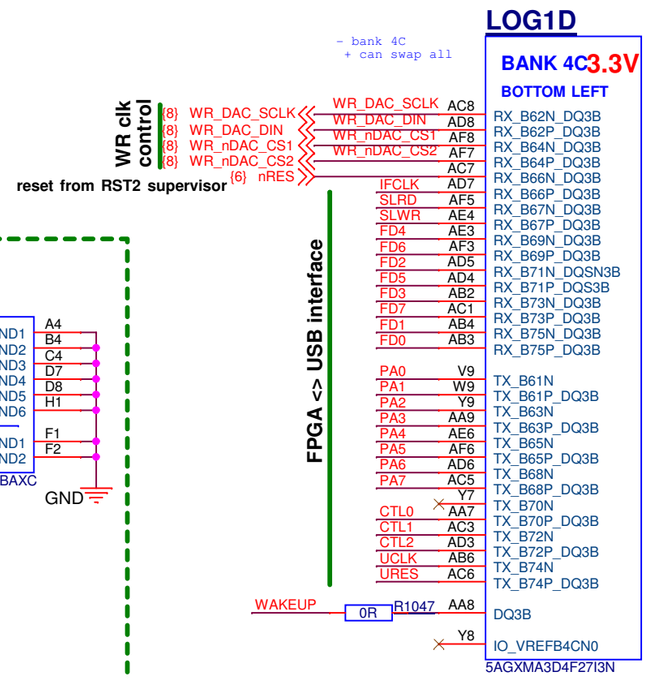


USER LEDs (on board from FPGA)

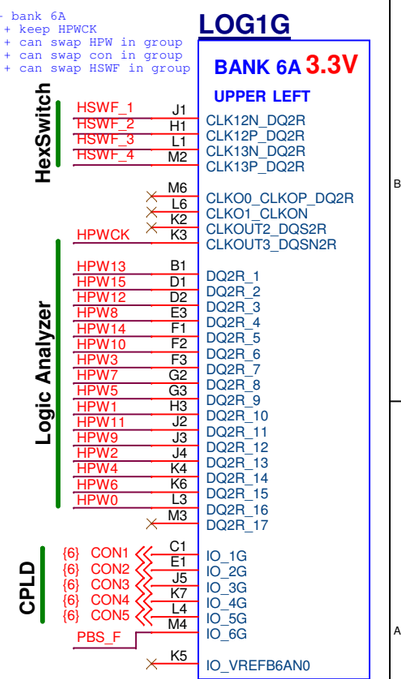


ROOM: LEDS_USER

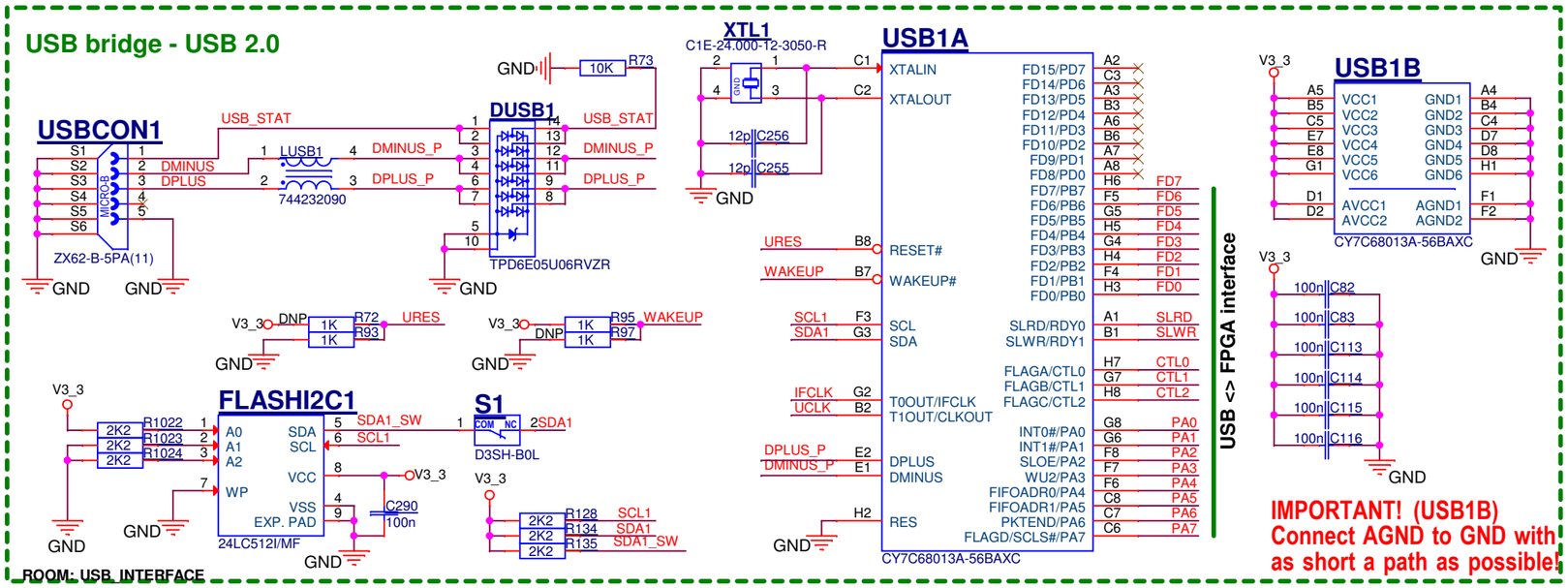
LOG1D



LOG1G



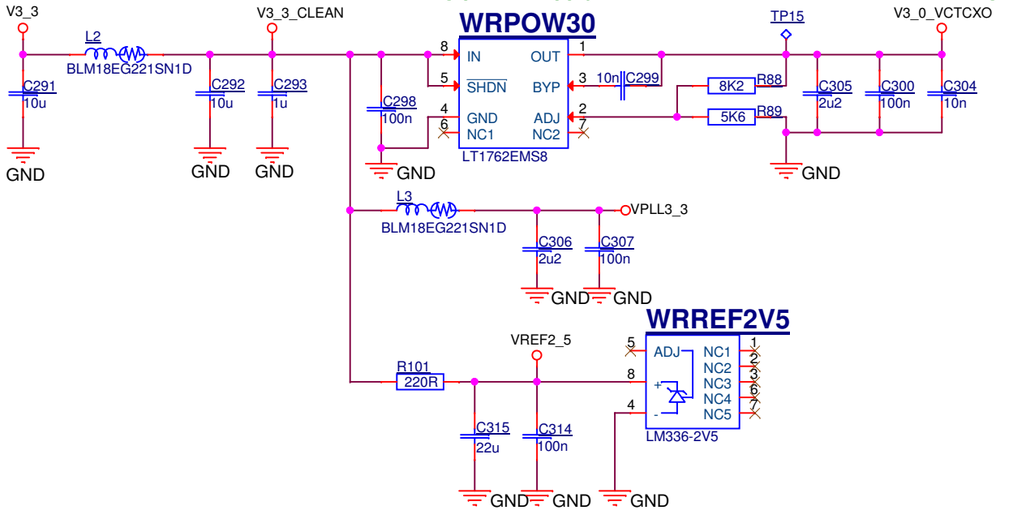
USB bridge - USB 2.0



ROOM: USB_INTERFACE

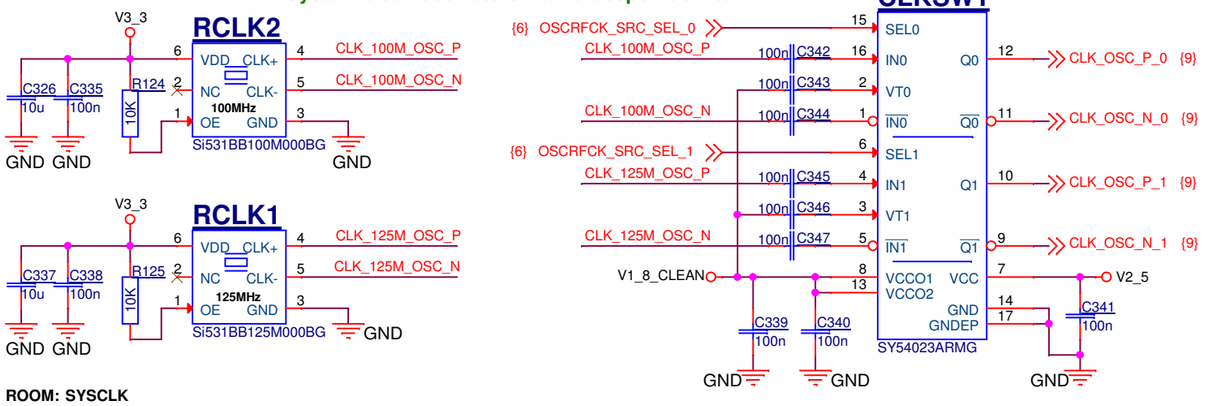
Clocking: White Rabbit DAC, oscillators, PLL ; System clocks and clock crosspoint switch

White Rabbit clocking power supply



ROOM: WRCLK_POWER

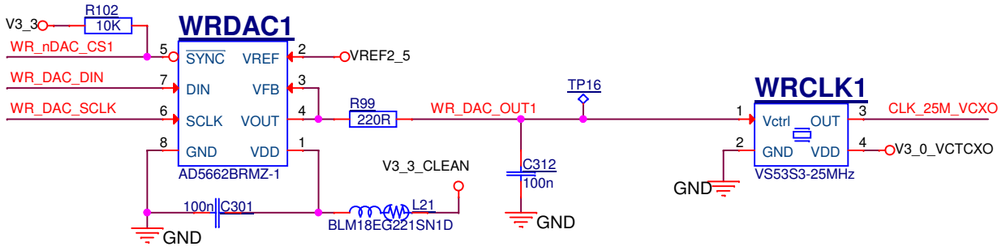
System clock oscillators with crosspoint switch



ROOM: SYSCLK

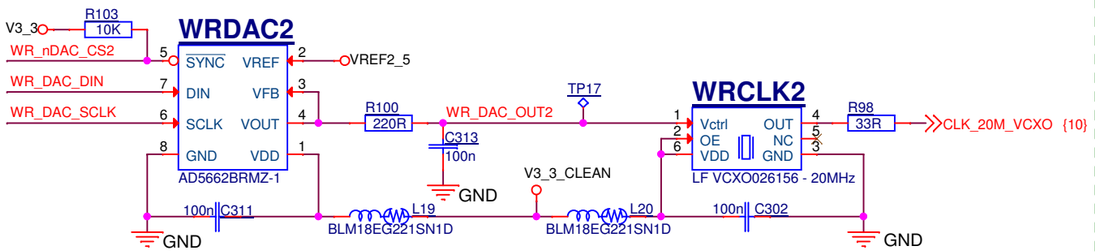
{7} WR_nDAC_CS1 — WR_nDAC_CS1
{7} WR_nDAC_CS2 — WR_nDAC_CS2
{7} WR_DAC_DIN — WR_DAC_DIN
{7} WR_DAC_SCLK — WR_DAC_SCLK

WRCLK_DAC1_CLK1



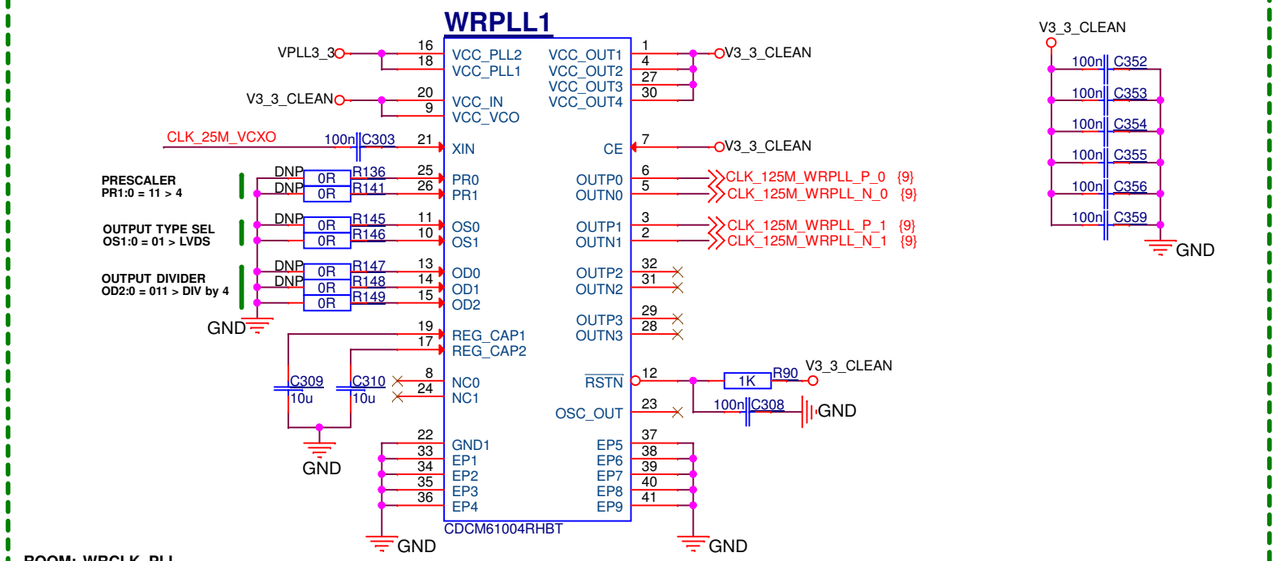
ROOM: WRCLK_DAC1_CLK1

WRCLK_DAC2_CLK2



ROOM: WRCLK_DAC2_CLK2

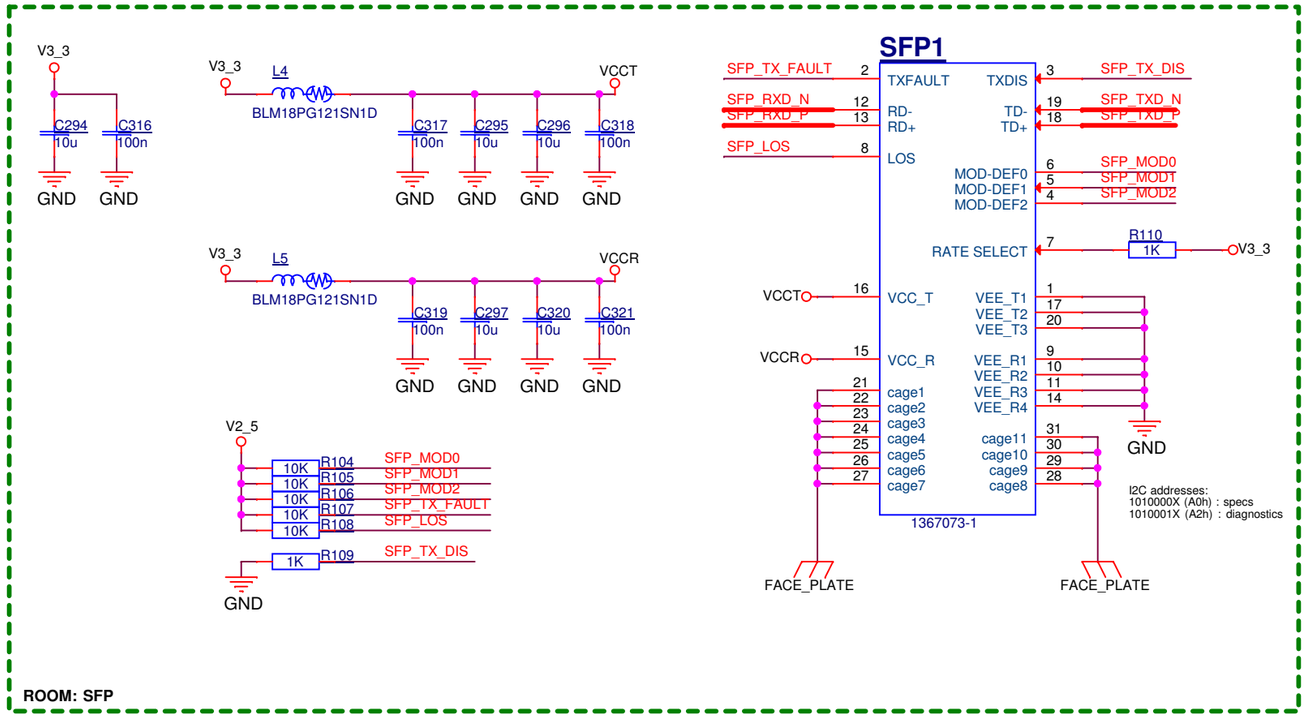
WRCLK_PLL



ROOM: WRCLK_PLL

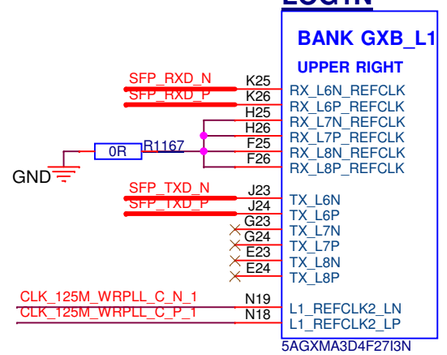
Title	Clocking: White Rabbit DAC, oscillators, PLL ; System clocks and clock crosspoint switch		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
		SHEET 8 OF 17	

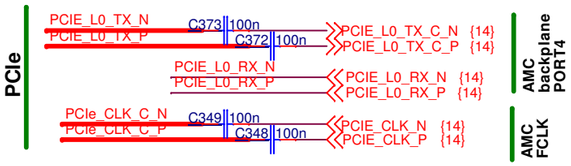
Fiber SFP, PCIe <> FPGA connections



IMPORTANT!
Hi speed Gigabit lines
100R differential

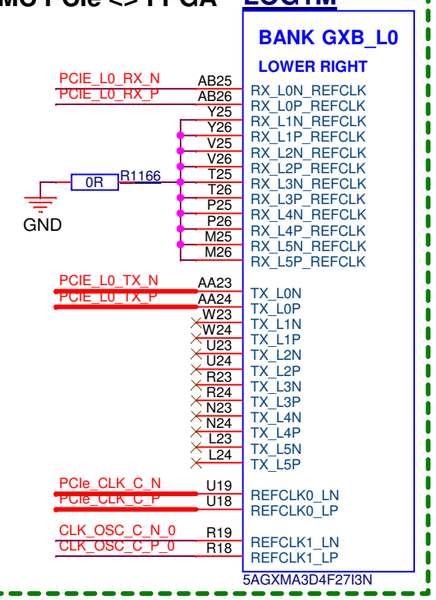
LOG1N





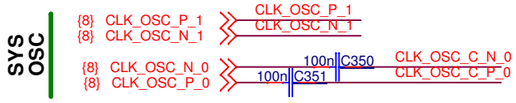
AMC PCIe <> FPGA

LOG1M



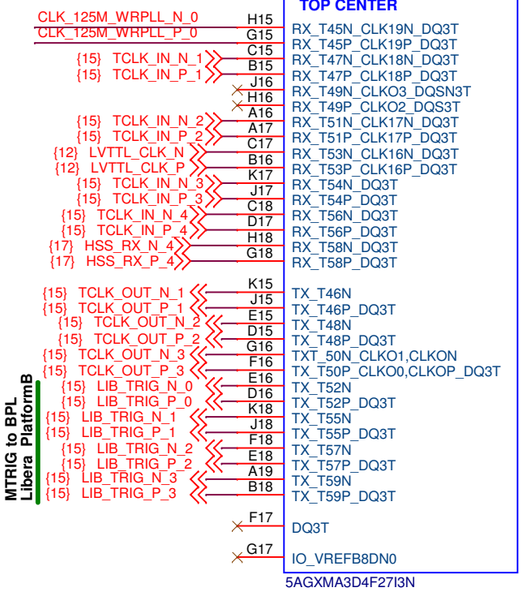
WR PLL 125 MHz

SYS OSC



LOG1L

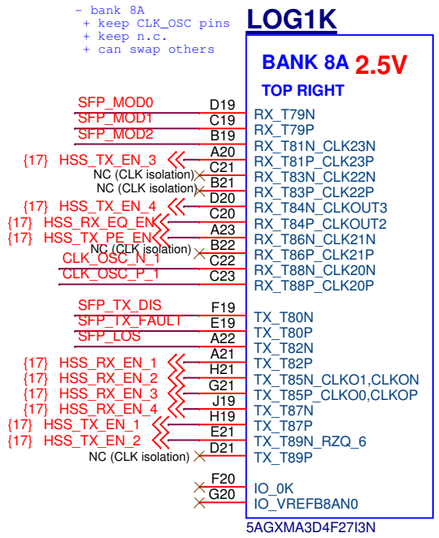
- bank 8D
+ keep CLK_125M_WRPLL
+ can swap RX 47, 51, 53
+ can swap RX 54, 56, 58
+ can swap TX half



MTRIG to BPL
Libera PlatformB

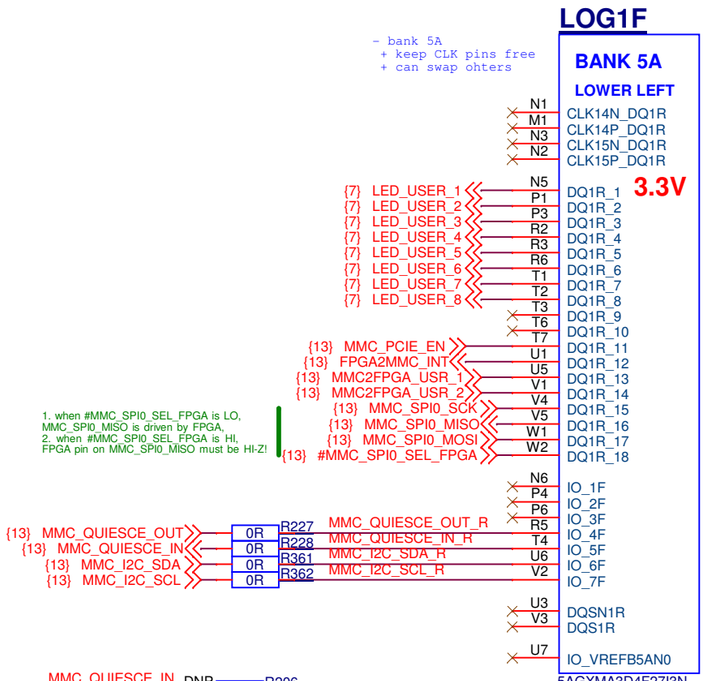
LOG1K

- bank 8A
+ keep CLK_OSC pins
+ keep n.c.
+ can swap others



LOG1F

- bank 5A
+ keep CLK pins free
+ can swap ohters



Title	Fiber SFP, PCIe <> FPGA connections		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
		SHEET 9 OF 17	

IO block power supply, FPGA <> IO block connections

LOG1J

- bank 7D
+ can swap RX group pairs
+ can swap TX group pairs

BANK 7D — TOP CENTER — 2.5V — 5AGXMA3D4F27I3N

MTCA.4 TRIG inputs from BPL

{16} MLVDIO_IN_N_1	C10	RX_T30N_DQ2T
{16} MLVDIO_IN_P_1	B10	RX_T30P_DQ2T
{16} MLVDIO_IN_N_2	K12	RX_T32N_DQ2T
{16} MLVDIO_IN_P_2	J11	RX_T32P_DQ2T
{16} MLVDIO_IN_N_3	A12	RX_T34N_DQSN2T
{16} MLVDIO_IN_P_3	A11	RX_T34P_DQS2T
{16} MLVDIO_IN_N_4	J12	RX_T36N_DQ2T
{16} MLVDIO_IN_P_4	H12	RX_T36P_DQ2T
{16} MLVDIO_IN_N_5	C12	RX_T38N_DQ2T
{16} MLVDIO_IN_P_5	B12	RX_T38P_DQ2T
{16} MLVDIO_IN_N_6	B13	RX_T39N_DQ2T
{16} MLVDIO_IN_P_6	A13	RX_T39P_DQ2T
{16} MLVDIO_IN_N_7	E13	RX_T41N_DQ2T
{16} MLVDIO_IN_P_7	D13	RX_T41P_DQ2T
{16} MLVDIO_IN_N_8	A14	RX_T43N_DQ2T
{16} MLVDIO_IN_P_8	A15	RX_T43P_DQ2T

MTCA.4 TRIG outputs from BPL

{16} MLVDIO_OUT_N_1	G11	TX_T31N
{16} MLVDIO_OUT_P_1	F11	TX_T31P_DQ2T
{16} MLVDIO_OUT_N_2	D11	TX_T33N
{16} MLVDIO_OUT_P_2	C11	TX_T33P_DQ2T
{16} MLVDIO_OUT_N_3	G12	TX_T35N
{16} MLVDIO_OUT_P_3	F12	TX_T35P_DQ2T
{16} MLVDIO_OUT_N_4	E12	TX_T37N
{16} MLVDIO_OUT_P_4	D12	TX_T37P_DQ2T
{16} MLVDIO_OUT_N_5	D14	TX_T40N
{16} MLVDIO_OUT_P_5	C14	TX_T40P_DQ2T
{16} MLVDIO_OUT_N_6	G14	TX_T42N
{16} MLVDIO_OUT_P_6	F14	TX_T42P_DQ2T
{16} MLVDIO_OUT_N_7	J14	TX_T44N
{16} MLVDIO_OUT_P_7	J13	TX_T44P_DQ2T
	G13	DQ2T
	H13	IO_VREFB7DN0

LOG1I

- bank 7C
+ can swap RX group pairs
+ can swap TX group pairs

BANK 7C — TOP LEFT — 2.5V — 5AGXMA3D4F27I3N

Front panel LEMO LVTTL IO data inputs LVDS, up to 200MHz

{11} LVTIO_IN_N_1	E6	RX_T15N_DQ1T
{11} LVTIO_IN_P_1	D6	RX_T15P_DQ1T
{11} LVTIO_IN_N_2	F7	RX_T17N_DQ1T
{11} LVTIO_IN_P_2	E7	RX_T17P_DQ1T
{11} LVTIO_IN_N_3	A6	RX_T19N_DQSN1T
{11} LVTIO_IN_P_3	A5	RX_T19P_DQS1T
{12} LVTIO_IN_N_4	C6	RX_T21N_DQ1T
{12} LVTIO_IN_P_4	B6	RX_T21P_DQ1T
{12} LVTIO_IN_N_5	H9	RX_T23N_DQ1T
{12} LVTIO_IN_P_5	G9	RX_T23P_DQ1T
{17} HSS_RX_N_1	D8	RX_T24N_DQ1T
{17} HSS_RX_P_1	C8	RX_T24P_DQ1T
{17} HSS_RX_N_2	E9	RX_T26N_DQ1T
{17} HSS_RX_P_2	D9	RX_T26P_DQ1T
{17} HSS_RX_N_3	H10	RX_T28N_DQ1T
{17} HSS_RX_P_3	G10	RX_T28P_DQ1T

Front panel LEMO LVTTL IO data outputs LVDS, up to 200MHz

{11} LVTIO_OUT_N_1	J8	TX_T16N
{11} LVTIO_OUT_P_1	J9	TX_T16P_DQ1T
{11} LVTIO_OUT_N_2	D5	TX_T18N
{11} LVTIO_OUT_P_2	C5	TX_T18P_DQ1T
{11} LVTIO_OUT_N_3	G8	TX_T20N
{11} LVTIO_OUT_P_3	F8	TX_T20P_DQ1T
{12} LVTIO_OUT_N_4	C7	TX_T22N
{12} LVTIO_OUT_P_4	B7	TX_T22P_DQ1T
{12} LVTIO_OUT_N_5	A9	TX_T25N
{12} LVTIO_OUT_P_5	A8	TX_T25P_DQ1T
{16} MLVDIO_OUT_N_8	K10	TX_T27N
{16} MLVDIO_OUT_P_8	J10	TX_T27P_DQ1T
{15} TCLK_OUT_N_4	C9	TX_T29N
{15} TCLK_OUT_P_4	B9	TX_T29P_DQ1T
	E10	DQ1T
	F10	IO_VREFB7CN0

LOG1H

- bank 7A
+ keep CRC_ERROR
+ kepp PCIE_RST
+ can swap others

BANK 7A — TOP LEFT — 3.3V — 5AGXMA3D4F27I3N

FRONT PANEL LEMO LVTTL IO control signals

	G4	RX_T1N
	F4	RX_T1P
	C2	RX_T2N_DEV_CLRN
	C3	RX_T2P_DEV_OE
{6} CRC_ERROR	A3	RX_T4N_CRC_ERROR
	A2	RX_T4P_CVP_CONFDONE
{12} #LVTTL_IN_CLK_EN	B3	RX_T6N_NCEO
	C4	RX_T6P_INIT_DONE
{11} #LVTIO_OE_1	E4	TX_T5N_PR_REQUEST
{11} #LVTIO_OE_2	D4	TX_T5P_PR_DONE
{11} #LVTIO_OE_3	B4	TX_T7N_PR_READY
{12} #LVTIO_OE_4	A4	TX_T7P_PR_ERROR
{12} #LVTIO_OE_5	J6	IO_0H
	G6	IO_RZQ_5
{13} #MMC_PCIE_RST	R229 1K	
	J7	IO_VREFB7AN0
#MMC_PCIE_RST_R	F6	NPERSTL0

LOG1B

- bank 3D
+ keep HHS_TX_x on TX half, or move to bank 3A
+ can swap ohters

BANK 3D — BOTTOM RIGHT — 2.5V — 5AGXMA3D4F27I3N

FRONT PANEL LEMO LVTTL IO control signals

{11} LVTIO_TERM_EN_1	AD18	RX_B32N_DQ1B
{11} LVTIO_LED_ACT_1	AE18	RX_B32P_DQ1B
{11} LVTIO_LED_DIR_1	W18	RX_B34N_DQ1B
{11} LVTIO_TERM_EN_2	Y18	RX_B34P_DQ1B
{11} LVTIO_LED_ACT_2	AB16	RX_B36N_DQ1B
{11} LVTIO_LED_DIR_2	AC16	RX_B36P_DQ1B
{11} LVTIO_TERM_EN_3	V16	RX_B37N_CLK4N_DQ1B
{11} LVTIO_LED_ACT_3	W16	RX_B37P_CLK4P_DQ1B
{11} LVTIO_LED_DIR_3	AF15	RX_B39N_CLK5N_DQ1B
{12} LVTIO_TERM_EN_4	AF16	RX_B39P_CLK5P_DQ1B
{11} LVTIO_LED_ACT_4	V15	RX_B41N_CLKO3_DQSN1B
{11} LVTIO_LED_DIR_4	W15	RX_B41P_CLKO2_DQS1B
{12} LVTIO_TERM_EN_5	AC14	RX_B43N_CLK6N_DQ1B
{7} LVTIO_LED_ACT_5	AD14	RX_B43P_CLK6P_DQ1B
{7} LVTIO_LED_DIR_5	AF14	RX_B45N_CLK7N_DQ1B
	AF13	RX_B45P_CLK7P_DQ1B
{7} LED_STATUS_1	AA18	TX_B31N
{7} LED_STATUS_2	AB18	TX_B31P_DQ1B
{7} LED_STATUS_3	Y17	TX_B33N
{7} LED_STATUS_4	AA17	TX_B33P_DQ1B
{7} LED_STATUS_5	AC17	TX_B35N
{7} LED_STATUS_6	AD17	TX_B35P_DQ1B
{17} HSS_TX_N_1	AD16	TX_B38N
{17} HSS_TX_P_1	AE16	TX_B38P_DQ1B
{17} HSS_TX_N_2	AA15	TX_B40N_CLKO1,CLKON
{17} HSS_TX_P_2	AB15	TX_B40P_CLKO0,CLKOP_DQ1B
{17} HSS_TX_N_3	AD15	TX_B42N
{17} HSS_TX_P_3	AE15	TX_B42P_DQ1B
{17} HSS_TX_N_4	Y14	TX_B44N
{17} HSS_TX_P_4	AA14	TX_B44P_DQ1B
	AA16	DQ1B
	Y16	IO_VREFB3DN0

LOG1A

- bank 3A
+ keep CLK_20M_VCXO
+ can move hss_rx_1, hss_rx_2 to bank 3A

BANK 3A — BOTTOM RIGHT — 2.5V — 5AGXMA3D4F27I3N

	AB21	RX_B2N_CLK0N
	AC21	RX_B2P_CLK0P
	AC22	RX_B4N_CLK1N
	AD22	RX_B4P_CLK1P
NC (CLK isolation)	AF22	RX_B6N_CLKOUT3
	AF23	RX_B6P_CLKOUT2
NC (CLK isolation)	AE21	RX_B7N_CLK2N
{8} CLK_20M_VCXO	AF21	RX_B7P_CLK2P
	AF19	RX_B9N_CLK3N
NC (CLK isolation)	AF20	RX_B9P_CLK3P
	AE19	RX_B11N
	AF18	RX_B11P
	AA20	TX_B1N_RZQ_0
	AB19	TX_B1P
	Y21	TX_B3N
	AA21	TX_B3P
	AD23	TX_B5N_CLKO1,CLKON
	AE23	TX_B5P_CLKO0,CLKOP
	AC20	TX_B8N
	AD20	TX_B8P
	AC19	TX_B10N
	AD19	TX_B10P
	Y19	IO_0A
	Y20	IO_VREFB3AN0

Power supply for output drivers

V12_0CAR — 10K R133 — CMDSH2-3 DSH12 — D17 LR QH9F red — GND

RUN driven by MMC or AUX V12 presence

POWIO33A — LTM8023EV

PRUN_3V3_IO	H5	RUN/SS	AUX F5
			BIAS G5
PGOOD_3V3_IO	H6	PGOOD	SYNC G6 — 10K R132
			ADJ H7 — 154K R131
	F7	SHARE	R_T G7 — 49K9 R129

PRUN_3V3_IO → PRUN_3V3_IO {13}

PGOOD_3V3_IO → PGOOD_3V3_IO {13}

GND

POWIO33B — LTM8023EV

V12_0CAR — C331 100n — C330 10u — GND GND

	G1	V_IN1	V_OUT1 A1
	G2	V_IN2	V_OUT2 A2
	G3	V_IN3	V_OUT3 A3
	H1	V_IN4	V_OUT4 A4
	H2	V_IN5	V_OUT5 B1
	H3	V_IN6	V_OUT6 B2
			V_OUT7 B3
			V_OUT8 B4
			V_OUT9 C1
			V_OUT10 C2
			V_OUT11 C3
			V_OUT12 C4

TP18 — SJMP8 (1) — C332 22u — GND

V33_ODRV — C333 100u — C334 100u — GND GND

POWIO33C — LTM8023EV

	A5	GND1	GND24 F6
	A6	GND2	GND23 E7
	B5	GND3	GND22 E6
	B6	GND4	GND21 E5
	B7	GND5	GND20 E4
	C5	GND6	GND19 E3
	C6	GND7	GND18 E2
	C7	GND8	GND17 E1
	D1	GND9	GND16 D7
	D2	GND10	GND15 D6
	D3	GND11	GND14 D5
		GND12	GND13 D4

GND GND

ROOM: IO_POWER

LOG1E

- bank 4D
+ keep fee DQ2B, IO_VREF
+ can swap other

BANK 4D — BOTTOM CENTER — 3.3V — 5AGXMA3D4F27I3N

{16} MLVDIO_DE_1	AB13	RX_B47N_DQ2B
{16} #MLVDIO_RE_1	AC13	RX_B47P_DQ2B
{16} MLVDIO_DE_2	AD13	RX_B49N_DQ2B
{16} #MLVDIO_RE_2	AE13	RX_B49P_DQ2B
{16} MLVDIO_DE_3	AD12	RX_B51N_DQ2B
{16} #MLVDIO_RE_3	AE12	RX_B51P_DQ2B
{16} MLVDIO_DE_4	AF12	RX_B52N_DQ2B
{16} #MLVDIO_RE_4	AF11	RX_B52P_DQ2B
{16} MLVDIO_DE_5	AC10	RX_B54N_DQ2B
{16} #MLVDIO_RE_5	AD10	RX_B54P_DQ2B
{16} MLVDIO_DE_6	AE10	RX_B56N_DQSN2B
{16} #MLVDIO_RE_6	AF9	RX_B56P_DQS2B
{16} MLVDIO_DE_7	V10	RX_B58N_DQ2B
{16} #MLVDIO_RE_7	W10	RX_B58P_DQ2B
{16} MLVDIO_DE_8	AB9	RX_B60N_DQ2B
{16} #MLVDIO_RE_8	AC9	RX_B60P_DQ2B
{16} MLVDIO_FSEN	V13	TX_B46N
{16} #MLVDIO_PDN	W13	TX_B46P_DQ2B
{15} #TCLK_EN_1	Y13	TX_B48N
{15} TCLK_DIR_1	AA13	TX_B48P_DQ2B
{15} #TCLK_EN_2	V12	TX_B50N
{15} TCLK_DIR_2	W12	TX_B50P_DQ2B
{15} #TCLK_EN_3	AC11	TX_B53N
{15} TCLK_DIR_3	AD11	TX_B53P_DQ2B
{15} #TCLK_EN_4	Y11	TX_B55N
{15} TCLK_DIR_4	AA11	TX_B55P_DQ2B
	AD9	TX_B57N
{15} LIB_TRIG_OE	AE9	TX_B57P_DQ2B
	Y10	TX_B59N
	AA10	TX_B59P_DQ2B
	AB12	DQ2B
	AA12	IO_VREFB4DN0

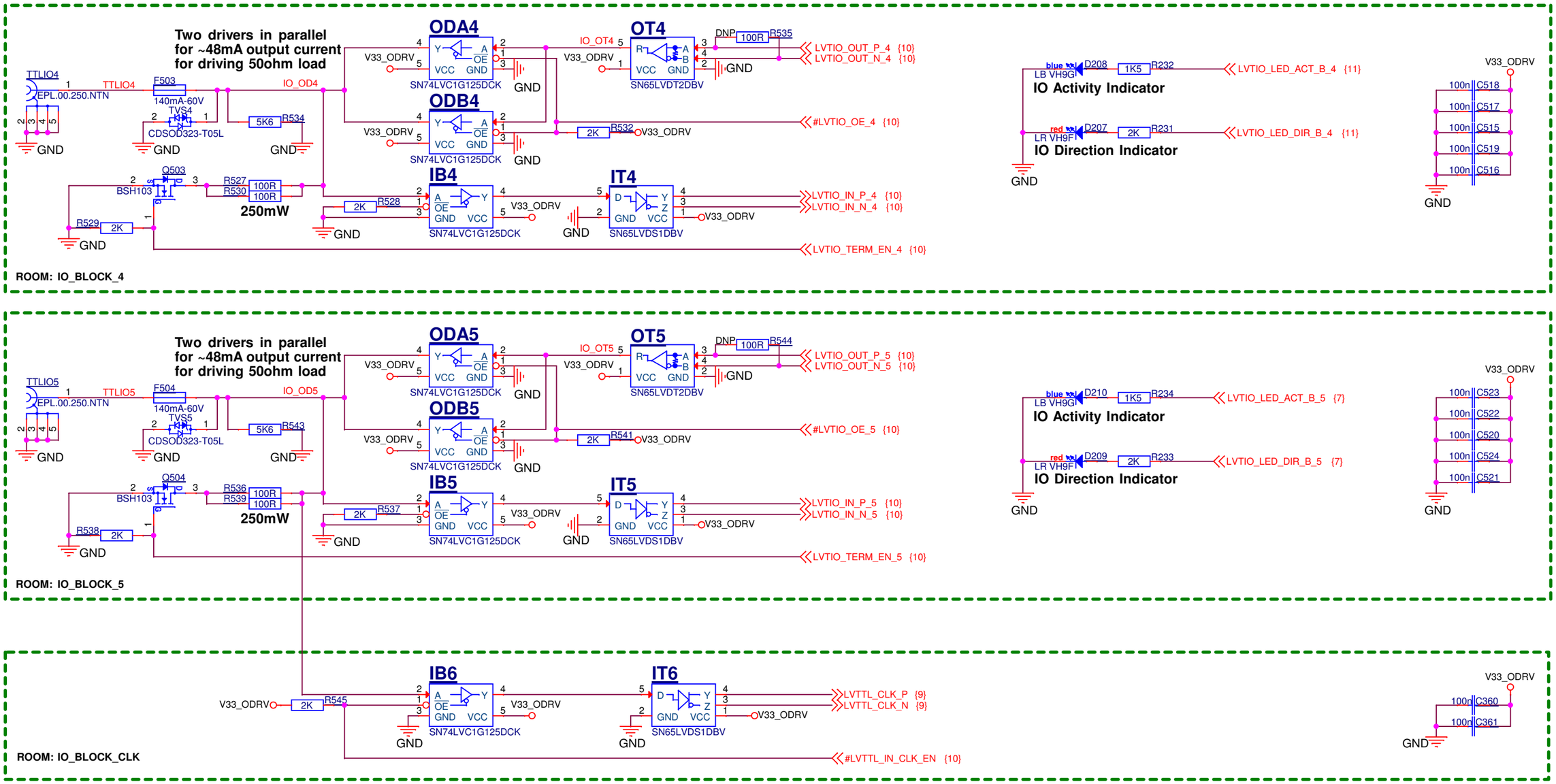
(1) - 0R solder connection, to test regulator outputs before connecting to load

Title	IO block power supply, FPGA <> IO block connections		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
			SHEET 10 OF 17

LVTTL IO blocks 1-3

Title	LVTTL IO blocks 1-3		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
		SHEET 11 OF 17	

LVTTL IO blocks 4-5, IO CLOCK input



Title	LVTTL IO blocks 4-5, IO CLOCK input		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
		SHEET 12 OF 17	

MMC, IPMI

MMC user push button

PBM1 (KMR223G-LFG): V33_MP — R175 10K — #MMC_PB_1; C490 100n to GND

PBM2 (KMR223G-LFG): V33_MP — R176 10K — #MMC_PB2_JCON; C491 100n to GND

#MMC_PB_2 used as MMC reset

ROOM: MMC_PBS_LEDS

MMC user LEDs

V33_MP — R96 1K — LR QH9F red DU1 — #MMC_ULED_0

R94 510R — LT QH9G green DU2 — #MMC_ULED_1

PMX1

V33_MP_BPL, V3_3 → IN1, IN2, VSNS, EN; STAT, OUT, ILIM, GND

R1165 0R → V33_MP; R1095 510R → GND

TPS2112APW

MP power MUX:
- in crate: V33_MP_BPL > 0.8V
  out = V33_MP_BPL
- not in crate, on AUX:
  V33_MP_BPL (0V) < 0.8V
  out = V3_3

MMC JTAG connector

JTAG1 M50-3600542: VCC, GND1, GND2, RTCK/NU, GND3, TMS/SWDIO, TCK/SWCLK, TDO/SWO, TDI/NU, #RESET

V33_MP — R1032 100R JTMS_MMC; R1033 100R JTCK_MMC; R1034 100R JTDO_MMC; R1035 100R JTDI_MMC; #MMC_PB2_JCON

DTV2 TPD6E05U06RVZR: JTMS_MMC, JTCK_MMC, JTDO_MMC, JTDI_MMC, #MMC_PB2_JCON

V33_MP — R157 10K; R161 10K; R158 10K; R159 10K; R160 10K; C366 100n

#JTRST_MMC {14} ← JTMS_MMC, JTCK_MMC, JTDO_MMC, JTDI_MMC

USB <> UART for MMC console (on the front panel if possible)

USBCON2 MICRO-B ZX62-B-5PA(11): MMC_USB_K_DM, MMC_USB_K_DP

LUSB2 744232090: MMC_USB_L_DM, MMC_USB_L_DP

DUSB2 TPD6E05U06RVZR: MMC_USB_VBUS, MMC_USB_L_DM, MMC_USB_L_DP

R163 10K; R162 4K7 → VBUS_SENSE; R164 33R → MMC_USB_R_DM; R165 33R → MMC_USB_R_DP

22p C381, C383, C382, C387 → GND

IC1 FT230XQ: USBDM, USBDP, CBUS3, CBUS2, CBUS1, CBUS0, GND1, GND2, EP, TXD, RXD, RTS#, CTS#, RESET#, VCCIO, 3V3OUT, VCC

MMC_USB_R_DM, MMC_USB_R_DP; MMC_UART_RX, MMC_UART_TX

VBUS_SENSE; #RX_LED, #TX_LED

R350 510R — green LT QH9G D23

R351 1K — white LW QH8G D24

2.2u C378, C379; 100n C374, C375, C380 → GND

ROOM: MMC_USB

MMC FW FLASH

MMEM1 M25P80-VMN6P: HOLD#, DOUT, DIN, CLK, CS#, VSS, VCC

MMC_SPI0_MISO, MMC_SPI0_MOSI, MMC_SPI0_SEL_FLASH

100n C403

MMC local I2C bus: - temp sensors, FRU EEPROM

R154 10K MMC_I2C_SDA; R155 10K MMC_I2C_SCL; R156 10K #OVERTEMP

TP21, TP22, TP23, TP25

TS1 LM73CIMK-0: VDD, SDA, SCL, ALERT, GND, ADDR

C400 100n; R166 10K 1001:001

TS2 LM73CIMK-0: C404 100n; R167 10K 1001:010

FRU, SDR, CONFIG EEPROM — MMEM2 24LC512I/MF: SDA, SCL, A0, A1, A2, VCC, WP, VSS, EXP. PAD

MMC_I2C_SDA, MMC_I2C_SCL; C372 100n; R172 10K; R173 10K; R174 10K

ROOM: MMC_TEMP_FRUMEM

MMC1A

LPC2136FBD64

TX and RX signal naming is refering to the MMC side

CLI and Debug UART: MMC_UART_TX, MMC_UART_RX

{14} IPMB_L_SCL, {14} IPMB_L_SDA

{9} MMC_SPI0_SCK, {9} MMC_SPI0_MISO, {9} MMC_SPI0_MOSI, #MMC_SPI0_SEL_FLASH

{9} #MMC_SPI0_SEL_FPGA, {14} JTAGSW_SEL, {9} MMC_PCIE_EN, {9} MMC_I2C_SCL, MMC_DCDC_EN, MMC_PGOOD, MMC_I2C_SDA, {9} MMC_I2C_SDA, #MMC_HANDLE_SW

P0.0/TXD0/PWM1, P0.1/RXD0/PWM3/EINT0, P0.2/SCL0/CAP0.0, P0.3/SDA0/MAT0.0/EINT1, P0.4/SCK0/CAP0.1/AD0.6, P0.5/MISO0/MAT0.1/AD0.7, P0.6/MOSI0/CAP0.2/AD1.0, P0.7/SSEL0/PWM2/EINT2

P0.8/TXD1/PWM4/AD1.1, P0.9/RXD1/PWM6/EINT3, P0.10/RTS1/CAP1.0/AD1.2, P0.11/CTS1/CAP1.1/SCL1, P0.12/DSR1/MAT1.0/AD1.3, P0.13/DTR1/MAT1.1/AD1.4, P0.14/DCD1/EINT1/SDA1, P0.15/RI1/EINT2/AD1.5

P0.16/EINT0/MAT0.2/CAP0.2, P0.17/CAP1.2/SCK1/MAT1.2, P0.18/CAP1.3/MISO1/MAT1.3, P0.19/MAT1.2/MOSI1/CAP1.2, P0.20/MAT1.3/SSEL1/EINT3, P0.21/PWM5/AD1.6/CAP1.3, P0.22/AD1.7/CAP0.0/MAT0.0, P0.23

P0.25/AD0.4/AOUT, P0.26/AD0.5, P0.27/AD0.0/CAP0.1/MAT0.1, P0.28/AD0.1/CAP0.2/MAT0.2, P0.29/AD0.2/CAP0.3/MAT0.3, P0.30/AD0.3/EINT3/CAP0.0, P0.31

#MMC_PB_1; FPGA2MMC_INT {9}; #MMC_FPGA_CONFIG {6}; MMC_QUIESCE_OUT {9}; MMC_QUIESCE_IN {9}

MMC2FPGA_USR_1 {9}; MMC2FPGA_USR_2 {9}; #MMC_PCIE_RST {10}

MMC_VS_V1_15_T, MMC_VS_V1_15_C, MMC_VS_V3_3, MMC_VS_V2_5, MMC_VS_V12CAR, MMC_VS_V3_3_MP, #MMC_LED_HOTSWAP

power voltage sensing - analog inputs

MMC1B

LPC2136FBD64

V33_MP — R186 30K1 IPMB_L_SDA; R187 30K1 IPMB_L_SCL → TP19, TP20, TP24

Test pads for I2C bus sniffing

#MMC_LED_FAIL, #MMC_LED_OK, #MMC_LED_FWRELOAD, #MMC_ULED_0, #MMC_ULED_1

{14} IPMI_GA_0, {14} IPMI_GA_1, {14} IPMI_GA_2 → IPMI_GA_0, IPMI_GA_1, IPMI_GA_2

3K3 R196 IPMI_GA_0; 3K3 R197 IPMI_GA_1; 3K3 R198 IPMI_GA_2

AMC geographical address from backplane

MMC_GA_COMMON, CONF_DONE, PRESENT_V12AUX

{6} CONF_DONE, {4,13,14} PRESENT_V12AUX

P1.16/TRACEPKT0, P1.17/TRACEPKT1, P1.18/TRACEPKT2, P1.19/TRACEPKT3, P1.20/TRACESYNC, P1.21/PIPESTAT0, P1.22/PIPESTAT1, P1.23/PIPESTAT2, P1.24/TRACECLK, P1.25/EXTIN0, P1.26/RTCK

P1.27/TDO, P1.28/TDI, P1.29/TCK, P1.30/TMS, P1.31/TRST

JTDO_MMC, JTDI_MMC, JTCK_MMC, JTMS_MMC

R1169 0R; R168 10K → V33_MP; #JTRST_MMC

JTRST# only from backplane, JTAG connector does not provide JTRST#

Resistor dividers for voltage sensors

V12_0CAR — R207 4K7 — MMC_VS_V12CAR — R208 510R — R212 1K

V33_MP — R209 510R — MMC_VS_V3_3_MP — R210 100R — R216 1K

V3_3 — R211 220R — MMC_VS_V3_3 — R217 1K

V2_5 — R213 33R — MMC_VS_V2_5 — R218 1K

V1_15_T — R214 33R — MMC_VS_V1_15_T — R219 1K

V1_15_C — R215 33R — MMC_VS_V1_15_C — R220 1K

GND

ROOM: MMC_VOLT_RED_DIV

MRST1

V33_MP — C385 100n — GND

MRST1 TPS3823-33DBVT: VDD, GND, WDI, out RST, in MR

#MMC_RESET, #MMC_RESET_CMB

ROOM: MMC_RST_EN

R183 10K — V33_MP; {13,14} #IPMI_MMC_ENABLE → Q10 BSH103

{4,13,14} PRESENT_V12AUX

Force #IPMI_MMC_ENABLE low when FTRN powered from AUX power (not in the crate). Use Push-button for MMC reset.

{13,14} #IPMI_MMC_ENABLE → #IPMI_MMC_ENABLE_R — R199 0R; R200 10K DNP → GND

Option to not use #IPMI_MMC_ENABLE for MMC reset

IC2

2-Input AND Gate With One Inverted Input (IN2):
If (NOT #IPMI_MMC_EN) = H and #MMC_PB_2 = H
#MMC_RESET_CMB = H
else
#MMC_RESET_CMB = L (active)

#MMC_PB2_JCON, #IPMI_MMC_ENABLE_R → IN0, IN1, IN2; Y → V33_MP

SN74LVC1G97DCK C384 100n

MVREF1

V33_MP — R188 220R — VREF2_5_MMC

C410 22u, C327 100n → GND

ADJ, NC1, NC2, NC3, NC4, NC5 LM336-2V5

XTL2

C1E-24.000-12-3050-R — 12p C401, 12p C402 → GND

#MMC_RESET

MMC1C

LPC2136FBD64

RESET, XTAL1, XTAL2, RTCX1, RTCX2, VBAT, VREF, VDDA, VSSA, VDD1, VDD2, VDD3, VSS1, VSS2, VSS3, VSS4, VSS5

V33_ADC, AGND, V33_MMC, V33_MMC, VREF2_5_MMC

V33_MMC — L17 BLM18PG221SN1D — 22u C395, 22u C396, 100n C392, 100n C393, 100n C394 → GND

V33_MP — L18 BLM18PG221SN1D — 100n C397, 100n C399, 10n C398 → L16 BLM18PG221SN1D → AGND

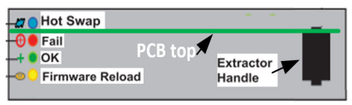
V33_ADC — V33_MP

MTCA Extractor handle switch

SW1 HDT0001 N.O.: 1, 2, 3, 4

R153 10K — V33_MP; R1031 1K — #MMC_HANDLE_SW; C412 100n

ROOM: MMC_HANDLE



IPMI/AMC status LEDs on the front panel

QH - top (green, white), VH - side (blue, red)

V33_MP — R300 510R — LB VH9G D32 blue — #MMC_LED_HOTSWAP

R301 1K — LR VH9F D33 red — #MMC_LED_FAIL

R302 510R — LT QH9G D20 green — #MMC_LED_OK

R303 1K — LW QH8G D22 white — #MMC_LED_FWRELOAD

ROOM: MMC_IPMI_LEDS

Power sequencing

TURN ON for main power regulators, 2 use cases:
- when in crate, by MMC_DCDC_EN
- when on AUX power, DCDC converters are turned on by default, MMC is overriden

MMC_DCDC_EN — DSH7 CMDSH2-3; {4,13,14} PRESENT_V12AUX — DSH8 CMDSH2-3 — R185 1K → GND

0R R201 PRUN_3V3; 0R R202 PRUN_1V15_T; 0R R203 PRUN_1V15_C; 0R R204 PRUN_2V5; 0R R205 PRUN_3V3_IO

PRUN_3V3 {4}, PRUN_1V15_T {4}, PRUN_1V15_C {4}, PRUN_2V5 {4}, PRUN_3V3_IO {10}

enable outputs of payload power converters

V33_MP — R184 10K — MMC_PGOOD

DSH3 CMDSH2-3 PGOOD_1V15 {4}

DSH5 CMDSH2-3 PGOOD_2V5_3V3 {4}

DSH6 CMDSH2-3 PGOOD_3V3_IO {10}

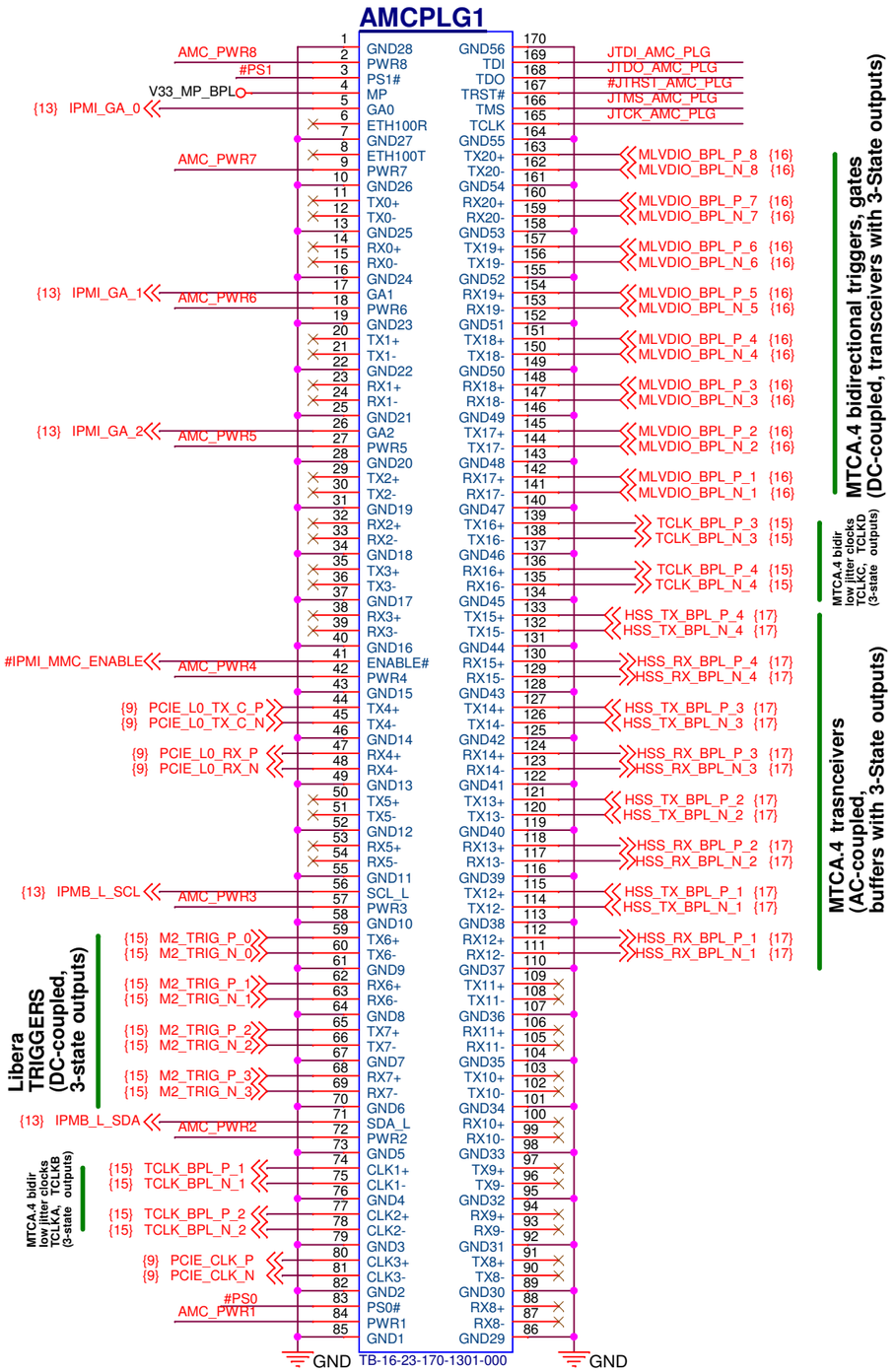
monitor status of payload power converters

PGOOD signals from each power converter are joined but still isolated (wired AND function). This way each PGOOD can still have its own LED indicator.

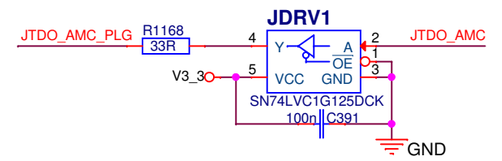
Title: MMC, IPMI			
Size: A3	Type: SE	DWG.NO. CSL_FTRN_AMC	REV. A
			SHEET 13 OF 17

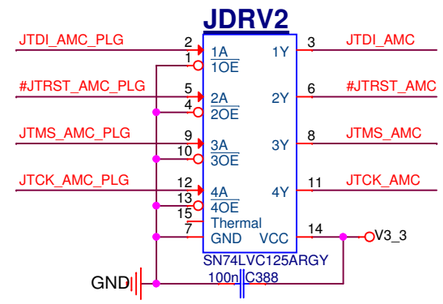
AMC backplane plug

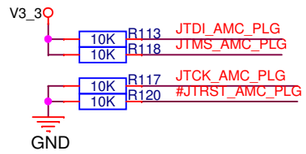
JTAG signals length from the AMCPLG1 connector to the JDRVx buffers is 100mm MAX!!!



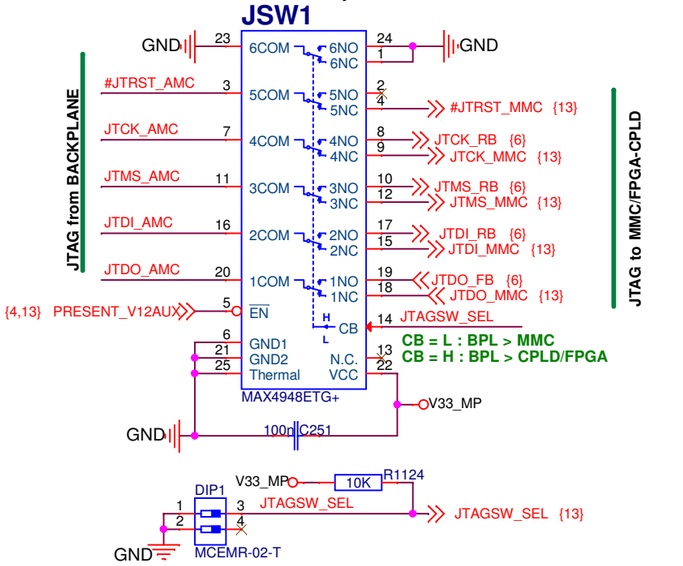
Backplane plug will be implemented directly on PCB!

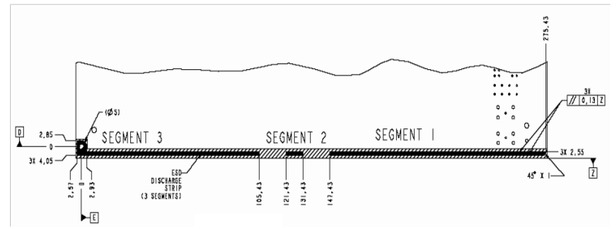


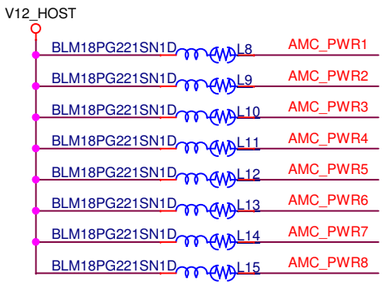


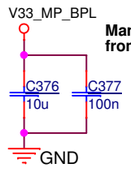


JTAG swithc for routing Backplane JTAG to MMC or CPLD/FPGA. Monitored by MMC.



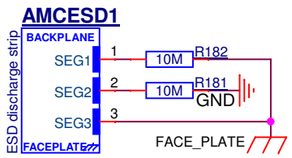


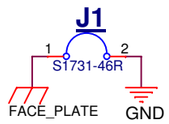




Management Power from MTCA backplane

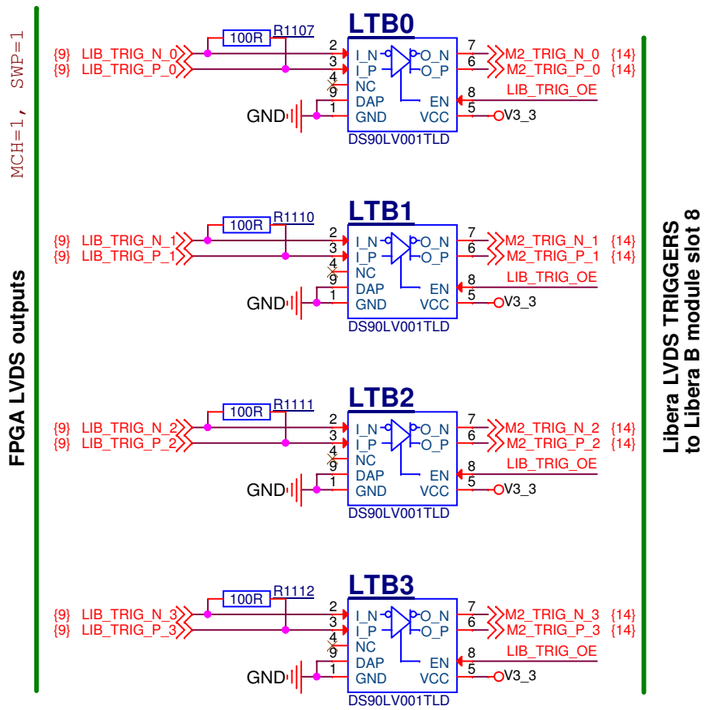
AMC card presence detection. PS1 "shorted" to PS0 when card fully inserted into host.

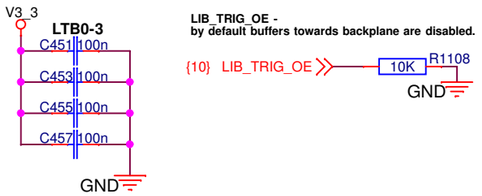




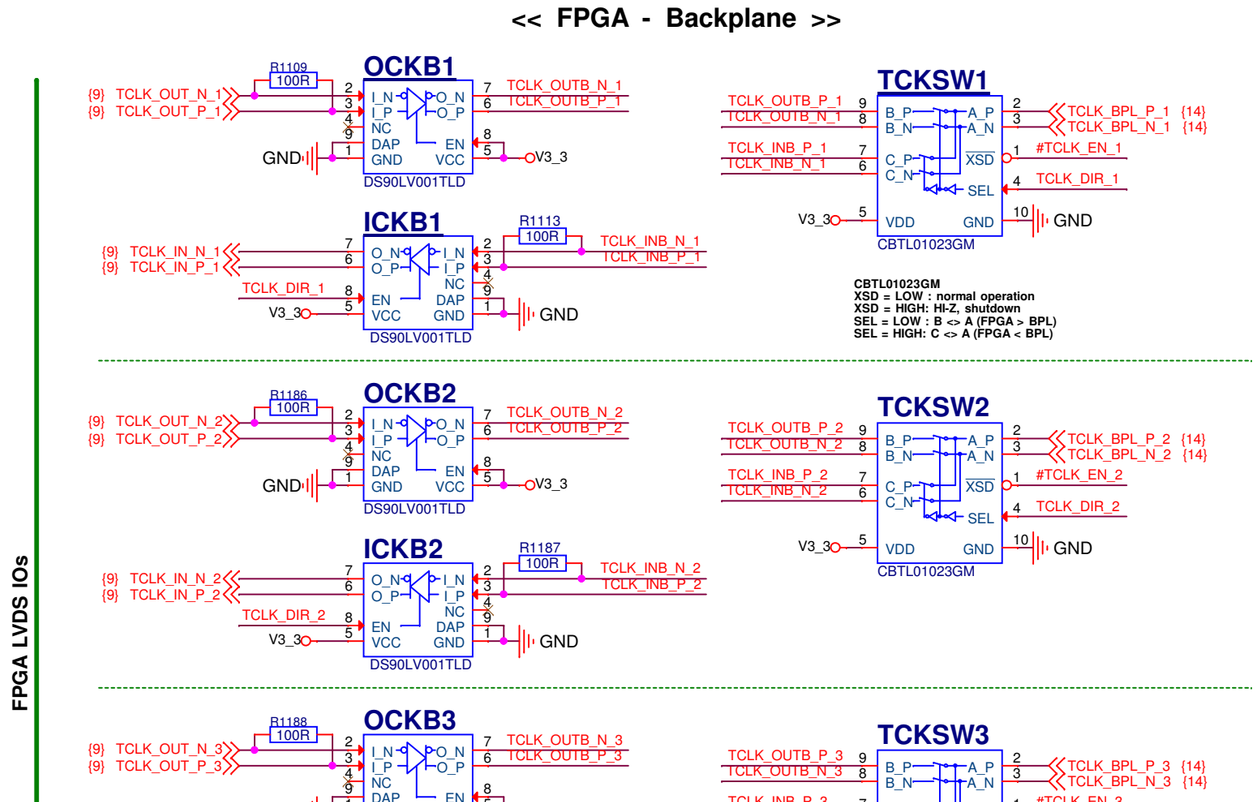
Title: AMC backplane plug			
Size: A3	Type: SE	DWG.NO. CSL_FTRN_AMC	REV. A
			SHEET 14 OF 17

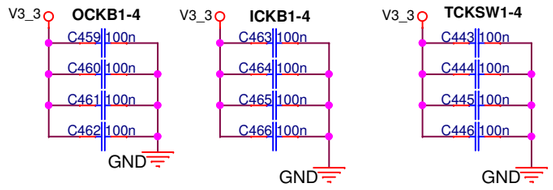
Backplane buffers - MTCA.4 TCLK A-D, Libera B triggers



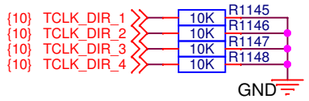


LIB_TRIG_OE -
by default buffers towards backplane are disabled.

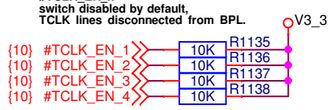




TCLK_DIR_x -
by default direction is CLK output (FPGA>BPL),
buffers towards FPGA are disabled.



#TCLK_EN_x -
switch disabled by default,
TCLK lines disconnected from BPL.



Title: Backplane buffers - MTCA.4 TCLK A-D, Libera B triggers			
Size: A3	Type: SE	DWG.NO. CSL_FTRN_AMC	REV. A
		SHEET 15 OF 17	

Backplane buffers - MTCA.4 PORT 17-20 (M-LVDS triggers, clocks, gates)

FPGA LVDS IOs

{10} MLVDIO_FSEN >> MLVDIO_FSEN

{10} #MLVDIO_PDN >> #MLVDIO_PDN

OTB1 — SN65LVDT2DBV
{10} MLVDIO_OUT_P_1, {10} MLVDIO_OUT_N_1 → MLVDIO_OUT_1; V3_3; GND

OTB2 — SN65LVDT2DBV
{10} MLVDIO_OUT_P_2, {10} MLVDIO_OUT_N_2 → MLVDIO_OUT_2; V3_3; GND

OTB3 — SN65LVDT2DBV
{10} MLVDIO_OUT_P_3, {10} MLVDIO_OUT_N_3 → MLVDIO_OUT_3; V3_3; GND

OTB4 — SN65LVDT2DBV
{10} MLVDIO_OUT_P_4, {10} MLVDIO_OUT_N_4 → MLVDIO_OUT_4; V3_3; GND

OTB5 — SN65LVDT2DBV
{10} MLVDIO_OUT_P_5, {10} MLVDIO_OUT_N_5 → MLVDIO_OUT_5; V3_3; GND

OTB6 — SN65LVDT2DBV
{10} MLVDIO_OUT_P_6, {10} MLVDIO_OUT_N_6 → MLVDIO_OUT_6; V3_3; GND

OTB7 — SN65LVDT2DBV
{10} MLVDIO_OUT_P_7, {10} MLVDIO_OUT_N_7 → MLVDIO_OUT_7; V3_3; GND

OTB8 — SN65LVDT2DBV
{10} MLVDIO_OUT_P_8, {10} MLVDIO_OUT_N_8 → MLVDIO_OUT_8; V3_3; GND

ITB1 — SN65LVDS1DBV
{10} MLVDIO_IN_P_1, {10} MLVDIO_IN_N_1; V3_3 → MLVDIO_IN_1; GND

ITB2 — SN65LVDS1DBV
{10} MLVDIO_IN_P_2, {10} MLVDIO_IN_N_2; V3_3 → MLVDIO_IN_2; GND

ITB3 — SN65LVDS1DBV
{10} MLVDIO_IN_P_3, {10} MLVDIO_IN_N_3; V3_3 → MLVDIO_IN_3; GND

ITB4 — SN65LVDS1DBV
{10} MLVDIO_IN_P_4, {10} MLVDIO_IN_N_4; V3_3 → MLVDIO_IN_4; GND

ITB5 — SN65LVDS1DBV
{10} MLVDIO_IN_P_5, {10} MLVDIO_IN_N_5; V3_3 → MLVDIO_IN_5; GND

ITB6 — SN65LVDS1DBV
{10} MLVDIO_IN_P_6, {10} MLVDIO_IN_N_6; V3_3 → MLVDIO_IN_6; GND

ITB7 — SN65LVDS1DBV
{10} MLVDIO_IN_P_7, {10} MLVDIO_IN_N_7; V3_3 → MLVDIO_IN_7; GND

ITB8 — SN65LVDS1DBV
{10} MLVDIO_IN_P_8, {10} MLVDIO_IN_N_8; V3_3 → MLVDIO_IN_8; GND

<< FPGA - Backplane >>

MTB1A — SN65MLVD040RGZ

{10} MLVDIO_DE_4	MLVDIO_OUT_4	1DE / 1D	1A / 1B → MLVDIO_BPL_P_4 {14} / MLVDIO_BPL_N_4 {14}
MLVDIO_FSEN	MLVDIO_IN_4	1FSEN / 1R / 1RE	
{10} #MLVDIO_RE_4			
{10} MLVDIO_DE_3	MLVDIO_OUT_3	2DE / 2D	2A / 2B → MLVDIO_BPL_P_3 {14} / MLVDIO_BPL_N_3 {14}
MLVDIO_FSEN	MLVDIO_IN_3	2FSEN / 2R / 2RE	
{10} #MLVDIO_RE_3			
{10} MLVDIO_DE_2	MLVDIO_OUT_2	3DE / 3D	3A / 3B → MLVDIO_BPL_P_2 {14} / MLVDIO_BPL_N_2 {14}
MLVDIO_FSEN	MLVDIO_IN_2	3FSEN / 3R / 3RE	
{10} #MLVDIO_RE_2			
{10} MLVDIO_DE_1	MLVDIO_OUT_1	4DE / 4D	4A / 4B → MLVDIO_BPL_P_1 {14} / MLVDIO_BPL_N_1 {14}
MLVDIO_FSEN	MLVDIO_IN_1	4FSEN / 4R / 4RE	
{10} #MLVDIO_RE_1			PDN ← #MLVDIO_PDN

MTB2A — SN65MLVD040RGZ

{10} MLVDIO_DE_8	MLVDIO_OUT_8	1DE / 1D	1A / 1B → MLVDIO_BPL_P_8 {14} / MLVDIO_BPL_N_8 {14}
MLVDIO_FSEN	MLVDIO_IN_8	1FSEN / 1R / 1RE	
{10} #MLVDIO_RE_8			
{10} MLVDIO_DE_7	MLVDIO_OUT_7	2DE / 2D	2A / 2B → MLVDIO_BPL_P_7 {14} / MLVDIO_BPL_N_7 {14}
MLVDIO_FSEN	MLVDIO_IN_7	2FSEN / 2R / 2RE	
{10} #MLVDIO_RE_7			
{10} MLVDIO_DE_6	MLVDIO_OUT_6	3DE / 3D	3A / 3B → MLVDIO_BPL_P_6 {14} / MLVDIO_BPL_N_6 {14}
MLVDIO_FSEN	MLVDIO_IN_6	3FSEN / 3R / 3RE	
{10} #MLVDIO_RE_6			
{10} MLVDIO_DE_5	MLVDIO_OUT_5	4DE / 4D	4A / 4B → MLVDIO_BPL_P_5 {14} / MLVDIO_BPL_N_5 {14}
MLVDIO_FSEN	MLVDIO_IN_5	4FSEN / 4R / 4RE	
{10} #MLVDIO_RE_5			PDN ← #MLVDIO_PDN

MTCA.4 M-LVDS TRIGGERS, GATES, CLOCKS (PORT 17-20)

/RE and FSEN pins have internal pull-UP resistors.
DE and /PDN pin has internal pull-DOWN resistors.

MLVDIO_IN_1	10K	R1153
MLVDIO_IN_2	10K	R1154
MLVDIO_IN_3	10K	R1155
MLVDIO_IN_4	10K	R1156
MLVDIO_IN_5	10K	R1157
MLVDIO_IN_6	10K	R1158
MLVDIO_IN_7	10K	R1159
MLVDIO_IN_8	10K	R1160

Define state when /RE is HI. → GND

MTB1B — SN65MLVD040RGZ
V3_3 → C389 100n, C413 100n, C414 100n, C415 100n, C416 100n, C417 100n, C418 100n, C419 100n → GND

MTB2B — SN65MLVD040RGZ
V3_3 → C390 100n, C420 100n, C421 100n, C422 100n, C423 100n, C424 100n, C425 100n, C426 100n → GND

OTB1-8
V3_3 → C431 100n, C432 100n, C433 100n, C434 100n, C427 100n, C428 100n, C429 100n, C430 100n → GND

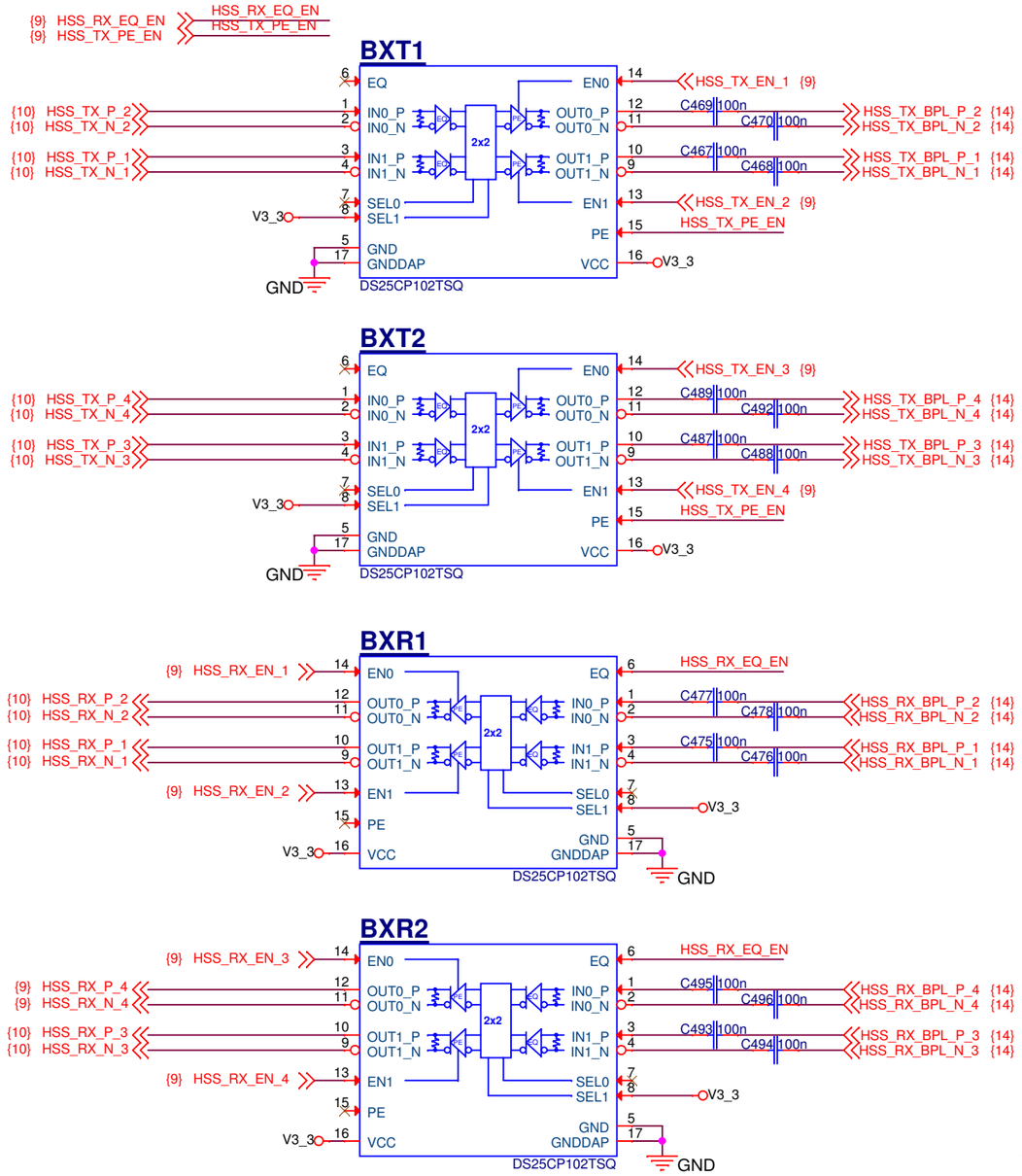
ITB1-8
V3_3 → C435 100n, C436 100n, C437 100n, C438 100n, C439 100n, C440 100n, C441 100n, C442 100n → GND

Title	Backplane buffers - MTCA.4 PORT 17-20 (M-LVDS triggers, clocks, gates)		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
			SHEET 16 OF 17

Backplane buffers - MTCA.4 PORT 12-15 (High Speed Serial)

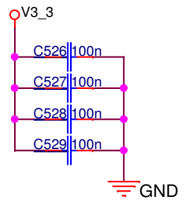
FPGA BANK GXB L0, Gigabit Transceivers

<< FPGA - Backplane >>



MTCA.4 backplane PORTs 12-15,

PE - Transmit Pre-Emphasis select pin. There is a 20k pulldown resistor on this pin
EQ - Receive Equalization select pin. There is a 20k pulldown resistor on this pin.
SEL0, SEL1 - Switch configuration pins. There is a 20k pulldown resistor on this pin.



Title: Backplane buffers - MTCA.4 PORT 12-15 (High Speed Se			
Size: A3	Type: SE	DWG.NO. CSL_FTRN_AMC	REV. A
		SHEET 17 OF 17	