FAIR Timing Receiver AMC form factor - CSL_FTRN_AMC
Single width, mid-height

SHEET	TITLE
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3	Power Tree
4	POWER DC-DC
5	POWER LDOs, FPGA BYPASS
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11	IO blocks 1-4
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13	IPMI MMC
14	AMC BACKPLANE PLUG
15	Backplane buffers - MTCA.4 TCLK A-D, Libera B triggers
16	Backplane buffers - MTCA.4 PORTs 17-20
17	Backplane buffers - MTCA.4 PORTs 12-15

DATE	REVISION DESCRIPTION	DRAWN	REV
01.09.2014	Initial version	dslavinec	A
19.09.2014	Flattened IO blocks	dslavinec	A
02.12.2014	Updates after QA review	dslavinec	A
16.04.2015	Added ADC clock generation and trigger signals to backplane, moved LVTTL_CLK, nRES and FPGA_RES to different FPGA pins	dslavinec	A
23.07.2015	removed ADC clocking page, only one set of triggers to backplane kept, incorporated changes from PMC (LED driving), added power mux for MMC	dslavinec	A
17.08.2015	added sheet 15 with MTCA.4 triggers and clocks to/from backplane	dslavinec	A
01.10.2015	MTCA.4 out clocks not connected to clk outputs, backplane buffers enable signals connected only to FPGA	dslavinec	A
27.11.2015	MTCA.4 connections to backplane finished, MMC PGOOD modified, relevant updates from PMC, MMC reset modified	dslavinec	A
09.12.2015	MTCA.4 HSS connections (backplane ports 12-15) moved from FPGA GXB banks to LVDS IOs	dslavinec	A
16.12.2015	libera triggers, MTCA.4 tclk and mlvdios moved to top FPGA banks	dslavinec	A
16.06.2016	LTM4620 replaced with LTM4619, FPGA core voltage increased to 1.15V, different TCLK buffers, larger LED resistors, replaced IO TVS	dslavinec	A
26.07.2017	one LTM4619 reverted back to LTM4620, added resistors for LTM mode configuration, modified JTAG chain connections, added JTAG switch indicator, WR/STATUS LEDs replaced with 90deg, WR and OSC clk lines back to AC-coupling	dslavinec	A

Value	Capatitors used
12p	0402, 50V, C0G, 1%
22p	0402, 50V, C0G, 1%
10n	0402, 25V, X7R, 10%
100n	0402, 25V, X7R, 10%
1u	0603, 16V, X7R, 10%
2.2u	1210, 100V, X7R, 10%
10u	1210, 25V, X7R, 10%
22u	1210, 10V, X7R, 10%
100u	1210, 10V, X5R, 20%

All resistors are SMD 0402, 63mW, 1% except where marked differently.

Components marked DNP (Do Not Place) are foreseen for testing purposes and should NOT be placed.

TOP layer

FM1 FIDUCIAL FM2 FIDUCIAL FM3 FIDUCIAL

BOTTOM layer

FM4 FIDUCIAL FM5 FIDUCIAL FM6 FIDUCIAL

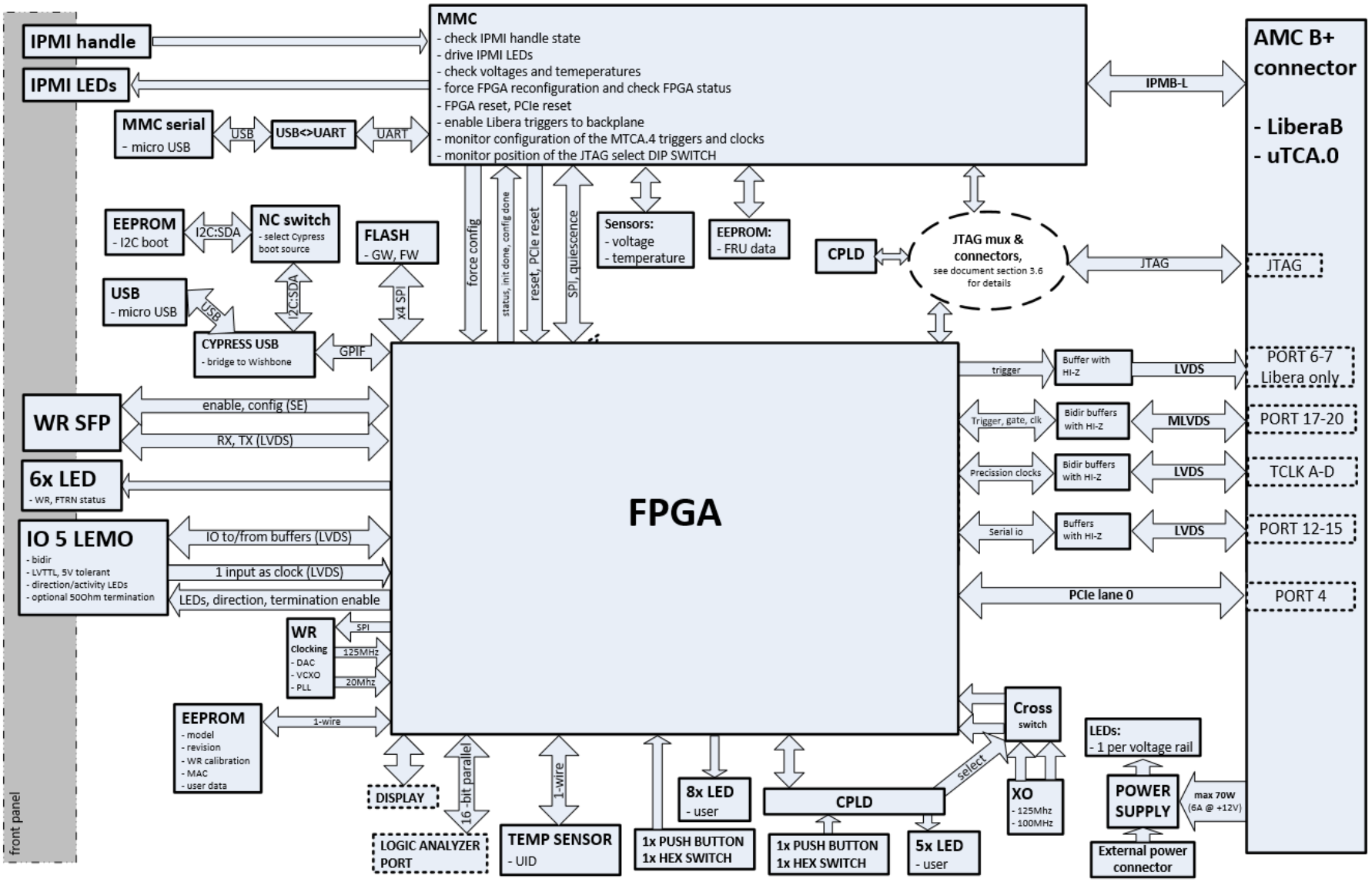
DRAWN	Dušan Slavinec		01.09.2014
CHECKED	-		
APPROVED	-		

Title

Size A3 | Type SE | DWG.NO. CSL_FTRN_AMC | REV. A

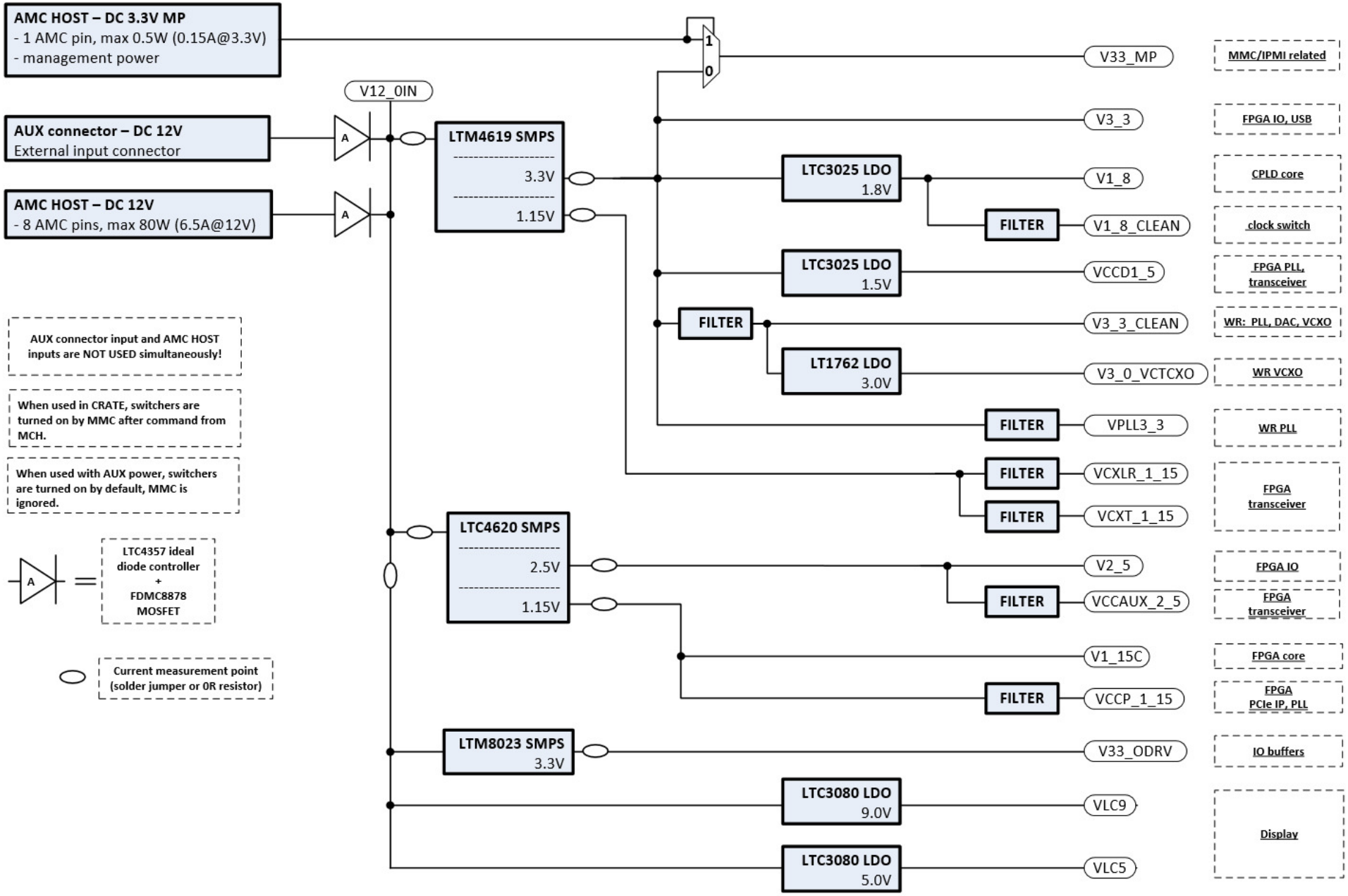
SHEET 1 OF 17

Block Diagram - FTRN, MMC



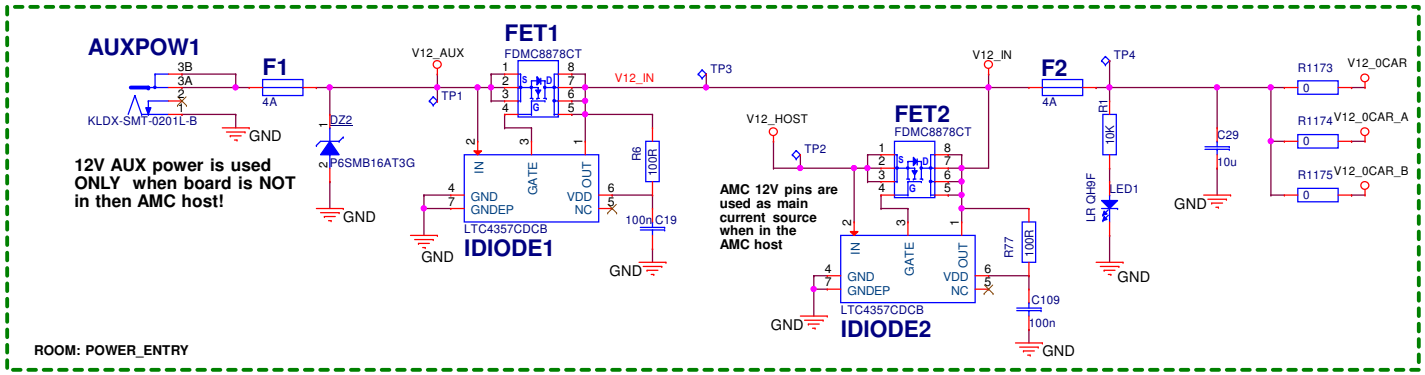
Title: Block Diagram - FTRN, MMC			
Size: A3	Type: SE	DWG.NO. CSL_FTRN_AMC	REV. A
			SHEET 2 OF 17

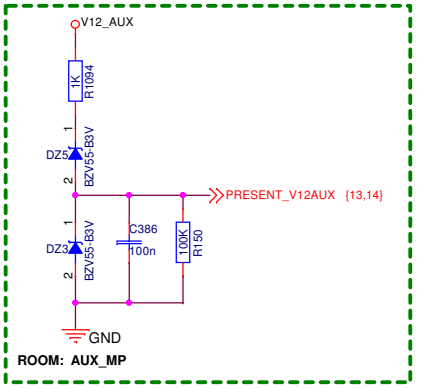
Power tree block scheme



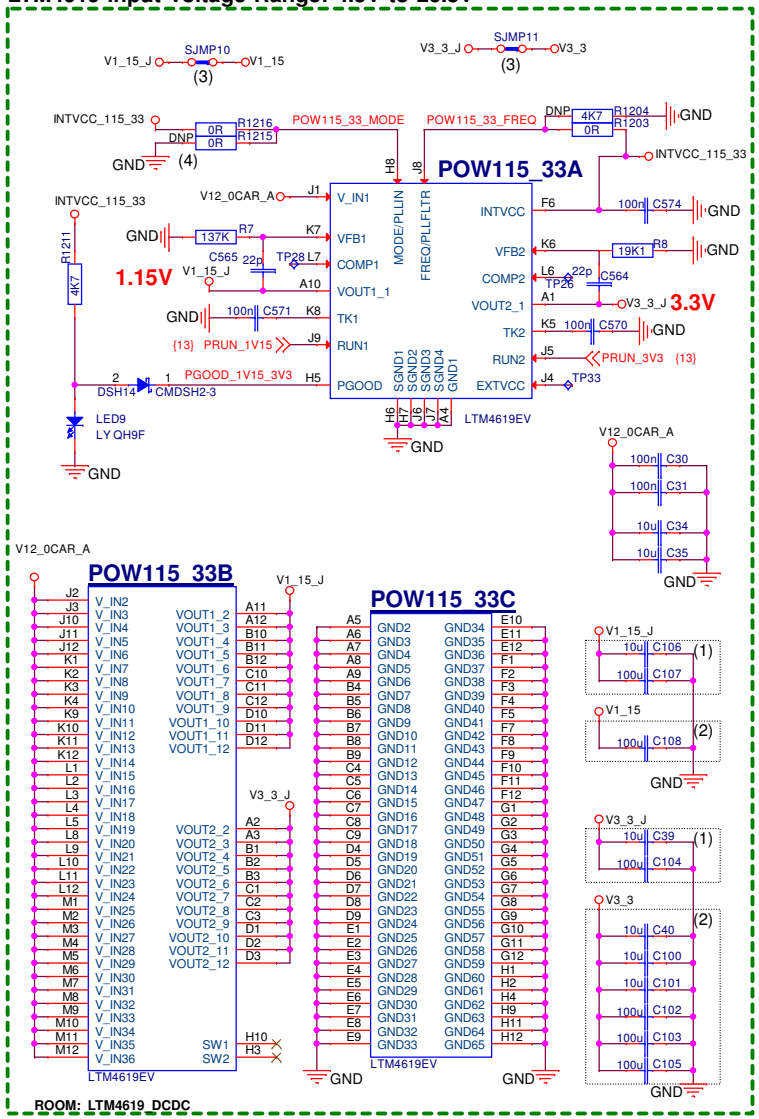
Title	Power tree block scheme		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
			SHEET 3 OF 17

Power entry and main DCDC power regulators

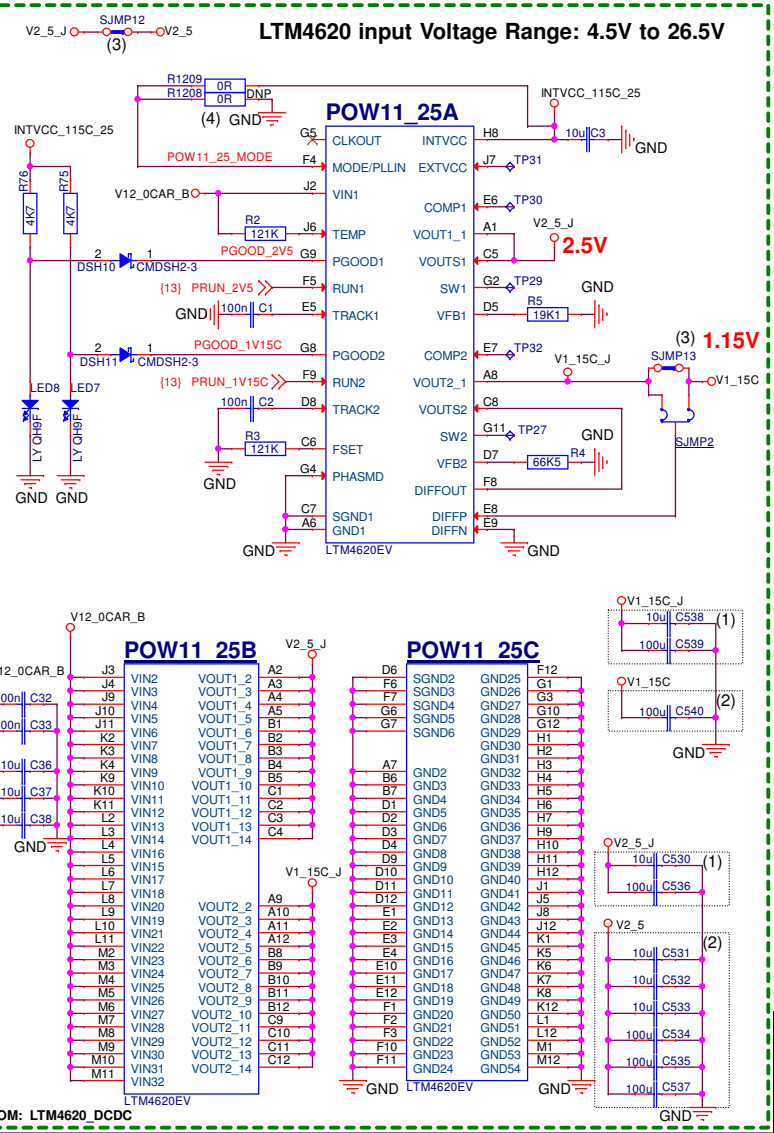


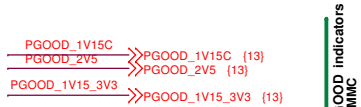


LTM4619 input Voltage Range: 4.5V to 26.5V



LTM4620 input Voltage Range: 4.5V to 26.5V





(1) - place capacitors on the regulator outputs

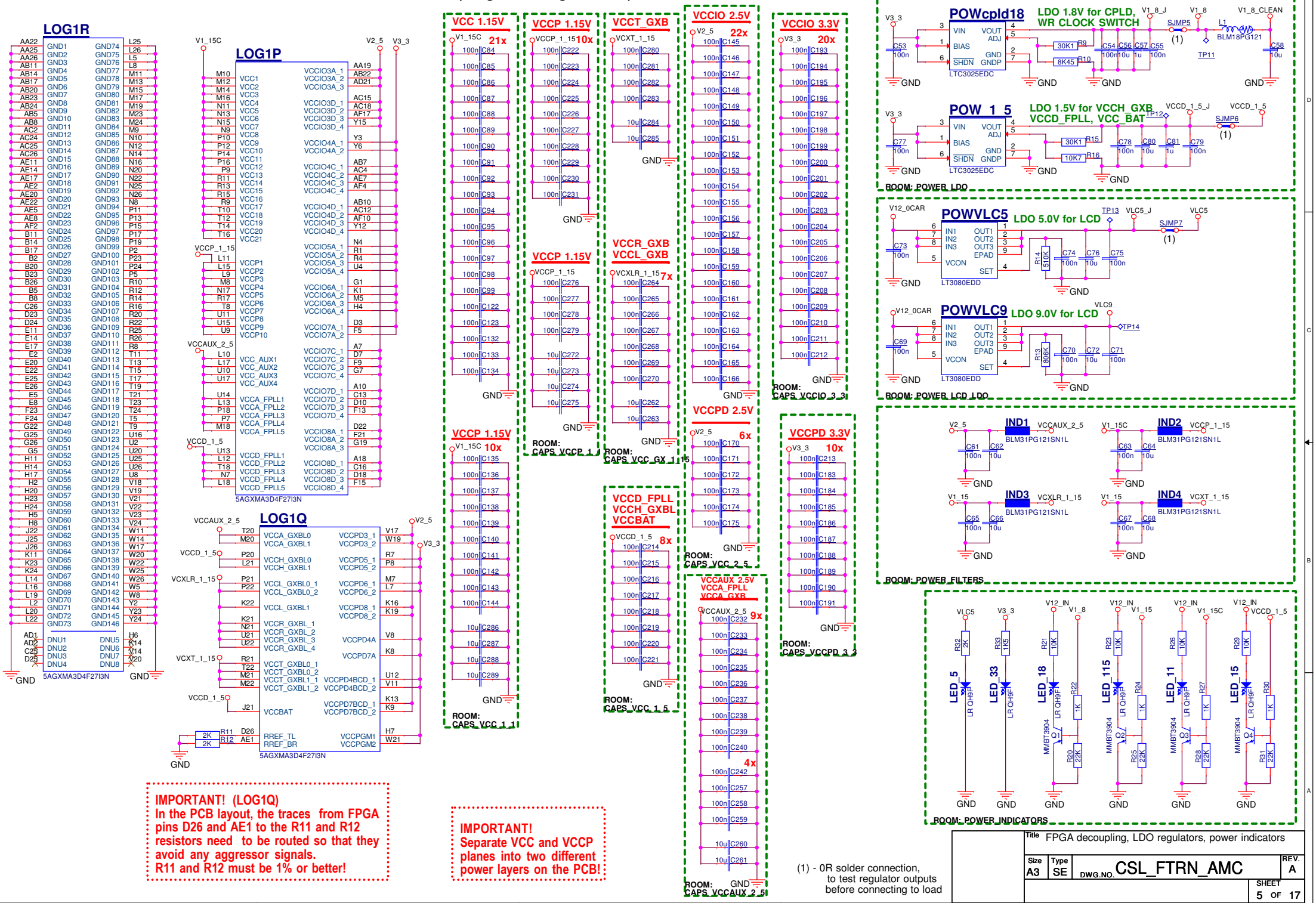
(2) - place capacitors away from the regulator outputs

(3) - solder jumper, to test power regulator outputs before powering FPGA and current measurement

(4) - None or only one resistor is placed to select converter mode (pulse-skipping, burst, continous)

Title: Power entry and main DCDC power regulators			
Size: A3	Type: SE	DWG.NO. CSL_FTRN_AMC	REV. A
			SHEET 4 OF 17

FPGA decoupling, LDO regulators, power indicators



Title	FPGA decoupling, LDO regulators, power indicators		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
			SHEET 5 OF 17

FPGA and CPLD JTAG, FPGA gateware FLASH, User Flash

JTAG signals flow :
C (USB connector) > R (resistor) > B (buffer) > P (PROG - CPLD) > F (FPGA) > B > C
or
BPL (backplane) > BB (backplane buffer) > BS (backplane JTAG switch) > R (resistor) > P (PROG - CPLD) > F (FPGA) > R > BS > BB > BPL

JTAG connector
(on the front panel if possible)

JTAGCON1

ZX62-B-5PA(11)

DTV1

TPD6E05U06RVZR

Straight-through Routing

FPGA/CPLD JTAG master select (DIP1, p14):
DIP1 = HI, FPGA/CPLD JTAG from backplane
DIP1 = LO, FPGA/CPLD JTAG from front panel connector

Parallel to USB connector JTAG signals are JTAG signals from JSW1 swtich (JTAG from backplane)

JTAG buffer and protection

DRV1

SN74LVC125ARGY

JTAG signal pull-ups

ROOM: FPGA_CPLD_JTAG_INPUT

LOG1O

5AGXMA3D4F27I3N

ROOM: MEMORY

SPIFLASHX4_1

N25Q256A13EF840

ROM1

DS18B20U+

ROM2

DS28EC20P

1-wire

IC3

SN74LVC1G97DCK

Y = IN0 AND IN2

FPGA status to MMC

ROOM: PROG_CPLD

PROG1C

XC2C64A-7CPG56C

XOF1

ECS-2033-500-BN

PROG1A

XC2C64A-7CPG56C

PROG1B

XC2C64A-7CPG56C

RST1

TPS3823-33DBVT

to PROG1C (pin C3)

RST2

TPS3823-33DBVT

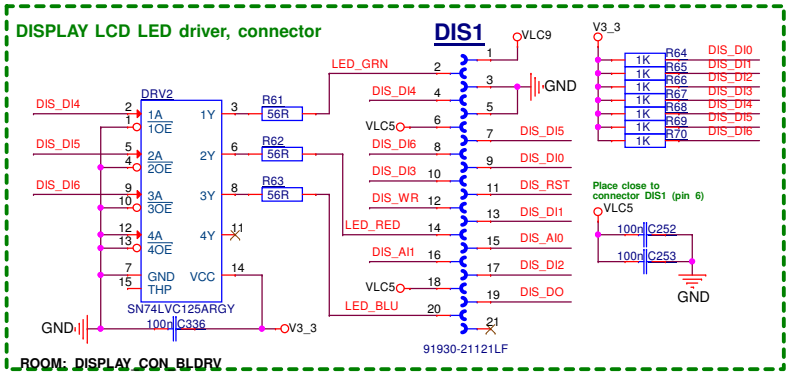
to LOG1D (pin AC7)

from PROG1C (pin F1)

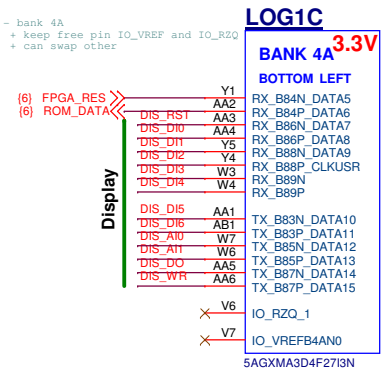
Title	FPGA and CPLD JTAG, FPGA gateware FLASH, User Flash		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
			SHEET 6 OF 17

User interface - USB, Display, push buttons, HEX switch, LEDs

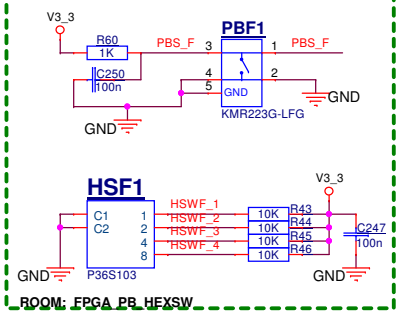
DISPLAY LCD LED driver, connector



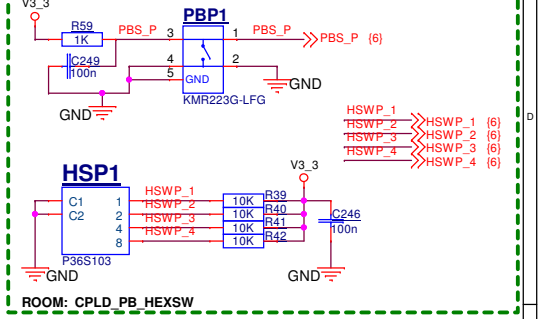
LOG1C



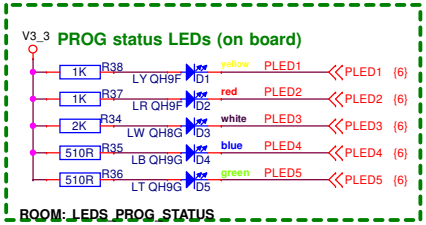
FPGA Push Button and HEX switch



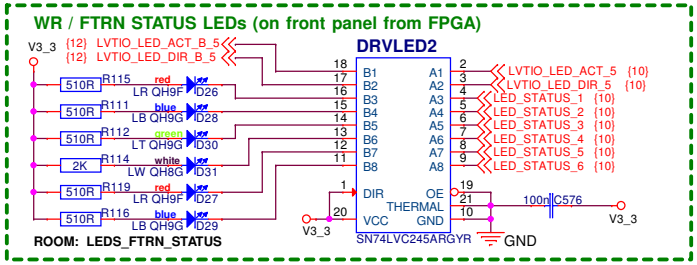
CPLD Push Button and HEX switch



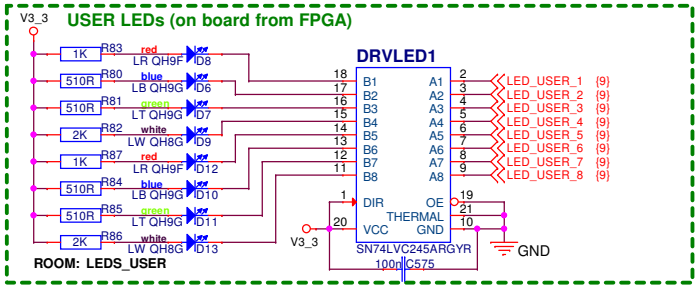
PROG status LEDs (on board)



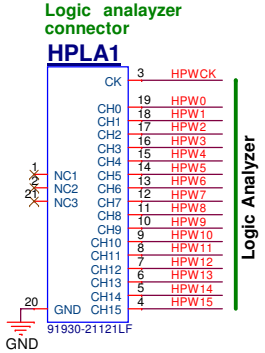
WR / FTRN STATUS LEDs (on front panel from FPGA)



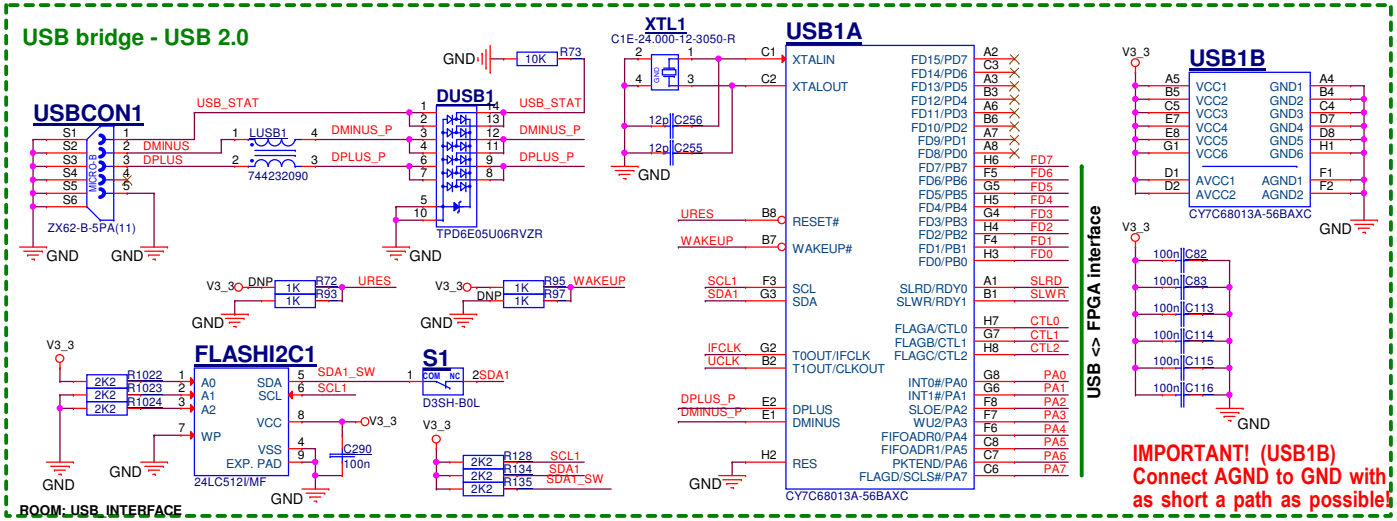
USER LEDs (on board from FPGA)



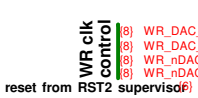
Logic analyzer connector



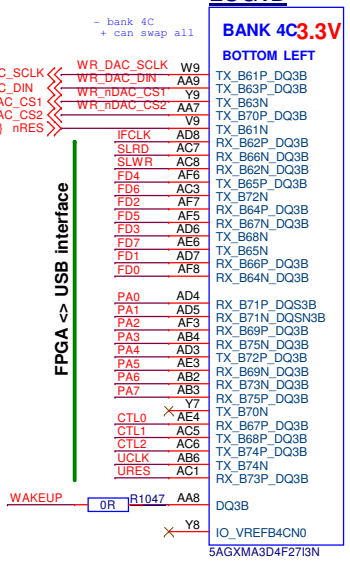
USB bridge - USB 2.0



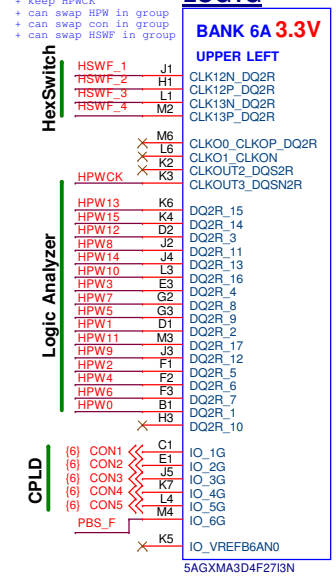
WR clk control



LOG1D

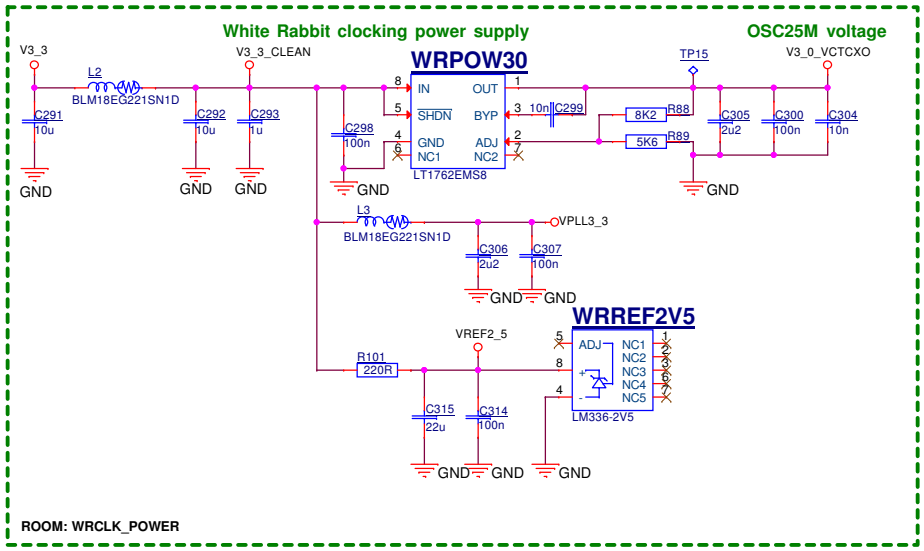


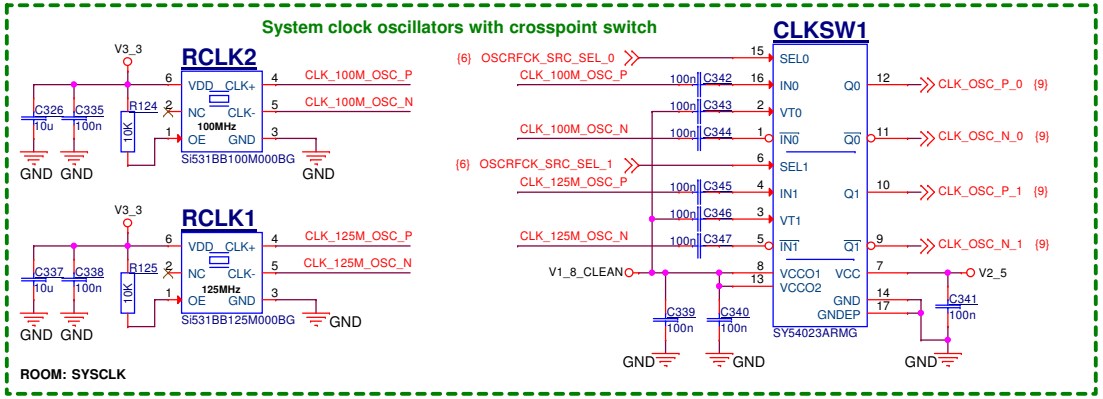
LOG1G

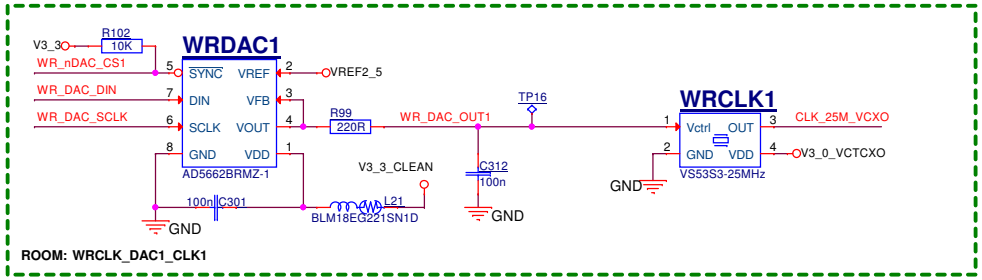


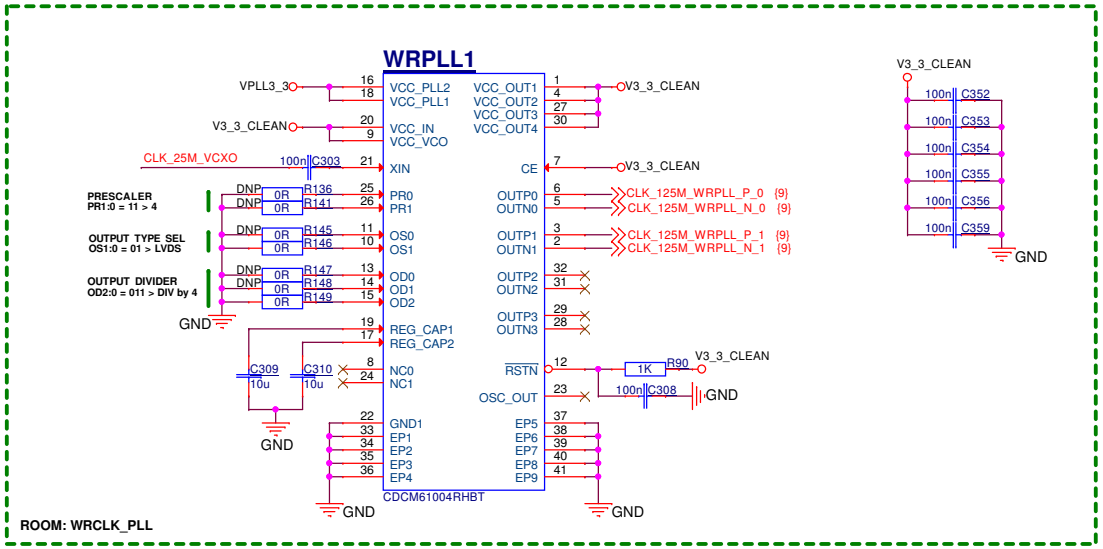
Title	User interface - USB, Display, push buttons, HEX switch, LEDs		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
			SHEET 7 OF 17

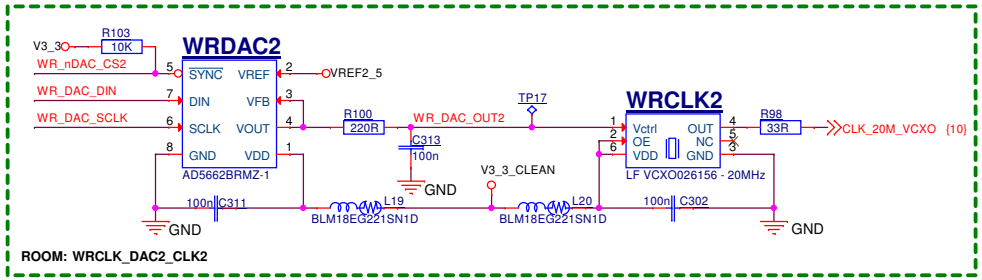
Clocking: White Rabbit DAC, oscillators, PLL ; System clocks and clock crosspoint switch











Title	Clocking: White Rabbit DAC, oscillators, PLL ; System clocks and clock crosspoint switch		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
			SHEET 8 OF 17

Fiber SFP, PCIe <> FPGA connections

IMPORTANT!
Hi speed Gigabit lines
100R differential

SFP1

V3_3, L4 (BLM18PG121SN1D), VCCT
C294 10u, C316 100n, C317 100n, C295 10u, C296 10u, C318 100n — GND

V3_3, L5 (BLM18PG121SN1D), VCCR
C319 100n, C297 10u, C320 10u, C321 100n — GND

V2_5
10K R104 SFP_MOD0
10K R105 SFP_MOD1
10K R106 SFP_MOD2
10K R107 SFP_TX_FAULT
10K R108 SFP_LOS
1K R109 SFP_TX_DIS
GND

SFP_TX_FAULT	2	TXFAULT	
	3	TXDIS	SFP_TX_DIS
SFP_RXD_N	12	RD-	
SFP_RXD_P	13	RD+	
	19	TD-	SFP_TXD_N
	18	TD+	SFP_TXD_P
SFP_LOS	8	LOS	
	6	MOD-DEF0	SFP_MOD0
	5	MOD-DEF1	SFP_MOD1
	4	MOD-DEF2	SFP_MOD2
	7	RATE SELECT	R110 1K → V3_3
VCCT	16	VCC_T	
VCCR	15	VCC_R	
	1, 17, 20	VEE_T1, VEE_T2, VEE_T3	GND
	9, 10, 11, 14	VEE_R1, VEE_R2, VEE_R3, VEE_R4	GND
	21, 22, 23, 24, 25, 26, 27	cage1, cage2, cage3, cage4, cage5, cage6, cage7	
	31, 30, 29, 28	cage11, cage10, cage9, cage8	

FACE_PLATE, FACE_PLATE

1367073-1

I2C addresses:
1010000X (A0h) : specs
1010001X (A2h) : diagnostics

ROOM: SFP

LOG1N

BANK GXB_L1
UPPER RIGHT

SFP_RXD_N	K25	RX_L6N_REFCLK
SFP_RXD_P	K26	RX_L6P_REFCLK
	H25	RX_L7N_REFCLK
	H26	RX_L7P_REFCLK
	F25	RX_L8N_REFCLK
	F26	RX_L8P_REFCLK
SFP_TXD_N	J23	TX_L6N
SFP_TXD_P	J24	TX_L6P
	G23	TX_L7N
	G24	TX_L7P
	E23	TX_L8N
	E24	TX_L8P
CLK_125M_WRPLL_C_N_1	N19	L1_REFCLK2_LN
CLK_125M_WRPLL_C_P_1	N18	L1_REFCLK2_LP

GND — 0R R1167

5AGXMA3D4F27I3N

PCIe

{14} PCIE_L0_TX_C_N	100n C373	PCIE_L0_TX_N
{14} PCIE_L0_TX_C_P	100n C372	PCIE_L0_TX_P
{14} PCIE_L0_RX_N		PCIE_L0_RX_N
{14} PCIE_L0_RX_P		PCIE_L0_RX_P
{14} PCIE_CLK_N	100n C349	PCIe_CLK_C_N
{14} PCIE_CLK_P	100n C348	PCIe_CLK_C_P

AMC backplane PORT4
AMC FCLK

WR PLL 125 MHz

{8} CLK_125M_WRPLL_N_0	100n C370	CLK_125M_WRPLL_C_N_0
{8} CLK_125M_WRPLL_P_0	100n C369	CLK_125M_WRPLL_C_P_0
{8} CLK_125M_WRPLL_N_1	100n C368	CLK_125M_WRPLL_C_N_1
{8} CLK_125M_WRPLL_P_1	100n C367	CLK_125M_WRPLL_C_P_1

SYS OSC

{8} CLK_OSC_P_1	100n C577	CLK_OSC_C_P_1
{8} CLK_OSC_N_1	100n C578	CLK_OSC_C_N_1
{8} CLK_OSC_N_0	100n C350	CLK_OSC_C_N_0
{8} CLK_OSC_P_0	100n C351	CLK_OSC_C_P_0

LOG1L

- bank 8D
+ keep CLK_125M_WRPLL
+ can swap RX 47, 51, 53
+ can swap RX 54, 56, 58
+ can swap TX half

BANK 8D 2.5V
TOP CENTER

CLK_125M_WRPLL_C_N_0	H15	RX_T45N_CLK19N_DQ3T
CLK_125M_WRPLL_C_P_0	G15	RX_T45P_CLK19P_DQ3T
{15} TCLK_IN_N_1	A16	RX_T51N_CLK17N_DQ3T
{15} TCLK_IN_P_1	A17	RX_T51P_CLK17P_DQ3T
	J16	RX_T49N_CLKO3_DQSN3T
	H16	RX_T49P_CLKO2_DQS3T
{15} TCLK_IN_N_2	C17	RX_T53N_CLK16N_DQ3T
{15} TCLK_IN_P_2	B16	RX_T53P_CLK16P_DQ3T
{12} LVTTL_CLK_N	C15	RX_T47N_CLK18N_DQ3T
{12} LVTTL_CLK_P	B15	RX_T47P_CLK18P_DQ3T
{15} TCLK_IN_N_3	C18	RX_T56N_DQ3T
{15} TCLK_IN_P_3	D17	RX_T56P_DQ3T
{15} TCLK_IN_N_4	H18	RX_T58N_DQ3T
{15} TCLK_IN_P_4	G18	RX_T58P_DQ3T
{17} HSS_RX_N_4	K17	RX_T54N_DQ3T
{17} HSS_RX_P_4	J17	RX_T54P_DQ3T
{15} TCLK_OUT_N_1	E15	TX_T48N
{15} TCLK_OUT_P_1	D15	TX_T48P_DQ3T
{15} TCLK_OUT_N_2	K15	TX_T46N
{15} TCLK_OUT_P_2	J15	TX_T46P_DQ3T
{15} TCLK_OUT_N_3	G16	TXT_50N_CLKO1,CLKON
{15} TCLK_OUT_P_3	F16	TX_T50P_CLKO0,CLKOP_DQ3T
{15} LIB_TRIG_N_0	E16	TX_T52N
{15} LIB_TRIG_P_0	D16	TX_T52P_DQ3T
{15} LIB_TRIG_N_1	K18	TX_T55N
{15} LIB_TRIG_P_1	J18	TX_T55P_DQ3T
{15} LIB_TRIG_N_2	A19	TX_T59N
{15} LIB_TRIG_P_2	B18	TX_T59P_DQ3T
{15} LIB_TRIG_N_3	F18	TX_T57N
{15} LIB_TRIG_P_3	E18	TX_T57P_DQ3T
	F17	DQ3T
	G17	IO_VREFB8DN0

5AGXMA3D4F27I3N

MTRIG to BPL Libera PlatformB

LOG1K

- bank 8A
+ keep CLK_OSC pins
+ keep n.c.
+ can swap others

BANK 8A 2.5V
TOP RIGHT

		RX_T79N
		RX_T79P
		RX_T81N_CLK23N
{17} HSS_TX_EN_3	A20	RX_T81P_CLK23P
NC (CLK isolation)	C21	RX_T83N_CLK22N
NC (CLK isolation)	B21	RX_T83P_CLK22P
{17} HSS_TX_EN_4	D20	RX_T84N_CLKOUT3
{17} HSS_RX_EQ_EN	C20	RX_T84P_CLKOUT2
{17} HSS_TX_PE_EN	A23	RX_T86N_CLK21N
NC (CLK isolation)	B22	RX_T86P_CLK21P
CLK_OSC_C_N_1	C22	RX_T88N_CLK20N
CLK_OSC_C_P_1	C23	RX_T88P_CLK20P
SFP_MOD0	D19	
SFP_MOD1	C19	
SFP_MOD2	B19	
SFP_TX_DIS	F19	TX_T80N
SFP_TX_FAULT	E19	TX_T80P
SFP_LOS	A22	TX_T82N
	A21	TX_T82P
{17} HSS_RX_EN_1	H21	TX_T85N_CLKO1,CLKON
{17} HSS_RX_EN_2	G21	TX_T85P_CLKO0,CLKOP
{17} HSS_RX_EN_3	J19	TX_T87N
{17} HSS_RX_EN_4	H19	TX_T87P
{17} HSS_TX_EN_1	E21	TX_T89N_RZQ_6
{17} HSS_TX_EN_2	D21	TX_T89P
NC (CLK isolation)	F20	IO_0K
	G20	IO_VREFB8AN0

5AGXMA3D4F27I3N

LOG1F

- bank 5A
+ keep CLK pins free
+ can swap others

BANK 5A 3.3V
LOWER LEFT

	N1	CLK14N_DQ1R
	M1	CLK14P_DQ1R
	N3	CLK15N_DQ1R
	N2	CLK15P_DQ1R
{7} LED_USER_1	P1	DQ1R_2
{7} LED_USER_2	T2	DQ1R_8
{7} LED_USER_3	V2	IO_7F
{7} LED_USER_4	W2	DQ1R_18
{7} LED_USER_5	T1	DQ1R_7
{7} LED_USER_6	U1	DQ1R_12
{7} LED_USER_7	V1	DQ1R_14
{7} LED_USER_8	W1	DQ1R_17
	T3	DQ1R_9
	T6	DQ1R_10
	T7	DQ1R_11
{13} MMC_PCIE_EN	R6	DQ1R_6
{13} FPGA2MMC_INT	U5	DQ1R_13
{13} MMC2FPGA_USR_1	R3	DQ1R_5
{13} MMC2FPGA_USR_2	V4	DQ1R_15
{13} MMC_SPI0_SCK	V5	DQ1R_16
{13} MMC_SPI0_MISO	N5	DQ1R_1
{13} MMC_SPI0_MOSI	R2	DQ1R_4
{13} #MMC_SPI0_SEL_FPGA		
	N6	IO_1F
	P4	IO_2F
	P6	IO_3F
	R5	IO_4F
	T4	IO_5F
	U6	IO_6F
	P3	DQ1R_3
	U3	DQSN1R
	V3	DQS1R
	U7	IO_VREFB5AN0

1, when #MMC_SPI0_SEL_FPGA is LO, MMC_SPI0_MISO is driven by FPGA.
2, when #MMC_SPI0_SEL_FPGA is HI, FPGA pin on MMC_SPI0_MISO must be HI-Z!

{13} MMC_QUIESCE_OUT — 0R R227 — MMC_QUIESCE_OUT_R
{13} MMC_QUIESCE_IN — 0R R228 — MMC_QUIESCE_IN_R

MMC_QUIESCE_OUT - MMC notifies FPGA that AMC will be shut down
MMC_QUIESCE_IN - FPGA notifies MMC that FPGA is ready for shutdown

MMC_QUIESCE_IN — DNP — 0R R206 — MMC_QUIESCE_OUT

MMC or AUX power enables triggers to backplane but FPGA/SW can give veto.

5AGXMA3D4F27I3N

AMC PCIe <> FPGA

LOG1M

BANK GXB_L0
LOWER RIGHT

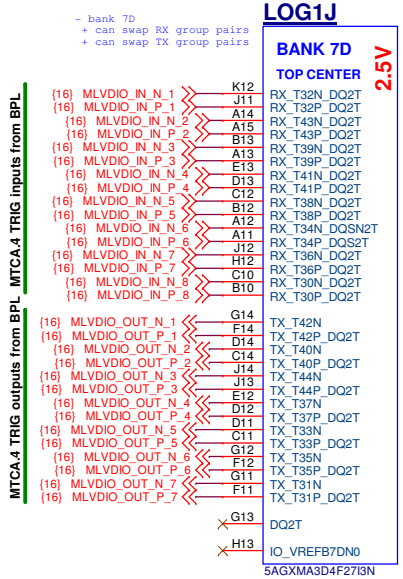
PCIE_L0_RX_N	AB25	RX_L0N_REFCLK
PCIE_L0_RX_P	AB26	RX_L0P_REFCLK
	Y25	RX_L1N_REFCLK
	Y26	RX_L1P_REFCLK
	V25	RX_L2N_REFCLK
	V26	RX_L2P_REFCLK
	T25	RX_L3N_REFCLK
	T26	RX_L3P_REFCLK
	P25	RX_L4N_REFCLK
	P26	RX_L4P_REFCLK
	M25	RX_L5N_REFCLK
	M26	RX_L5P_REFCLK
PCIE_L0_TX_N	AA23	TX_L0N
PCIE_L0_TX_P	AA24	TX_L0P
	W23	TX_L1N
	W24	TX_L1P
	U23	TX_L2N
	U24	TX_L2P
	R23	TX_L3N
	R24	TX_L3P
	N23	TX_L4N
	N24	TX_L4P
	L23	TX_L5N
	L24	TX_L5P
PCIe_CLK_C_N	U19	REFCLK0_LN
PCIe_CLK_C_P	U18	REFCLK0_LP
CLK_OSC_C_N_0	R19	REFCLK1_LN
CLK_OSC_C_P_0	R18	REFCLK1_LP

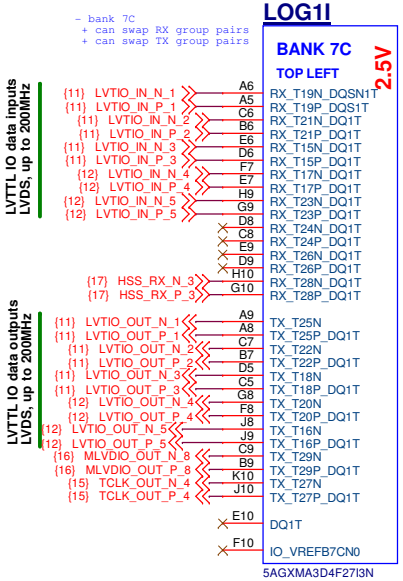
GND — 0R R1166

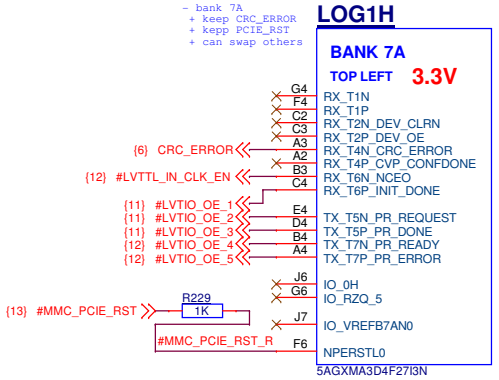
5AGXMA3D4F27I3N

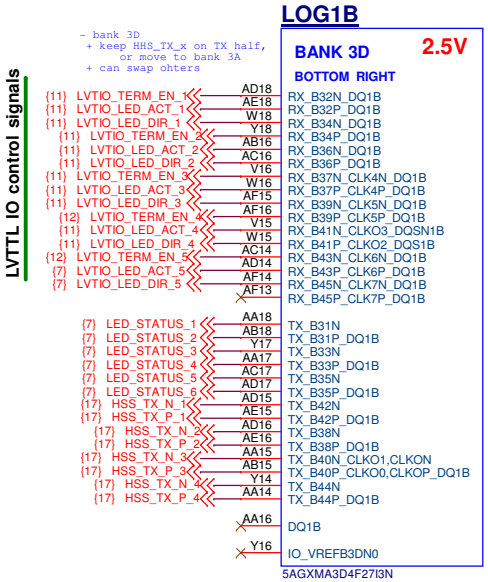
Title	Fiber SFP, PCIe <> FPGA connections		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
			SHEET 9 OF 17

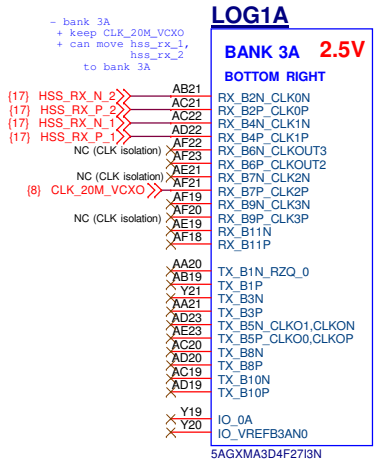
IO block power supply, FPGA <> IO block connections

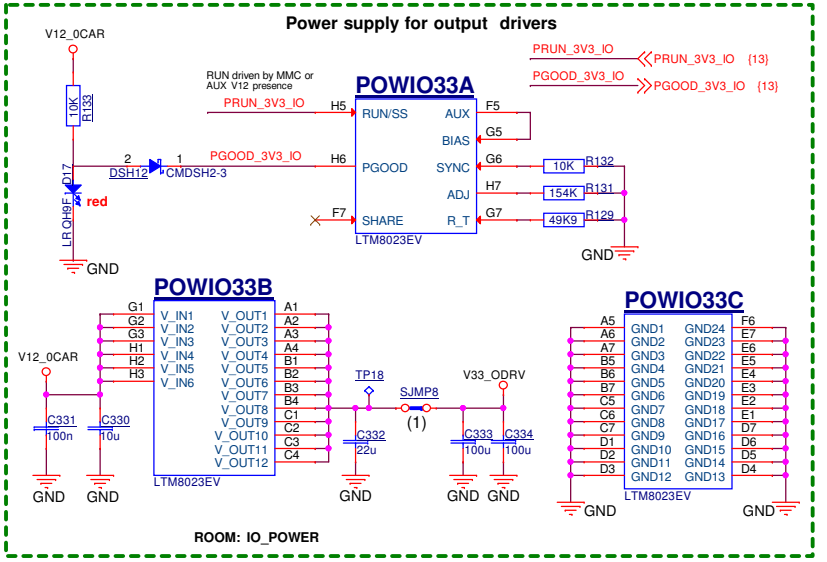


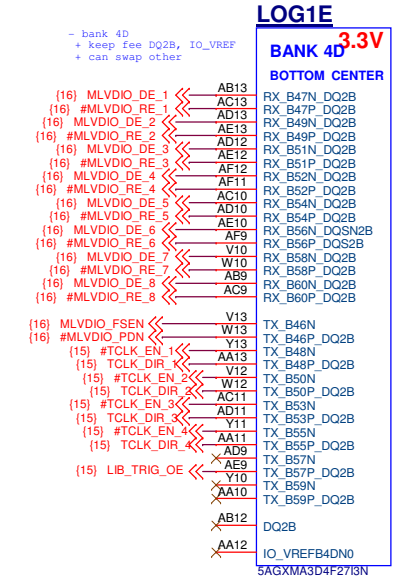








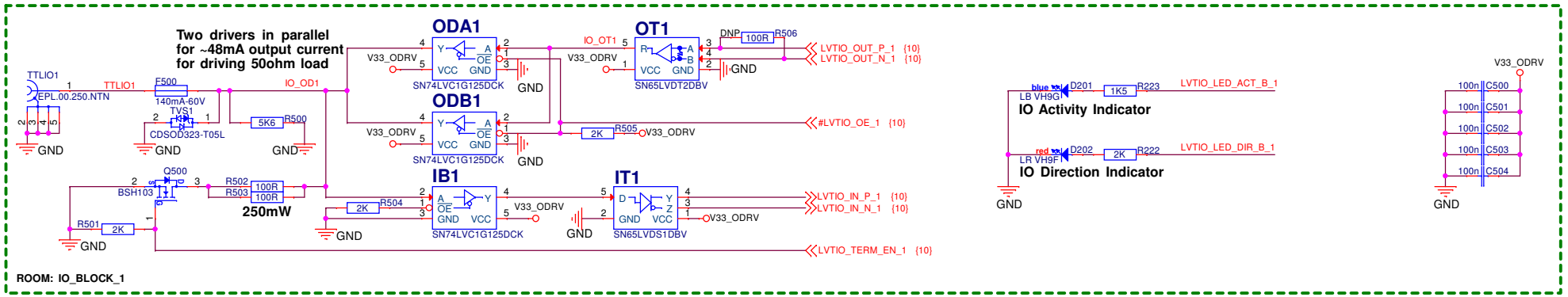


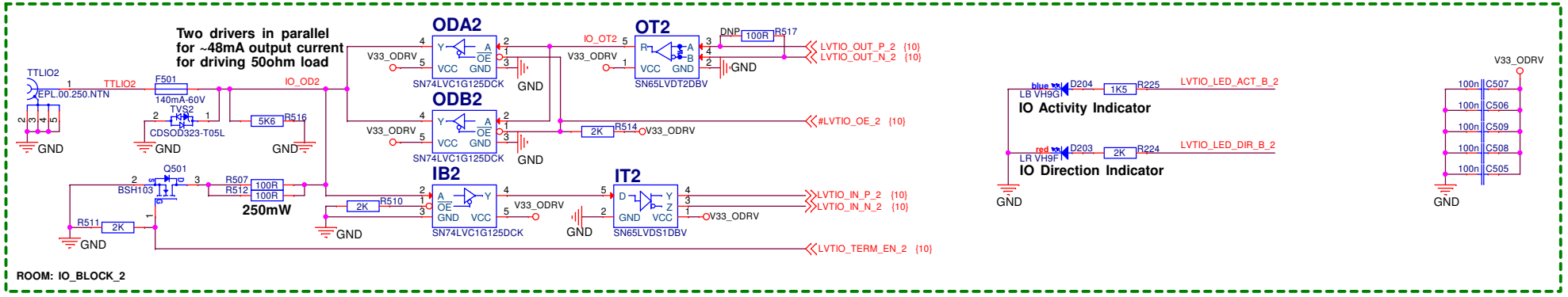


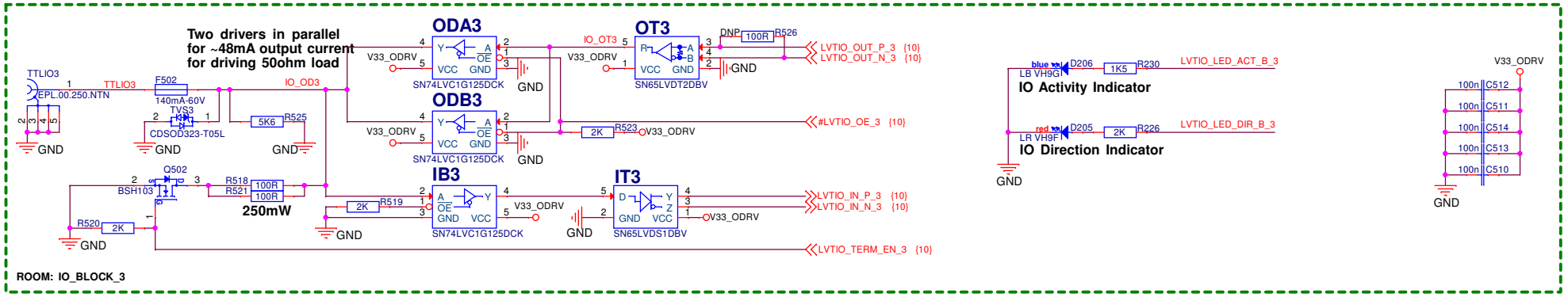
(1) - 0R solder connection,
to test regulator outputs
before connecting to load

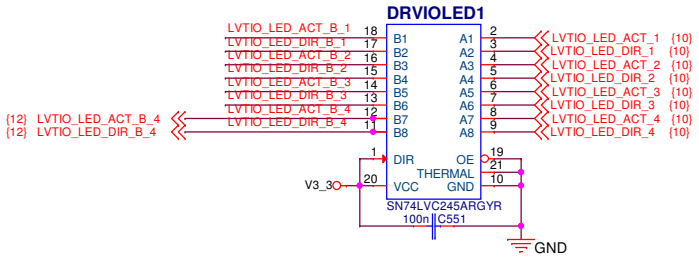
Title: IO block power supply, FPGA <> IO block connections			
Size: A3	Type: SE	DWG.NO. CSL_FTRN_AMC	REV. A
			SHEET 10 OF 17

LVTTL IO blocks 1-3



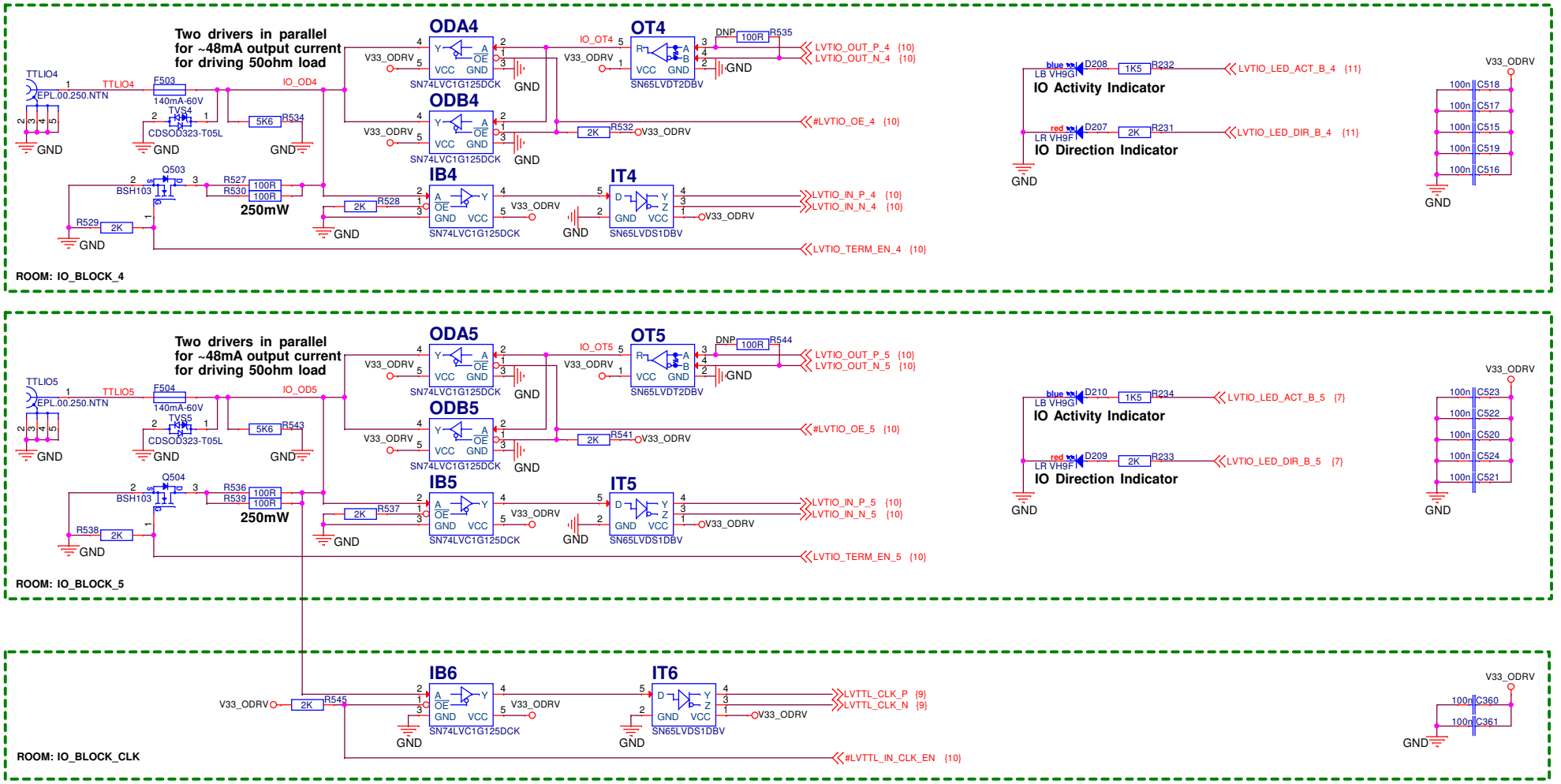






Title	LVTTL IO blocks 1-3		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
			SHEET 11 OF 17

LVTTL IO blocks 4-5, IO CLOCK input



Title	LVTTL IO blocks 4-5, IO CLOCK input		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
			SHEET 12 OF 17

MMC, IPMI

MMC user push button

PBM1

PBM2

#MMC_PB_2 used as MMC reset

ROOM: MMC_PBS_LEDS

MMC user LEDs

LR QH9F LT QH9G

PMX1

MP power MUX:
- in crate: V33_MP_BPL > 0.8V
  out = V33_MP_BPL
- not in crate, on AUX:
  V33_MP_BPL (0V) < 0.8V
  out = V3_3

TPS2112APW

JTAG1 MMC JTAG connector

M50-3600542

DTV2

TPD6E05U06RVZR

USB <> UART for MMC console (on the front panel if possible)

USBCON2

DUSB2

TPD6E05U06RVZR

IC1

FT230XQ

ROOM: MMC_USB

MMC FW FLASH

MMEM1

M25P80-VMN6P

MMC local I2C bus: - temp sensors, FRU EEPROM

TS1

TS2

LM73CIMK-0

MMEM2

24LC512I/MF

ROOM: MMC_TEMP_FRUMEM

Resistor dividers for voltage sensors

ROOM: MMC_VOLT_RED_DIV

MMC1A

LPC2138FBD64/01

MMC1B

LPC2138FBD64/01

JTRST# only from backplane, JTAG connector does not provide JTRST#

MMC1C

LPC2138FBD64/01

MRST1

TPS3823-33DBVT

ROOM: MMC_RST_EN

IC2

SN74LVC1G97DCK

MTCA Extractor handle switch

SW1

HDT0001

ROOM: MMC_HANDLE

MVREF1

LM336-2V5

XTL2

C1E-24.000-12-3050-R

IPMI/AMC status LEDs on the front panel

QH - top (green, white), VH - side (blue, red)

ROOM: MMC_IPMI_LEDS

Title	MMC, IPMI
Size	A3
Type	SE
DWG.NO.	CSL_FTRN_AMC
REV.	A
SHEET	13 OF 17

AMC backplane plug

JTAG signals length from the AMCPLG1 connector to the JDRVx buffers is 100mm MAX!!!

AMCPLG1

TB-16-23-170-1301-000

	1	GND28	GND56	170	
AMC_PWR8	2	PWR8	TDI	169	JTDI_AMC_PLG
#PS1	3	PS1#	TDO	168	JTDO_AMC_PLG
V33_MP_BPL	4	MP	TRST#	167	#JTRST_AMC_PLG
{13} IPMI_GA_0	5	GA0	TMS	166	JTMS_AMC_PLG
	6	ETH100R	TCLK	165	JTCK_AMC_PLG
	7	GND27	GND55	164	
AMC_PWR7	8	ETH100T	TX20+	163	MLVDIO_BPL_P_8 {16}
	9	PWR7	TX20-	162	MLVDIO_BPL_N_8 {16}
	10	GND26	GND54	161	
	11	TX0+	RX20+	160	MLVDIO_BPL_P_7 {16}
	12	TX0-	RX20-	159	MLVDIO_BPL_N_7 {16}
	13	GND25	GND53	158	
	14	RX0+	TX19+	157	MLVDIO_BPL_P_6 {16}
	15	RX0-	TX19-	156	MLVDIO_BPL_N_6 {16}
	16	GND24	GND52	155	
{13} IPMI_GA_1	17	GA1	RX19+	154	MLVDIO_BPL_P_5 {16}
AMC_PWR6	18	PWR6	RX19-	153	MLVDIO_BPL_N_5 {16}
	19	GND23	GND51	152	
	20	TX1+	TX18+	151	MLVDIO_BPL_P_4 {16}
	21	TX1-	TX18-	150	MLVDIO_BPL_N_4 {16}
	22	GND22	GND50	149	
	23	RX1+	RX18+	148	MLVDIO_BPL_P_3 {16}
	24	RX1-	RX18-	147	MLVDIO_BPL_N_3 {16}
	25	GND21	GND49	146	
	26	GA2	TX17+	145	MLVDIO_BPL_P_2 {16}
{13} IPMI_GA_2	27	PWR5	TX17-	144	MLVDIO_BPL_N_2 {16}
AMC_PWR5	28	GND20	GND48	143	
	29	TX2+	RX17+	142	MLVDIO_BPL_P_1 {16}
	30	TX2-	RX17-	141	MLVDIO_BPL_N_1 {16}
	31	GND19	GND47	140	
	32	RX2+	TX16+	139	TCLK_BPL_P_3 {15}
	33	RX2-	TX16-	138	TCLK_BPL_N_3 {15}
	34	GND18	GND46	137	
	35	TX3+	RX16+	136	TCLK_BPL_P_4 {15}
	36	TX3-	RX16-	135	TCLK_BPL_N_4 {15}
	37	GND17	GND45	134	
	38	RX3+	TX15+	133	HSS_TX_BPL_P_4 {17}
	39	RX3-	TX15-	132	HSS_TX_BPL_N_4 {17}
	40	GND16	GND44	131	
{13} #IPMI_MMC_ENABLE	41	ENABLE#	RX15+	130	HSS_RX_BPL_P_4 {17}
AMC_PWR4	42	PWR4	RX15-	129	HSS_RX_BPL_N_4 {17}
	43	GND15	GND43	128	
{9} PCIE_L0_TX_C_P	44	TX4+	TX14+	127	HSS_TX_BPL_P_3 {17}
{9} PCIE_L0_TX_C_N	45	TX4-	TX14-	126	HSS_TX_BPL_N_3 {17}
	46	GND14	GND42	125	
{9} PCIE_L0_RX_P	47	RX4+	RX14+	124	HSS_RX_BPL_P_3 {17}
{9} PCIE_L0_RX_N	48	RX4-	RX14-	123	HSS_RX_BPL_N_3 {17}
	49	GND13	GND41	122	
	50	TX5+	TX13+	121	HSS_TX_BPL_P_2 {17}
	51	TX5-	TX13-	120	HSS_TX_BPL_N_2 {17}
	52	GND12	GND40	119	
	53	RX5+	RX13+	118	HSS_RX_BPL_P_2 {17}
	54	RX5-	RX13-	117	HSS_RX_BPL_N_2 {17}
	55	GND11	GND39	116	
{13} IPMB_L_SCL	56	SCL_L	TX12+	115	HSS_TX_BPL_P_1 {17}
AMC_PWR3	57	PWR3	TX12-	114	HSS_TX_BPL_N_1 {17}
	58	GND10	GND38	113	
{15} M2_TRIG_P_0	59	TX6+	RX12+	112	HSS_RX_BPL_P_1 {17}
{15} M2_TRIG_N_0	60	TX6-	RX12-	111	HSS_RX_BPL_N_1 {17}
	61	GND9	GND37	110	
{15} M2_TRIG_P_1	62	RX6+	TX11+	109	
{15} M2_TRIG_N_1	63	RX6-	TX11-	108	
	64	GND8	GND36	107	
{15} M2_TRIG_P_2	65	TX7+	RX11+	106	
{15} M2_TRIG_N_2	66	TX7-	RX11-	105	
	67	GND7	GND35	104	
{15} M2_TRIG_P_3	68	RX7+	TX10+	103	
{15} M2_TRIG_N_3	69	RX7-	TX10-	102	
	70	GND6	GND34	101	
{13} IPMB_L_SDA	71	SDA_L	RX10+	100	
AMC_PWR2	72	PWR2	RX10-	99	
	73	GND5	GND33	98	
{15} TCLK_BPL_P_1	74	CLK1+	TX9+	97	
{15} TCLK_BPL_N_1	75	CLK1-	TX9-	96	
	76	GND4	GND32	95	
{15} TCLK_BPL_P_2	77	CLK2+	RX9+	94	
{15} TCLK_BPL_N_2	78	CLK2-	RX9-	93	
	79	GND3	GND31	92	
{9} PCIE_CLK_P	80	CLK3+	TX8+	91	
{9} PCIE_CLK_N	81	CLK3-	TX8-	90	
	82	GND2	GND30	89	
#PS0	83	PS0#	RX8+	88	
AMC_PWR1	84	PWR1	RX8-	87	
	85	GND1	GND29	86	

GND GND

MTCA.4 bidirectional triggers, gates (DC-coupled, transceivers with 3-State outputs)

MTCA.4 bidir low jitter clocks TCLKC, TCLKD (AC-coupled, 3-state outputs)

MTCA.4 trasnceivers (AC-coupled, buffers with 3-State outputs)

Libera Module 2 TRIGGERS (DC-coupled, 3-state outputs)

MTCA.4 bidir low jitter clocks TCLKA, TCLKB (AC-coupled, 3-state outputs)

JDRV1

JTDO_AMC_PLG — R1168 33R — JTDO_AMC

V33_MP — VCC, GND — SN74LVC1G125DCK — 100n C391 — GND

JDRV2

JTDI_AMC_PLG	1A	1Y	JTDI_AMC
	1OE		
#JTRST_AMC_PLG	2A	2Y	#JTRST_AMC
	2OE		
JTMS_AMC_PLG	3A	3Y	JTMS_AMC
	3OE		
JTCK_AMC_PLG	4A	4Y	JTCK_AMC
	4OE		
	Thermal		
	GND	VCC	V33_MP

SN74LVC125ARGY — 100n C388 — GND

V33_MP — 10K R113 JTDI_AMC_PLG — 10K R118 JTMS_AMC_PLG — 10K R117 JTCK_AMC_PLG — 10K R120 #JTRST_AMC_PLG — GND

JTAG swithc for routing Backplane JTAG to MMC or CPLD/FPGA. Monitored by MMC.

JSW1

MAX4948ETG+

GND	23	6COM	6NO 24 — GND
		6NC 1	
#JTRST_AMC	3	5COM	5NO 2
		5NC 4	#JTRST_MMC {13}
JTCK_AMC	7	4COM	4NO 8 — JTCK_SR {6}
		4NC 9	JTCK_MMC {13}
JTMS_AMC	11	3COM	3NO 10 — JTMS_SR {6}
		3NC 12	JTMS_MMC {13}
JTDI_AMC	16	2COM	2NO 17 — JTDI_SR {6}
		2NC 15	JTDI_MMC {13}
JTDO_AMC	20	1COM	1NO 19 — JTDO_RS {6}
			1NC 18 — JTDO_MMC {13}
{4,13} PRESENT_V12AUX	5	EN	H CB L — 14 JTAGSW_SEL
	6	GND1	CB = L : BPL > MMC
	21	GND2	CB = H : BPL > CPLD/FPGA
	25	Thermal	N.C. 13 / VCC 22

JTAG from BACKPLANE

JTAG to MMC/FPGA-CPLD

V33_MP — 100n C251 — GND

V33_MP — 10K R1124 — DIP1 MCEMR-02-T — JTAGSW_SEL — JTAGSW_SEL {6,13} — GND

V33_MP — R1227 1K — D211 red LR VH9F — Place LED on front panel!

Q505 BSH103 — JTAGSW_SEL

GND

V12_HOST

BLM18PG221SN1D	L8	AMC_PWR1
BLM18PG221SN1D	L9	AMC_PWR2
BLM18PG221SN1D	L10	AMC_PWR3
BLM18PG221SN1D	L11	AMC_PWR4
BLM18PG221SN1D	L12	AMC_PWR5
BLM18PG221SN1D	L13	AMC_PWR6
BLM18PG221SN1D	L14	AMC_PWR7
BLM18PG221SN1D	L15	AMC_PWR8

V33_MP_BPL — C376 10u — C377 100n — GND

Management Power from MTCA backplane

#PS1 — DSH2 CMDSH2-3 — #PS0

AMC card presence detection. PS1 "shorted" to PS0 when card fully inserted into host.

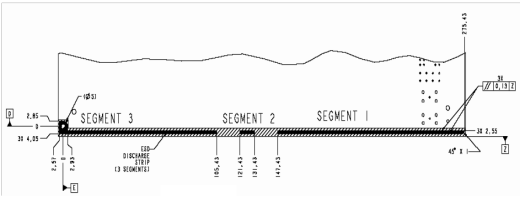
AMCESD1

BACKPLANE — SEG1 — 10M R182 — SEG2 — 10M R181 — GND — SEG3 — FACEPLATE — FACE_PLATE

ESD discharge strip

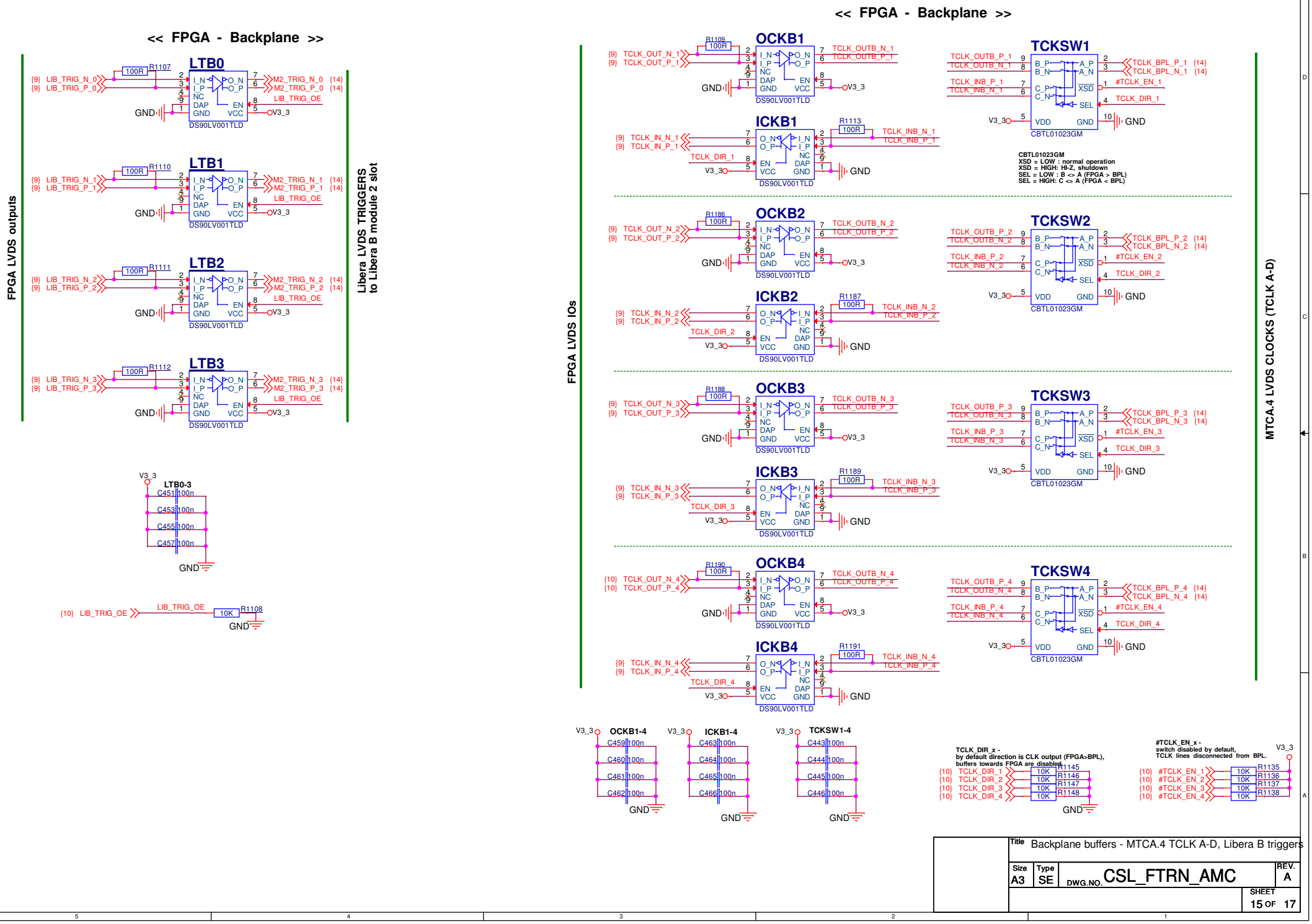
J1

1 — S1731-46R — 2 — FACE_PLATE — GND



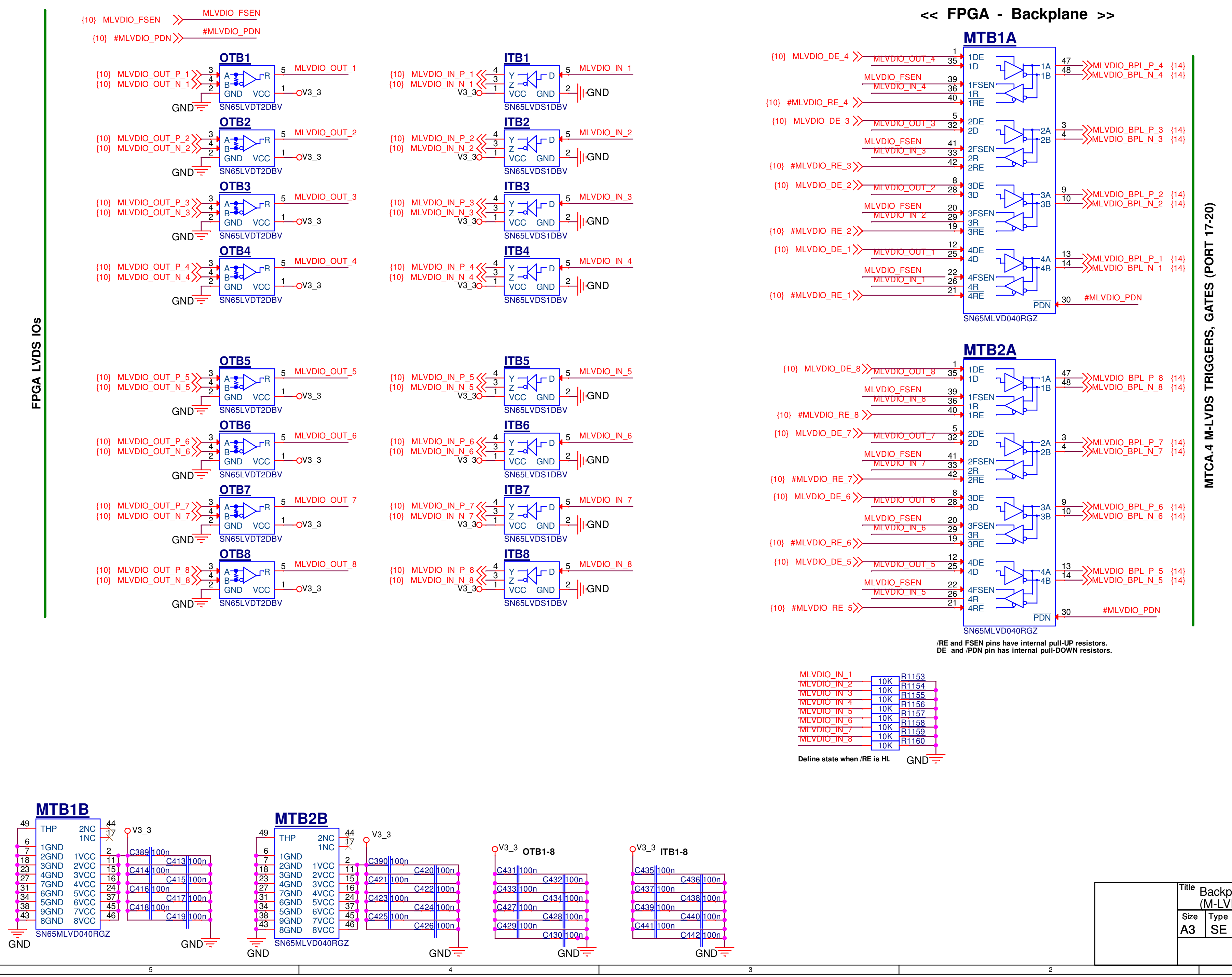
Title	AMC backplane plug		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
			SHEET 14 OF 17

Backplane buffers - MTCA.4 TCLK A-D, Libera B triggers



Title	Backplane buffers - MTCA.4 TCLK A-D, Libera B triggers		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
			SHEET 15 OF 17

Backplane buffers - MTCA.4 PORT 17-20 (M-LVDS triggers, clocks, gates)



Title	Backplane buffers - MTCA.4 PORT 17-20 (M-LVDS triggers, clocks, gates)
Size	A3
Type	SE
DWG.NO.	CSL_FTRN_AMC
REV.	A
SHEET	16 OF 17

Backplane buffers - MTCA.4 PORT 12-15 (High Speed Serial)

IMPORTANT!
Hi speed Gigabit lines
100R differential

<< FPGA - Backplane >>

FPGA BANK GXB L0, Gigabit Transceivers

MTCA.4 backplane PORTs 12-15,

{9} HSS_RX_EQ_EN
{9} HSS_TX_PE_EN
HSS_RX_EQ_EN
HSS_TX_PE_EN

BXT1

DS25CP102TSQ

EQ		EN0	HSS_TX_EN_1 {9}
{10} HSS_TX_P_2	IN0_P	OUT0_P	C469 100n → HSS_TX_BPL_P_2 {14}
{10} HSS_TX_N_2	IN0_N	OUT0_N	C470 100n → HSS_TX_BPL_N_2 {14}
{10} HSS_TX_P_1	IN1_P	OUT1_P	C467 100n → HSS_TX_BPL_P_1 {14}
{10} HSS_TX_N_1	IN1_N	OUT1_N	C468 100n → HSS_TX_BPL_N_1 {14}
V3_3	SEL0	EN1	HSS_TX_EN_2 {9}
V3_3	SEL1	PE	HSS_TX_PE_EN
GND	GND	VCC	V3_3
GND	GNDDAP		

BXT2

DS25CP102TSQ

EQ		EN0	HSS_TX_EN_3 {9}
{10} HSS_TX_P_4	IN0_P	OUT0_P	C489 100n → HSS_TX_BPL_P_4 {14}
{10} HSS_TX_N_4	IN0_N	OUT0_N	C492 100n → HSS_TX_BPL_N_4 {14}
{10} HSS_TX_P_3	IN1_P	OUT1_P	C487 100n → HSS_TX_BPL_P_3 {14}
{10} HSS_TX_N_3	IN1_N	OUT1_N	C488 100n → HSS_TX_BPL_N_3 {14}
V3_3	SEL0	EN1	HSS_TX_EN_4 {9}
V3_3	SEL1	PE	HSS_TX_PE_EN
GND	GND	VCC	V3_3
GND	GNDDAP		

BXR1

DS25CP102TSQ

{9} HSS_RX_EN_1	EN0	EQ	HSS_RX_EQ_EN
{10} HSS_RX_P_2	OUT0_P	IN0_P	C477 100n → HSS_RX_BPL_P_2 {14}
{10} HSS_RX_N_2	OUT0_N	IN0_N	C478 100n → HSS_RX_BPL_N_2 {14}
{10} HSS_RX_P_1	OUT1_P	IN1_P	C475 100n → HSS_RX_BPL_P_1 {14}
{10} HSS_RX_N_1	OUT1_N	IN1_N	C476 100n → HSS_RX_BPL_N_1 {14}
{9} HSS_RX_EN_2	EN1	SEL0	V3_3
	PE	SEL1	V3_3
V3_3	VCC	GND	GND
		GNDDAP	

BXR2

DS25CP102TSQ

{9} HSS_RX_EN_3	EN0	EQ	HSS_RX_EQ_EN
{9} HSS_RX_P_4	OUT0_P	IN0_P	C495 100n → HSS_RX_BPL_P_4 {14}
{9} HSS_RX_N_4	OUT0_N	IN0_N	C496 100n → HSS_RX_BPL_N_4 {14}
{10} HSS_RX_P_3	OUT1_P	IN1_P	C493 100n → HSS_RX_BPL_P_3 {14}
{10} HSS_RX_N_3	OUT1_N	IN1_N	C494 100n → HSS_RX_BPL_N_3 {14}
{9} HSS_RX_EN_4	EN1	SEL0	V3_3
	PE	SEL1	V3_3
V3_3	VCC	GND	GND
		GNDDAP	

PE - Transmit Pre-Emphasis select pin. There is a 20k pulldown resistor on this pin
EQ - Receive Equalization select pin. There is a 20k pulldown resistor on this pin.
SEL0, SEL1 - Switch configuration pins. There is a 20k pulldown resistor on this pin.

V3_3
C526 100n
C527 100n
C528 100n
C529 100n
GND

Title	Backplane buffers - MTCA.4 PORT 12-15 (High Speed Serial)		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
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