White Rabbit

Dimitrios Lampridis

CERN BE-CO
Hardware and Timing section

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Besançon, 29 June 2017
What is White Rabbit?

- Renovation of accelerator’s control and timing
- Based on well-known technologies
- Open Hardware and Open Software with commercial support
- International collaboration
- Many users: CERN, GSI, KM3NET, cosmic ray detectors, metrology labs...
Why we use Open Hardware?

<table>
<thead>
<tr>
<th>Open</th>
<th>Commercial</th>
<th>Non-commercial</th>
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<tr>
<td>Winning combination. Best of both worlds.</td>
<td>Whole support burden falls on developers. Not scalable.</td>
<td></td>
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<td>Vendor lock-in.</td>
<td>Dedicated non-reusable projects.</td>
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- Get a design just the way we want it
- Peer review and design re-use
- Healthier relationship with companies
White Rabbit: an *extension* of Ethernet

- Standard Ethernet network
- Ethernet features (VLAN) & protocols (SNMP)
- High accuracy synchronization
- Reliable and low-latency Control Data
White Rabbit application examples

- CERN and GSI
White Rabbit application examples

- CERN and GSI
- HiSCORE: Gamma & Cosmic-Ray experiment
White Rabbit application examples

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- The Large High Altitude Air Shower Observatory
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- KM3NET: European deep-sea neutrino telescope
White Rabbit application examples

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- MIKES: Centre for metrology and accreditation
- KM3NET: European deep-sea neutrino telescope

More WR collaborators:
http://www.ohwr.org/projects/white-rabbit/wiki/WRUsers
Outline

1. Introduction
2. Technology
3. Equipment
4. Performance
5. Current developments
6. Conclusions
White Rabbit technology

Based on

- Gigabit Ethernet over fiber
- IEEE-1588 protocol
White Rabbit technology

**Based on**
- Gigabit Ethernet over fiber
- IEEE-1588 protocol

**Enhanced with**
- Layer 1 syntonization
- Digital Dual Mixer Time Difference (DDMTD)
- Link delay model
Open Systems Interconnection (OSI) network model

1. Physical
2. Data Link
3. Network
4. Transport
5. Session
6. Presentation
7. Application
Open Systems Interconnection (OSI) network model

E-mail client to compose a message
Open Systems Interconnection (OSI) network model

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2. Data Link
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E-mail client to compose a message
Data format, compression, encryption
Open Systems Interconnection (OSI) network model

1. Physical
2. Data Link
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6. Presentation
7. Application

- E-mail client to compose a message
- Data format, compression, encryption
- Start, management and termination of communication with a recipient
Open Systems Interconnection (OSI) network model

- **7. Application**: E-mail client to compose a message
- **6. Presentation**: Data format, compression, encryption
- **5. Session**: Start, management and termination of communication with a recipient
- **4. Transport**: Split data into segments to be sent, add information about protocol, make sure all segments reach the destination
- **3. Network**: 
- **2. Data Link**: 
- **1. Physical**: 
Open Systems Interconnection (OSI) network model

1. Physical
   - Add destination IP address to each segment

2. Data Link
   - Split data into segments to be sent, add information about protocol, make sure all segments reach the destination

3. Network
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4. Transport
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5. Session
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6. Presentation
   - Start, management and termination of communication with a recipient
   - Data format, compression, encryption

7. Application
   - E-mail client to compose a message

Other than the content mentioned in the diagram, there is no additional information.
Open Systems Interconnection (OSI) network model

1. Physical
   - Convert bits to electrical signals for a given medium

2. Data Link
   - Add physical addresses (MAC) of the sender and the next hop in the network

3. Network
   - Add destination IP address to each segment

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   - Add information about protocol, make sure all segments reach the destination

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   - Start, management and termination of communication with a recipient

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   - E-mail client to compose a message, data format, compression, encryption

E-mail client to compose a message

Data format, compression, encryption

Start, management and termination of communication with a recipient

Split data into segments to be sent, add information about protocol, make sure all segments reach the destination

Add destination IP address to each segment

Add physical addresses (MAC) of the sender and the next hop in the network

Convert bits to electrical signals for a given medium
Ethernet switches in a nutshell

Ethernet Switch

1 2 3 4 5 6 7 8

MAC: 00-1B-C5-00-00-01
MAC: 00-1B-C5-00-00-02
MAC: 00-1B-C5-00-00-03

D: 00-1B-C5-00-00-02
S: 00-1B-C5-00-00-01
Ethernet switches in a nutshell

- **PC1** → **PC2**

  - D: 00-1B-C5-00-00-02
  - S: 00-1B-C5-00-00-01

**MAC:**
- **PC1:** 00-1B-C5-00-00-01
- **PC2:** 00-1B-C5-00-00-02
- **PC3:** 00-1B-C5-00-00-03
Ethernet switches in a nutshell
Ethernet switches in a nutshell
White Rabbit in OSI model
White Rabbit technology

Based on
- Gigabit Ethernet over fiber
- IEEE-1588 protocol

Enhanced with
- Layer 1 syntonization
- Digital Dual Mixer Time Difference (DDMTD)
- Link delay model
Frame-based synchronization protocol.

Simple calculations:

- link delay\(_{ms}\) \(\delta_{ms} = \frac{t_4 - t_1 - (t_3 - t_2)}{2}\)
- clock offset\(_{ms}\) \(= t_2 - t_1 + \delta_{ms}\)
Precision Time Protocol (IEEE 1588)

- Frame-based synchronization protocol.
- Simple calculations:
  - link delay \( \delta_{ms} = \frac{(t_4-t_1)-(t_3-t_2)}{2} \)
  - clock offset \( \delta_{ms} = t_2 - t_1 + \delta_{ms} \)
- Disadvantages
  - assumes symmetry of medium
  - all nodes have free-running oscillators
  - frequency drift compensation vs. message exchange traffic
Layer 1 Syntonization

- All network devices use the same physical layer clock.
- Clock is encoded in the Ethernet carrier and recovered by the receiver chip.
- Phase detection allows sub-ns delay measurement.
Digital Dual Mixer Time Difference
DDMTD

- Used for precise phase measurements
- Implemented in FPGA and SoftPLL
- 62.5MHz WR clock and N=14 results in 3.814kHz output signals

\[ f_{DDMTD} = \frac{2^n}{2^2 + 1} f_{Ain} \]

\[ x_{in} \]
\[ x_{out} \]
**SoftPLL**

**Introduction**
- Technology
  - Equipment
  - Performance
  - Current developments
  - Conclusions

**Technology**
- **Equipment**
- **Performance**
- **Current developments**
- **Conclusions**

**SoftPLL**

**WRPTP**
- link delay and offset from Master measurement

**DAC**
- **DAC**

**PI controller**
- **PI controller**

**DDMTD**
- **DDMTD**

**FPGA**
- **FPGA**

**External components**
- **FPGA**

**f_{Ref} [Mhz]**
- **f_{Ref} [Mhz]**

**f_{DMTD} = f_{Ref} 2^n/(Δ+2^n) [Mhz]**
- **f_{DMTD} = f_{Ref} 2^n/(Δ+2^n) [Mhz]**

**VM53S3**
- **VM53S3**

**FRETHE025**
- **FRETHE025**

**Software in embedded CPU inside FPGA**

**FPGA**
- **FPGA**

**DDMTD clock signal**
- **DDMTD clock signal**

**Local PTP clock signal**
- **Local PTP clock signal**

**L1 rx clock signal**
- **L1 rx clock signal**

**Ext. ref. clock signal**
- **Ext. ref. clock signal**

**Helper PLL**
- **Helper PLL**

**Main PLL**
- **Main PLL**

**PI controller**
- **PI controller**

**Channel select**
- **Channel select**

**MUX**
- **MUX**

**Phase tag**
- **Phase tag**

**Error**
- **Error**

**Period**
- **Period**

**Phase correction**
- **Phase correction**

**Phase setpoint Up0**
- **Phase setpoint Up0**

**Phase setpoint Up1**
- **Phase setpoint Up1**

**Slow up-down counter**
- **Slow up-down counter**

**2nd channel**
- **2nd channel**

**Helper PLL**
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**Main PLL**
- **Main PLL**

**WRPTP**
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**Link delay and offset from Master measurement**
- **Link delay and offset from Master measurement**

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- **White Rabbit**

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Link delay model

- static hardware delays: $\Delta TXM, \Delta RXM, \Delta TXS, \Delta RXS$
- semi-static hardware delays: $\epsilon_M, \epsilon_S$
- fiber asymmetry coefficient: $\alpha = \frac{\delta_{MS} - \delta_{SM}}{\delta_{SM}}$
Link delay model

- static hardware delays: $\Delta_{TXM}, \Delta_{RXM}, \Delta_{TXS}, \Delta_{RXS}$
- semi-static hardware delays: $\epsilon_M, \epsilon_S$
- fiber asymmetry coefficient: $\alpha = \frac{\delta_{MS} - \delta_{SM}}{\delta_{SM}}$

Calibration procedure to find $\Delta_{TXM}, \Delta_{RXM}, \Delta_{TXS}, \Delta_{RXS}$ and $\alpha$. 
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Typical WR network
White Rabbit Switch

- Central element of WR network
- 18 port gigabit Ethernet switch with WR features
- Optical transceivers: up to 10km, single-mode fiber
- Fully open design, commercially available
Simplified block diagram of the gateware
WR Node: SPEC board

FMC-based Hardware Kit

- All carrier cards are equipped with a White Rabbit port.
- Mezzanines can use the accurate clock signal and “TAI” (synchronous sampling clock, trigger time tag, ...).
White Rabbit PTP Core
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WR time transfer performance: basic test setup

Stable oscillator
- Cesium beam clock
  - $^{133}Cs$
  - 10 MHz
  - 1 PPS

Oscilloscope
- CH1, CH2, CH3, CH4
- 1 PPS

WR Switch
- (master)
- 5 km

WR Switch
- (slave 1)
- 5 km

WR Switch
- (slave 2)
- 5 km

WR Switch
- (slave 3)
- 5 km

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WR time transfer performance: test results

Histogram of offsets between master and each slave

- **Master (CH1)**
- **Slave 1 (CH2)**
  - Mean: 161.86 ps
  - Standard deviation: 5.45 ps
- **Slave 2 (CH3)**
  - Mean: 24.67 ps
  - Standard deviation: 5.30 ps
- **Slave 3 (CH4)**
  - Mean: -135.25 ps
  - Standard deviation: 6.14 ps
WR Switch: low jitter daughterboard

- Current release of WRS in GM mode has suboptimal performance on both jitter (9ps RMS 1Hz-100kHz) and ADEV (1.4E-11 $\tau=1s$ ENBW 50Hz).
- A daughterboard was designed, produced and tested to improve the performance.
- Modified WRS improves performance on both jitter ($<2ps$ RMS 10Hz-100kHz) and ADEV ($<5E-13$ $\tau=1s$ ENBW 50Hz) in GM mode.
Daughterboard Test Setup

![Diagram showing the setup of a GM and Slave with 1 MB/s traffic over 10 km, and a Cs4000 Reference device. The setup includes connections and notes about only one source being measured at the same time (GM or Slave).]
Test Results in GM mode: PM noise

Phase Noise $\mathcal{L}(f)$ in dBc/Hz

AM Noise $\mathcal{M}(f)$ in dBc/Hz

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<th>Notes</th>
<th>RMS Jitter</th>
<th>Duration</th>
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<td>GM Standard Switch (Unsaved)</td>
<td>ref is cesium</td>
<td>9.1E-12 s</td>
<td>20m 0s</td>
<td>120000 pts</td>
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Test Results in GM mode: Modified ADEV

Modified Allan Deviation ($\text{Mod } \sigma_y(\tau)$)

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Test Results in Slave mode: PM noise

Phase Noise $\mathcal{L}(f)$ in dBC/Hz
AM Noise $\mathcal{M}(f)$ in dBC/Hz

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**Modified Allan Deviation (Mod $\sigma_y(\tau)$)**

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Switches and nodes are commercially available

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Standardization

IEEE 1588 revision process is ongoing and contains a sub-committee (High Accuracy) dedicated to White Rabbit. Revised standard expected in mid-2018.
Switches and nodes are commercially available

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Robustness

Based on redundant information and fast switch-over between redundant fibers and switches.
Ethernet Clock distribution a.k.a. Distributed DDS

Distributed Direct Digital Synthesis
- Replaces dozens of cables with a single fiber.
- Works over big distances without degrading signal quality.
- Can provide various clocks (RF of many rings and linacs) with a single, standard link.
Common clock in entire network: no skew between ADCs.
Ability to sample with different clocks via Distributed DDS.
External triggers can be time tagged with a TDC and used to reconstruct the original time base in the operator’s PC.
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- More applications than ever expected
- A versatile solution for general control and data acquisition
- Standard-compatible and standard-extending
- Active participation in IEEE1588 revision process
Need more information?

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