The White Rabbit project
an Ethernet-based solution for sub-ns synchronization and
deterministic delivery

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30 January 2014
Outline

1. Introduction
2. White Rabbit Network
3. Time Distribution
4. Data Distribution
5. Applications
6. Summary
What’s in a name?

Oh dear! Oh dear! I shall be too late!
The White Rabbit in charge of real time
What is White Rabbit?

- Renovation of accelerator’s control and timing
- Based on well-known technologies
- Open Hardware and Open Software with commercial support
- International collaboration
- Many users: CERN, GSI, KM3NET, cosmic ray detectors, metrology labs...
Why we use Open Hardware?

- Get a design just the way we want it
- Peer review
- Healthier relationship with companies
White Rabbit features

- Ethernet-based
  - thousands-nodes system
  - tens-km span
- Synchronism
  - sub-ns accuracy
  - tens-ps precision
- Determinism
  - upper-bound low-latency
  - high reliability
White Rabbit Network

- Standard Ethernet network
- Ethernet features (VLAN) & protocols (SNMP)
- High accuracy synchronization
- Reliable and low-latency Control Data
White Rabbit Switch

- Central element of WR network
- Designed from scratch
- 18 ports
- 1000BASE-BX10 SFPs: up to 10 km, single-mode fiber
- Open design (H/W and S/W)
White Rabbit Node

Modular hardware kit:
- set of Mezzanine boards: ADC, DAC, TDC, Fine delay...
- set of carriers for various needs: PCIe, VME64x, PXIe...
- all carriers equipped with a White Rabbit port
White Rabbit Node - example
White Rabbit Node - example
White Rabbit Node - example
White Rabbit Node - example
White Rabbit Node - example
White Rabbit PTP Core

- Fancy Ethernet MAC with White Rabbit support
- Open IP Core
- Easily integrated into custom FPGA-based designs
Open Hardware Repository (OHWR)

- All schematics, HDL designs and software sources available in OHWR
- Over 100 projects currently hosted
- 11 scientific institutes and 16 companies involved

http://www.ohwr.org
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Time Distribution in White Rabbit Network

- Synchronization with **sub-ns** accuracy **tens-ps** precision
- Combination of
  - Precision Time Protocol (**IEEE1588**) synchronization
  - Layer 1 syntonization
  - Phase measurements
Precision Time Protocol (IEEE1588)

Simple calculations:
- link delay $\delta_{ms} = \frac{(t_4 - t_1) - (t_3 - t_2)}{2}$
- clock offset $\delta_{ms} = t_2 - t_1 + \delta_{ms}$
**Simple calculations:**
- link delay\(_{ms}\): \( \delta_{ms} = \frac{(t_4 - t_1) - (t_3 - t_2)}{2} \)
- clock offset\(_{ms}\): \( t_2 - t_1 + \delta_{ms} \)

**Disadvantages**
- assumes symmetry of medium
- all nodes have free-running oscillators
- frequency drift compensation vs. message exchange traffic
Layer 1 Syntonization

- **System Timing Master**
- **Cesium**
- **Ethernet link**
- **Uplink port**
- **Switch fabric**
- **Clock loopback**

**Cesium**

55 Cs

132.91
Phase measurements

- Monitor phase of bounced-back clock
- Enhance PTP timestamps with phase measurement
- Phase-locked loop in the slave follows the phase changes
WR synchronization performance

Stable oscillator

Cesium beam clock

WR Switch (master)

10 MHz 1 PPS

5 km

Oscilloscope

CH1 CH2 CH3 CH4

1 PPS

WR Switch (slave 1)

WR Switch (slave 2)

WR Switch (slave 3)

5 km

hot-air gun

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White Rabbit

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WR synchronization performance

Histogram of offsets between master and each slave

- Master (CH1)
- Slave 1 (CH2)
  - mean = 161.86 ps
  - sdev = 5.45 ps
- Slave 2 (CH3)
  - mean = 24.67 ps
  - sdev = 5.30 ps
- Slave 3 (CH4)
  - mean = -135.25 ps
  - sdev = 6.14 ps
WR synchronization performance

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ISPCS Plug Fest
WR: most accurate PTP implementation in the world!
WR Standardization under IEEE1588

- We want to standardize!
We want to standardize!

Intention by 1588
Standardization Group expressed in Project Authorization Request

IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems

1. Overview

The protocol enhances support for synchronization to better than 1 nanosecond.
WR Standardization under IEEE1588

- We want to standardize!
- Intention by 1588 Standardization Group expressed in Project Authorization Request
- Enhanced Accuracy Options / Profile
Data Distribution in a White Rabbit Network

Deterministic frame delivery

Topology redundancy

Data redundancy
Types of data distinguished by 802.1Q tag:

- **Control Data** (strict priority)
- Standard Data (Best Effort)

**Control Data** characteristics:

- Sent by Data Master(s)
- Broadcast (one-to-many)
- Deterministic and low-latency
- Reliable delivery

Low-latency WR Switch by design (< 10us)
Data Redundancy (Node)

- **Forward Error Correction (FEC)** – transparent layer:
  - One message encoded into 4 Ethernet frames
  - Recovery of message from any 2 frames
**Data Redundancy (Node)**

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  - One message encoded into 4 Ethernet frames
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- FEC can prevent data loss due to:

![Diagram of FEC process]

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Data Redundancy (Node)

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- FEC can prevent data loss due to:
  - bit errors
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FEC can prevent data loss due to:
- **bit errors**
- **network reconfiguration**
Ideas:
- Using VLANs
- H/W switch-over to the backup link
- WR Rapid Spanning Tree Protocol
- WR Shortest Path Bridging

Seamless redundancy requires Forward Error Correction
Topography reconfiguration performance

Frame Loss and Latencies

<table>
<thead>
<tr>
<th>Frame Size (bytes)</th>
<th>Load (%)</th>
<th>Tx Frames</th>
<th>Rx Frames</th>
<th>Frame Loss</th>
<th>Max Latency (uSec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>288</td>
<td>10</td>
<td>1,217,533</td>
<td>1,217,533</td>
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<td>10,957,793</td>
<td>10,957,792</td>
<td>1</td>
<td>6.12</td>
</tr>
</tbody>
</table>
Introduction

White Rabbit Network

Time Distribution

Data Distribution

Applications

Summary
Distributed oscilloscope

- Common clock in the entire network: no skew between ADCs.
- Ability to sample with different clocks
- Internal time triggers or external asynchronous triggers time tagged with a TDC
CERN Neutrinos to Gran Sasso project

- Investigation of neutrino oscillation
- Time of Flight measurement
CERN Neutrinos to Gran Sasso project

Global Positioning System (GPS)

Long distance

Local

CERN Timing System

Timing by BE-CO-HT

Experiments Timing Systems

Timing by experiments
WR transferring UTC from GPS receiver to the measurement point
8km of fiber between WR Switches
WR Switch in the cavern serves various experiments
Performance monitoring
Results from ~31 days:
  - Accuracy: 0.517 ns
  - Precision: 0.119 ns (std. dev)
Other WR Applications

- CERN and GSI
Other WR Applications

- CERN and GSI
- HiSCORE: Gamma & Cosmic-Ray experiment

> Institute for Nuclear Research of the Russian Academy of Sciences
> Moscow State University
> Irkutsk State University
Other WR Applications

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- HiSCORE: Gamma&Cosmic-Ray experiment
- The Large High Altitude Air Shower Observatory
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- MIKES: Centre for metrology and accreditation
Other WR Applications

- CERN and GSI
- HiSCORE: Gamma&Cosmic-Ray experiment
- The Large High Altitude Air Shower Observatory
- MIKES: Centre for metrology and accreditation
- KM3NET: European deep-sea research infrastructure

Full list of WR users:
http://www.ohwr.org/projects/white-rabbit/wiki/WRUsers
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Successful international collaboration of institutes, universities and companies

WR Users:
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White Rabbit Family

Successful international collaboration of institutes, universities and companies

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Pushing frontiers

- Scientific, open (H/W & S/W), with commercial support
**Pushing frontiers**

- **Scientific, open (H/W & S/W), with commercial support**
- **More applications than ever expected**
Pushing frontiers

- Scientific, open (H/W & S/W), with commercial support
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- A versatile solution for general control and data acquisition
Pushing frontiers

- Scientific, open (H/W & S/W), with commercial support
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- A versatile solution for general control and data acquisition
- Fulfilling all our needs in synchronization and determinism
Scientific, open (H/W & S/W), with commercial support
More applications than ever expected
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Standard-compatible and standard-extending
Pushing frontiers

- Scientific, open (H/W & S/W), with commercial support
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- Standard-compatible and standard-extending
- Active participation in IEEE1588 revision process
Pushing frontiers

- Scientific, open (H/W & S/W), with commercial support
- More applications than ever expected
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Thank you

More information:
http://www.ohwr.org/projects/white-rabbit/wiki
Link Delay Model

\[
\begin{align*}
\text{delay}_{ms} & = \mu + \text{asymmetry} \\
\text{offset}_{ms} & = t_2 - (t_1 + \text{delay}_{ms})
\end{align*}
\]
Link Delay Model

\[ \mu = \frac{(t_4 - t_1) - (t_3 - t_2)}{2} \]

\[ \text{delay}_{ms} = \mu + \text{asymmetry} \]

\[ \text{offset}_{ms} = t_2 - (t_1 + \text{delay}_{ms}) \]
Link Delay Model

\[
\begin{align*}
\text{delay}_{ms} &= \Delta_{txm} + \delta_{ms} + \Delta_{rxs} \\
\text{delay}_{sm} &= \Delta_{txs} + \delta_{sm} + \Delta_{rxm}
\end{align*}
\]
Link Delay Model

\[ \text{delay}_{ms} = \Delta_{txm} + \delta_{ms} + \Delta_{rxs} \]
\[ \text{delay}_{sm} = \Delta_{txs} + \delta_{sm} + \Delta_{rxm} \]

Relative Delay Coefficient \((\alpha)\) for 1000base-X over a Single-mode Optical Fibre

\[ \delta_{ms} = (1 + \alpha) \delta_{sm} \]
Link Delay Model

\[ \text{delay}_{ms} = \Delta_{txm} + \delta_{ms} + \Delta_{rxs} \]

\[ \text{delay}_{sm} = \Delta_{txs} + \delta_{sm} + \Delta_{rxm} \]

Measuring fixed delays is hard

but we use mathematical tricks for that - WR Calibration procedure (http://www.ohwr.org/documents/213)
White Rabbit extension to PTP

White Rabbit requires:
- WR-specific states
- Exchange of WR-specific information
- Asymmetry estimation based on Link Delay Model

WR PTP
- PTP extensions mechanisms
- Enhanced precision \( t_1, t_2, t_3, t_4 \)
- Correction for asymmetry
- Interoperability with PTP gear
White Rabbit Network

- White Rabbit Switch
- White Rabbit Node (White Rabbit PTP Core)
White Rabbit Switch

Functionality of a professional Gigabit Ethernet Switch with White Rabbit extensions

3 layers of design:
WR Switch: hardware

- Xilinx Virtex 6, Atmel AT91SAM9G45
- 18 cages for Gigabit SFPs, 10/100 Ethernet management port
- 5 SMC connectors (1-PPS in/out, CLK in/out)
- designed and produced by *Seven Solutions* in cooperation with CERN
WR Switch: gateware

Implemented in Xilinx Virtex6 FPGA:
Running on ARM processor:
- Embedded Linux
- kernel 2.6.39 with patches and modules for HDL components
- Hardware Abstraction Layer
- RTU daemon
- PTP daemon with WR extension
- CLI and SNMP support coming
White Rabbit Node - WR PTP Core

HDL IP-Core

developed on Xilinx Spartan 6 but not tied to Xilinx

it is a fancy Ethernet MAC

- interfaces user-defined module sending/receiving Ethernet frames with PHY layer
- provides precise timing by implementing WR protocol

ready to be integrated in user’s devices

requires only two tunable oscillators and EEPROM to store the configuration
WR PTP Core: interfaces

- clocks and reset
- frame interface (WR Fabric)
- timecode and 1-PPS output
- PHY interface (*GTP/GTX* tested and supported)
- *I²C*, 1-Wire, UART, GPIO
WR PTP Core: HDL design
WR PTP Core: HDL design