Acknowledgements

• GSI Timing Team: Michael Reese, Jiaoni Bai, Alexander Hahn, Marcus Zweig, Stefan Rauch (associated), Mathias Kreider, Cesar Prados, Anjan Suresh, Wesley Terpstra, Dietrich Beck
• GSI groups: Accelerator Control System, Experiment Electronics, Beam Instrumentation, Ring RF ...
• White Rabbits from CERN and elsewhere

some figures are pirated from
Mathias Kreider, Alexander Hahn and Hanno Hüther (our chief architect)
On Time - In Time: Successful Operation of the GSI Facility by White Rabbit (except UNILAC)

Dietrich Beck - GSI

7 Oct 2018

Dietrich Beck, TOS, d.beck@gsi.de

- What Happened since 2016
- Timing @ GSI (Nodes)
- Timing @ GSI (Data Master)
- Releases
- More Interesting Stuff (if I have time)
- Summary
Outlook: Facility for Antiproton and Ion Research
Photo 2014-05-25: Jan Schäfer for FAIR
FAIR Construction Site (August 2018)
https://www.youtube.com/watch?v=wSN7jloV5nM&index=16&t=4s&list=PL4f-N4xeXktlrQ_6lihokY8eIYDcNTeh
FAIR Phase 0: Operation in 2018

https://www.gsi.de/en/work/accelerator_operations/accelerators.htm?no_cache=1
FAIR Phase 0: Operation in 2018

https://www.gsi.de/en/work/accelerator_operations/accelerators.htm?no_cache=1

development meets reality ...
- very little time for maintenance
- on-call service 24/7 😞

1. Ion sources
2. High charge state injector
3. Transfer channel
4. SIS 18
5. HITRAP
6. ESR
7. CRYRING
8. Target hall (high energy)
9. Experiment area (low energy)
10. UNILAC
11. High current injector

WR @ 2016
WR @ 2018 (MIL Hybrid), LSA
Primer: Event Condition Action Unit (ECA)

- **Event**: DM telegram
- **Condition**: index
- **Action**: configured, executed on-time

**Data Master**
- broadcast telegrams
  - index
  - deadline (ns)
  - ...

**ECA**
- filter (condition)
- `channel`
- `t=x?`
- `on-time`
- `receiver`
- `lemo out`

**Front-End Computer**
- OS
  - user-space
    - `user program ('FESA')`
  - kernel-space
    - `EB library/API`
    - `driver`

**FPGA**
- `driver`
- `bus`
- `timing receiver`

1 ns resolution (order matters!)
On-Time LEMO output or MSI to the host system are simple...

... the so-called **Function Generator** is more challenging.

- a key feature of the accelerator control system
- implementation involves many people/teams (not just TOS)
- use case: ramped devices
- RF-systems
- magnets
- synchronized operation (that's why I mention this topic on a WR workshop)
- 1us precision is sufficient
Primer: Event Condition Action Unit (ECA)

- **Event**: DM telegram
- **Condition**: index
- **Action**: configured, executed on-time

Data Master

- broadcast telegrams
  - index
  - deadline (ns)
  - ...

'event'

ECA

- filter (condition)
- channel
- t=x?
- channel
- 'receiver'
- channel
- lemo out
- on-time action

Front-End Computer

OS

host

user-space

user program ('FESA')

EB library/API

kernel-space

driver

FPGA

Timing receiver

1 ns resolution (order matters!)
Front-End Computer

FESA

Data Master

ECA

'receiver'
• beams A, B, C
• function described as 2nd order polynomials
• the device needs three sets of data
• each data set referenced by an index

Data Master
1. select set
2. prepare
3. start

ECA

Front-End Computer

FESA: 3 data sets

LM32
a) send data
b) start
c) sync clock

FPGA board gen. function from polynomials

after 'start', the function could run 'forever' (seconds, minutes, hours)
power supplies for SIS 18 dipoles – 7MW max output controlled by one SCU (timing receiver)
30MW peak: nice sound when ramping up SIS18!
(synchronized by White Rabbit)
not all devices are ramped
shown: 2 out of 6 rows with 'static' supplies for transfer line magnets
Who you gonna call?

What is this? What is it good for?

This is a simplified view of a part of the control system's architecture, created with the intention to help you make an educated guess on who to call when something's not working. If you're not sure, don't worry. It'll take time to get to know the new control system structures and no one will get mad if you call the "wrong" group.

Please be aware that the diagram focuses on certain areas of the control system and consequently, other equally important components are missing. Also, consider this diagram to be work-in-progress. If you'd like to contribute, see below.

What do the symbols mean?
The boxes symbolize applications, components or subsystems of the control system. The arrows stand for data flows between them. The colored regions represent areas of responsibility. The terms next to the telephone icons are taken from FSN (when switched to English) and may help you look up the on-call number you need to dial.

Who can I ask about it?
If you have any questions, comments, suggestions or corrections regarding this diagram, please feel free to call Hannes at 3089 or write to h.hueber@gsi.de.

Thanks!
**Primer: Data Master**

- **LSA** generates so-called 'patterns groups'
- **Director** controls pattern execution by commands
- **Generator** FESA class as interface to DM
- **CarpeDM** library as interface to firmware
- **DM FPGA**
  - runs on standard PCIe Timing Receiver (ArriaV)
  - lm32 cluster, priority Q, ECA

DM starts scheduling telegrams 1ms ahead of deadline.
- 500us margin for DM
- 500us margin for WR network
**LSA** generates so-called 'patterns groups'

**Director** controls pattern execution by commands

**Generator** FESA class as interface to DM

**CarpeDM** library as interface to firmware

**DM FPGA**
- runs on standard PCIe Timing Receiver (ArriaV)
- Im32 cluster, priority Q, ECA

DM starts scheduling telegrams 1ms ahead of deadline.
CarpeDM is a framework for a domain specific programming language, designed for use with both the FAIR Data Master (DM) and the LHC Software Architecture (LSA).

- CarpeDM also handles data transmission to and from the DM and manages the DM's HW resources (FPGA => memory, bandwidth, etc.).
- Usually, the DM never stops. If timing messages shall not be sent to the network, an 'idle pattern' is executed.
- LSA adds/removes patterns on-the-fly. CarpeDM allows to remove active patterns under certain conditions.
- During operation, pattern execution can be modified by commands sent to the FPGA via CarpeDM.

*Add optional blocks to achieve different durations of alternate paths

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**Figure 3.3: Schedule cheatsheet**

- (a) if...then*
- (b) if...then, else
- (c) case...with default
- (d) until...repeat
- (e) repeat until...
- (f) while...do
- (g) do while...
- (h) for 0 ≤ i < n
- (i) for 0 ≤ i ≤ n
- (j) Simple wait loop
- (k) Wait loop with timeout
LSA and DM: Patterns for Operation
LSA and DM: Patterns are DOT Language

ESR storage ring

Collect
Bunching
Coupling to SIS18
Cooler

Fast transfer to HHD cave with cooler

Fast acceleration

SIS18 synchrotron

CRYRING storage ring

Injection

Idle

Slow transfer to HADES cave

Slow transfer to HHD cave
Release Process: Responsibility

- Asterisk (2014)
- Balloon (2016)
- Cherry (2017)
- Doomsday (2018)
- E...

Timing Team Responsibility

Data Master

Front-End Computer

OS

host

user-space

FESA

Timing API 'saftlib'

EB library/API

kernel-space

driver

FPGA

timing receiver

Gateware

bus

bridge
Release Process: Challenges

- large user community with different applications
  - Accelerator Control System (1µs precision)
  - Beam Instrumentation (1ps jitter using dedicated HW, 1ns precision)
  - RF Systems (< 3ns accuracy from WR, ref clock distribution system BuTiS)
  - Experiments (< 10ps precision with local calibration)
- lot of feature requests and bug fixes for each release
- different target OS (CentOS, Debian, SuSe, ...)
- variety of kernels (3.X to 4.X)
- many form factors (SCU, µTCA, PMC, PCIe, ...)
- has to work with FESA
- release of stable libraries, tools, gateways (FPGA)
- testing (automated an manually), sometimes really exhausting and difficult
- must be rock-solid (uptime of accelerator has priority)
Release Process: Our Tools

Git
- allows tags and branches
- we use GitHub's issue tracker and pull request system

Jenkins
- provides nightly builds and auto builds after someone pushed code
- automated hardware and software tests for gateware and libraries

Bitstream Mining
- FPGA is nearly out of resources, we have to try a hole series of „Fitter Initial Placement Seeds“ to meet all timing constraints and requirements! This is automated at runs until a good seed is found. Otherwise White Rabbit or other parts of the design won't work properly (also critical for remote updating).

Timing Test Facility
- everything comes together here (gateware, libraries, tools, ...)
- 40 timing receivers, different OS, different kernels, different hosts, different bitstream on FPGAs
- small replication of our facility, data master plays random schedules
- White Rabbit has to stay in track phase for weeks, PPS on IOs is measured constantly
- 10 layers of switches and an additional ethernet traffic generator for random „ethernet noise“
- testing (automated an manually), sometimes really exhausting and difficult
Test Facility
FAIR Phase 0: Operation in 2018

https://www.gsi.de/en/work/accelerator_operations/accelerators.htm?no_cache=1

1. Ion sources
2. High charge state injector
3. Transfer channel
4. SIS 18
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8. Target hall (high energy)
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11. High current injector

WR @ 2016

WR @ 2018 (MIL Hybrid), LSA
### Hybrid: White Rabbit + MIL

**alarm based** → **event based**

#### (New) General Machine Timing
- White Rabbit PTP (IEEE 1588)
- all nodes share a common notion of time
- alarm based system
- primary system
- used for all important / advanced / LSA supplied equipment such as ramped devices (magnets, RF, ...)

#### (Old) 'MIL Timing'
- MIL-STD-1553 (+ extension)
- event based system
- remains for 'simple' equipment

#### Gateway
- timing receiver node
- receives timing telegrams from Data Master
- on-time: translate 256bit timing telegram to 16bit event data and send data to the MIL bus

**Why?** cost and effort
FAIR Phase 0: Operation in 2018

https://www.gsi.de/en/work/accelerator_operations/accelerators.htm?no_cache=1

WR @ 2016
WR @ 2018 (MIL Hybrid, LSA)

1. Ion sources
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11. High current injector
1. receive 'announce message' from DM (containing 'addresses' of shared mem)
2. receive message from DM (containing beam properties requested by LSA)
3. request beam with properties at UNILAC (via field bus)
4. receive MIL event exactly 10ms prior to beam delivery: timestamping + analysis
5. via Etherbone / WR network: analyze state of DM, **last chance to quit**
6. via Etherbone / WR network: set start time of SIS18 injection sequence at DM
7. DM starts injection sequence 8.5ms prior to beam arrival (start ramping magnets..)
- 20ms cycle time
- instant switching between 3 ion sources, energies
- typically 1s cycles
- 10 ms

1. receive 'announce message' from DM (containing 'addresses' of shared mem)
2. receive message from DM (containing beam properties requested by LSA)
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7. DM starts injection sequence 8.5ms prior to beam arrival (Start ramping magnets..)
WR Wishlist

- less lossy WRS, see RFC 2889 test by GSI (2016), available via OHWR. Low average bandwidth utilization, but data often sent in bursts.
- WRS SNMP:
  - support for SFPs with Digital Diagnostics Monitoring (DMM)
  - possibility for acknowledgment of WRS errors
- WRS hardware 3.4 (working horse for the next 10 years): long term support of gateware, firmware, software
- UTC offset and leap seconds handling (availability in nodes), see https://www.ohwr.org/projects/wr-cores/work_packages/1168/activity
- VLAN support for WRS and nodes
- LLDP
- ...

Summary

- GSI, a leading particle accelerator for science, is using a White Rabbit based Timing System for all ring machines and high energy transfer lines
- so far: 32 WRS and 134 nodes (production system 8/2018), **numbers increasing**
- Timing System works reliable and stable
- lots of features for upcoming beam times still missing ('storage ring operation', 'therapy-like operation', ...)
- lots of features for FAIR still missing ('Forward Error Correction', 'Bunch-To-Bucket', ...)
- https://github.com/GSI-CS-CO/bel_projects
- OHWR (software, firmware, HDL, ...)
- https://www.ohwr.org/projects/tr-pmc (Arria V GX based PMC module)
- https://www.ohwr.org/projects/tr-amc (Arria V GX based AMC module)
- https://www.acc.gsi.de/wiki/Timing
### 'Event Snooping': Line Mode

<table>
<thead>
<tr>
<th>Event</th>
<th>BeamIn</th>
<th>Seq. Id</th>
<th>Proc. Id</th>
<th>Reserved</th>
<th>Chain Id</th>
<th>Parameter</th>
<th>Flags</th>
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</table>

**Statistics**
- Late Event Count: 0
- Early Event Count: 0
- FTRN Action Count: 27244826
- FTRN Overflow Count: 0
Thank you for your attention!
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<td>4.0.4</td>
<td>PEXARIA5b; CID 55 0093 0068; SIS18 ACCT; BG2.009; H.Braeuning*</td>
</tr>
<tr>
<td>vme1021t</td>
<td>Production</td>
<td>ok</td>
<td>1</td>
<td>1534748733</td>
<td>36999</td>
<td>TRACING</td>
<td>UP</td>
<td>482.43</td>
<td>4.0.5</td>
<td>PEXARIA5b; CID 55 0093 0111; Steinhagen</td>
</tr>
<tr>
<td>vme1021t</td>
<td>Production</td>
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<td>36999</td>
<td>TRACING</td>
<td>UP</td>
<td>953.89</td>
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</tr>
<tr>
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<td>Production</td>
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<td>1534748733</td>
<td>36999</td>
<td>TRACING</td>
<td>UP</td>
<td>983.90</td>
<td>4.0.5</td>
<td>PEXARIA5b; CID 55 0093 0111; Steinhagen</td>
</tr>
<tr>
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<td>Production</td>
<td>ok</td>
<td>1</td>
<td>1534748733</td>
<td>36999</td>
<td>TRACING</td>
<td>UP</td>
<td>832.61</td>
<td>4.0.4</td>
<td>PEXARIA5b; CID 55 0093 0362; CID_PROTOTYPE; LOBI Harald Br*</td>
</tr>
<tr>
<td>vme1021t</td>
<td>Production</td>
<td>ok</td>
<td>1</td>
<td>1534748733</td>
<td>36999</td>
<td>TRACING</td>
<td>UP</td>
<td>623.96</td>
<td>4.0.4</td>
<td>PEXARIA5b; CID 55 0093 0362; CID_PROTOTYPE; LOBI Harald Br*</td>
</tr>
<tr>
<td>vme1021t</td>
<td>Production</td>
<td>ok</td>
<td>1</td>
<td>1534748733</td>
<td>36999</td>
<td>TRACING</td>
<td>UP</td>
<td>166.69</td>
<td>4.0.4</td>
<td>PEXARIA5b; CID 55 0093 0362; CID_PROTOTYPE; LOBI Harald Br*</td>
</tr>
</tbody>
</table>

1: tr-status_2018-08-30.txt  Top 1  (Text)
GMT Status

Generator (Data Master)

- nomen: ZT002Z21 (CMW dir: cmwpro00a.acc.gsi.de:5021)
- EB dev: connected
- WR sync: TRACKING

<table>
<thead>
<tr>
<th>CPU</th>
<th>what</th>
<th>msg</th>
<th>10s</th>
<th>1m</th>
<th>1h</th>
<th>wrn</th>
<th>10s</th>
<th>1m</th>
<th>1h</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>SIS+HEST</td>
<td>26.6</td>
<td>24.0</td>
<td>23.2</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>CRYRING</td>
<td>22.1</td>
<td>21.4</td>
<td>21.3</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>ESR</td>
<td>1.0</td>
<td>1.0</td>
<td>1.2</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>N/A</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>total</td>
<td></td>
<td>49.7</td>
<td>46.4</td>
<td>45.8</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
</tbody>
</table>

Table: CPU message rates and number of warnings [Hz].

Clock Master

- WRS: nw0013m66.timing.acc.gsi.de

<table>
<thead>
<tr>
<th>what</th>
<th>port</th>
<th>TX:10s</th>
<th>1m</th>
<th>1h</th>
<th>RX:10s</th>
<th>1m</th>
<th>1h</th>
</tr>
</thead>
<tbody>
<tr>
<td>data master</td>
<td>port1</td>
<td>6.0</td>
<td>6.0</td>
<td>5.2</td>
<td>32.5</td>
<td>32.0</td>
<td>30.5</td>
</tr>
<tr>
<td>1st down-link</td>
<td>port13</td>
<td>27.1</td>
<td>26.3</td>
<td>25.6</td>
<td>1.1</td>
<td>0.9</td>
<td>0.9</td>
</tr>
<tr>
<td>2nd down-link</td>
<td>port14</td>
<td>29.5</td>
<td>29.0</td>
<td>27.6</td>
<td>3.3</td>
<td>3.8</td>
<td>2.9</td>
</tr>
</tbody>
</table>

Table: Packet rates [Hz] at various ports. Assuming an average size of 125 bytes/packet, the above numbers are in [kbit/s].

Node

- nomen: ZT002M02 (CMW dir: cmwpro00a.acc.gsi.de:5021)

<table>
<thead>
<tr>
<th>what</th>
<th>count</th>
<th>last change on</th>
</tr>
</thead>
<tbody>
<tr>
<td>action</td>
<td>64515130</td>
<td>Thu Aug 9 13:42:28 CEST 2018</td>
</tr>
<tr>
<td>late</td>
<td>11</td>
<td>Sun Jul 29 01:06:49 CEST 2018</td>
</tr>
<tr>
<td>early</td>
<td>0</td>
<td>Thu Jul 19 12:57:14 CEST 2018</td>
</tr>
<tr>
<td>overflow</td>
<td>0</td>
<td>Thu Jul 19 12:57:14 CEST 2018</td>
</tr>
</tbody>
</table>

Table: ECA statistics.

Gateways

<table>
<thead>
<tr>
<th>what</th>
<th>node</th>
<th>sync</th>
<th>UTC offset [ms]</th>
<th>status</th>
<th>10s</th>
<th>1m</th>
<th>1h</th>
<th>late info [1]</th>
<th>noBeam</th>
</tr>
</thead>
<tbody>
<tr>
<td>dm-unixz</td>
<td>scu0223</td>
<td>TRACKING</td>
<td>37000</td>
<td>OpReady OK</td>
<td>.3</td>
<td>.3</td>
<td>.2</td>
<td>1.451</td>
<td>0</td>
</tr>
<tr>
<td>wrmli-sis</td>
<td>scu0228</td>
<td>TRACKING</td>
<td>36999</td>
<td>configured</td>
<td>5.7</td>
<td>5.7</td>
<td>4.2</td>
<td>08-Aug-326</td>
<td>N/A</td>
</tr>
<tr>
<td>wrmli-esr</td>
<td>scu00068</td>
<td>TRACKING</td>
<td>37000</td>
<td>configured</td>
<td>1.1</td>
<td>1.0</td>
<td>1.0</td>
<td>not yet late</td>
<td>N/A</td>
</tr>
</tbody>
</table>

Table: Info, operation rates [Hz] and "late info''.
[1] late info:
- unixz: remaining time budget for data master [ms] (min 1.0ms)
- wrmli: last occurrence, when lm32 was not able to dispatch MIL event on time

Icinga

<table>
<thead>
<tr>
<th>node</th>
<th>date</th>
<th>status</th>
</tr>
</thead>
<tbody>
<tr>
<td>scu0116</td>
<td>Thu Aug 9 13:41:12 2018</td>
<td>ok: everything is fine</td>
</tr>
<tr>
<td>scu0143</td>
<td>Thu Aug 9 13:38:05 2018</td>
<td>ok: everything is fine</td>
</tr>
</tbody>
</table>

Table: Status of dedicated Event Listeners.

version 0.0.5
FAIR Timing Master (Clock, Data, Management)
General Machine Timing System (GMT)  
Real-Time Control of the Facility

**LSA** Settings Management „off-line system“  
generates settings: indexed data and schedule for GMT

index data  
schedule with index

Black: preload data ahead of time
Red: real-time

1 x Data Master  
μs real-time (!) scheduling, broadcast of messages,  
embedded multi-core lm32 cluster (+multi-threading) *

nnnn x Timing Receiver Nodes  
Event-Condition-Action unit (ECA): map messages to timely  
executed actions (1ns), error handling+reporting, VHDL **

nnnn x Front-End  
„on-time“ execution of pre-configured actions

* M. Kreider, New developments on the FAIR Data Master, PCaPAC2014, Karlsruhe, Germany  
** W. Terpstra, Inexpensive Scheduling in FPGAs, PCaPAC2014, Karlsruhe, Germany
Multiple GMT Instances
(each instance interconnects multiple buildings)

Production:
• operation of facility only
• strict policies
• backup GPSDO
• backup grandmaster WRS
• backup data master

Timing:
• dedicated to nasty testing
• locked to GPSDO
• data master
• new: 24 port traffic generator
• exclusive use by timing team

User:
• service to others
• users may test GMT here
• locked to GPSDO
• data master
• best effort only
General Plan of Accelerator Operations 2018 (approved: 2018-09-12)

January
Sources
Unilac
SIS 18
ESR
Crying
cw Demo

February
Sources
Unilac
SIS 18
ESR
Crying
cw Demo

March
Sources
Unilac
SIS 18
ESR
Crying
cw Demo

April
Sources
Unilac
SIS 18
ESR
Crying
cw Demo

May
Sources
Unilac
SIS 18
ESR
Crying
cw Demo

June
Sources
Unilac
SIS 18
ESR
Crying
cw Demo

July
Sources
Unilac
SIS 18
ESR
Crying
cw Demo

August
Sources
Unilac
SIS 18
ESR
Crying
cw Demo

September
Sources
Unilac
SIS 18
ESR
Crying
cw Demo

October
Sources
Unilac
SIS 18
ESR
Crying
cw Demo

November
Sources
Unilac
SIS 18
ESR
Crying
cw Demo

December
Sources
Unilac
SIS 18
ESR
Crying
cw Demo

Legend
Bake Out
Dry-Run
Commissioning without beam
Beam Setup
User Beam Time
Ext. Beamtime Machine Coordinator
Operator Training
FF-Conditioning
EGG Test
Test Period
Engineering Run
Holidays
Weekends
Public Holidays

Information
Date of last update: 2018-09-28
Stephan Reimann, Head of Operations, Tel +49 1520 4206156, Email: s.reimann@psi.de

User Beamtime

<table>
<thead>
<tr>
<th>Name</th>
<th>Days</th>
<th>Shifts</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unilac</td>
<td>30</td>
<td>90</td>
</tr>
<tr>
<td>SIS 18</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>ESR</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Crying</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>cw Demo</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

MCR manned: 214, 792
GMT: Linked to GPS and RF Clock System BuTiS

GMT: 10 MHz + PPS + date/time

BuTiS: 10 MHz + 100 kHz