Development of a White Rabbit Interface for Synchronous Data Acquisition and Timing Control

Weibin Pan, Qiang Du, Guanghua Gong

***Abstract*–Sub-nanosecond precision timing distribution and control are key techniques in various distributed real-time applications, where the proposed White Rabbit (WR) project provides a solution combining both data transmission and timing control via the same media. This paper demonstrates the design and development of a compact, standalone WR node following FPGA Mezzanine Card (FMC) standard, which would work as a common WR interface to different applications. Test results show that the timestamp synchronization precision of 65ps (RMS) has been observed between the node and a WR switch, and the data throughput of over 0.3Gbps has been verified in a preliminary test between the node and a PC host.**

I. Introduction

THE White Rabbit project (WR) is a timing control solution aims to synchronize over 1000 nodes with sub-ns accuracy over fiber lengths of up to 10km [1]. It is based on several technologies including Synchronous Ethernet, PTP and DDMTD phase detection.

A typical WR link path consists of a timing master and multiple slaves connected via WR switches. The WR node provides an endpoint interface to each application, providing synchronous clock, calibrated timestamps and Gigabit Ethernet interface. Currently the most common hardware platform of WR node is developed as the Simple PCIe FMC Carrier (SPEC) [2]. For applications that require standalone, compact and low-cost WR interface, a compact universal timing endpoint based on the White Rabbit (CUTE-WR) is developed. The features of the CUTE-WR include:

1. Standalone operation without PC or crates;
2. Compact. A White Rabbit node implementation with minimum components required;
3. Universal. A standard FPGA Mezzanine Card (FMC);
4. Multiplexing of time synchronization and DAQ;
5. Potential ability of remote upgrading and management.

The CUTE-WR, which is dedicated for clock and time synchronization, can be mounted to a FMC carrier specific to the application. Since White Rabbit network is fully compatible with IEEE 802.3 Ethernet, a DAQ function could be integrated into the CUTE-WR.

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II. Hardware

The initial design of the CUTE-WR is derived from the SPEC, a simple 4-lane PCIe card, acts as a carrier for FPGA Mezzanine Cards. However, the CUTE-WR would work in an opposite manner as a FPGA Mezzanine Card. This makes the CUTE-WR quite easy to be integrated into some complicated systems.

For a White Rabbit node design, several essential components are required:

1. FPGA. This is the main component implementing the WR PTP Core (WRPC) [3];
2. Reference clock generator consisting of a DAC chip, a 25MHz VCTCXO and a PLL fanout chip;
3. DMTD clock generator consisting of a DAC chip and a 20MHz VCXO;
4. A SFP transceiver.

In the CUTE-WR, a Xilinx FPGA XC6SLX45T-3FGG484C is chosen for an optimal balance of cost, power and performance. Moreover, this device offers 4 GTP transceivers capable of operating at data rates up to 3.2Gb/s. An external PHY chip will be required for FPGAs without build in transceivers.

The hardware block diagram of the CUTE-WR is shown in Fig. 1.

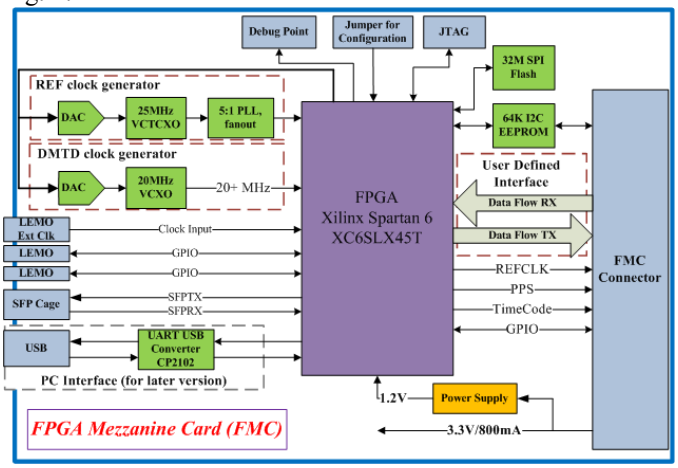

Fig. 1. The CUTE-WR hardware bock diagram

The CUTE-WR contains a few components that are not necessary for a WR node but might be quite useful for practice. A SPI flash is used to store firmware if self-loading mode (also called master mode) is chosen for FPGA configuration. The FPGA can also be configured by an external controller (slave mode) through FMC connector. A jumper is mounted on the CUTE-WR for configuration mode selection.

According to the FMC standard, an on board I2C EEPROM which keeps information pertaining to the characteristics of the CUTE-WR is required [4]. In current version of the CUTE-WR, three LEMO connectors, two dual LEDs and a SFP cage are placed on the front panel. One LEMO is used for external clock input because the hardware of the CUTE-WR is designed to be compatible for both master and slave WR node. The other two LEMOs are used as general purpose IO. One of them would be replaced by a USB connector in later version. Since the CUTE-WR is designed for standalone work mode, an interface like USB or UART is used only for development and debug.

III. Function Verification

Two tests have been made to verify the major functions of the CUTE-WR: time synchronization and high speed data transmission.

A. Time Synchronization Test

The PPS signal skew between two WR nodes was measured over a period of 20 minutes with a LeCroy 10GS/s oscilloscope. The WR switch is the master while the CUTE-WR is the slave as shown in Fig. 2.

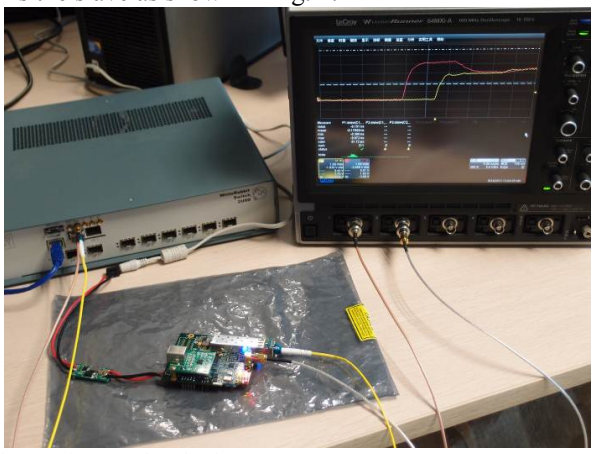

Fig. 2. Time synchronization test setup

The statistic histogram of obtained PPS skew samples is depicted in Fig. 3.

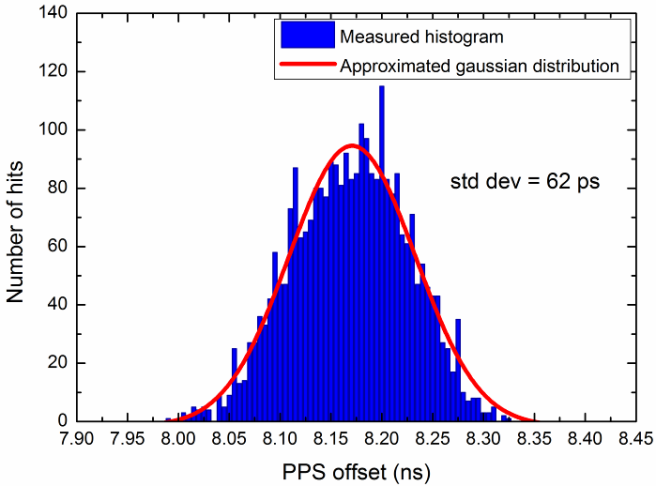

Fig. 3. Measured histogram of PPS offset between the CUTE-WR and the WR switch

The result shows a standard deviation of 62ps and a span of 350ps. An approximate delay of 8ns mainly comes from the difference of the PPS signal routing length, from FPGA logic element to the oscilloscope.

The PPS skew between WR switch and SPEC is also measured. A standard deviation of 115ps is achieved as shown in Fig. 4.

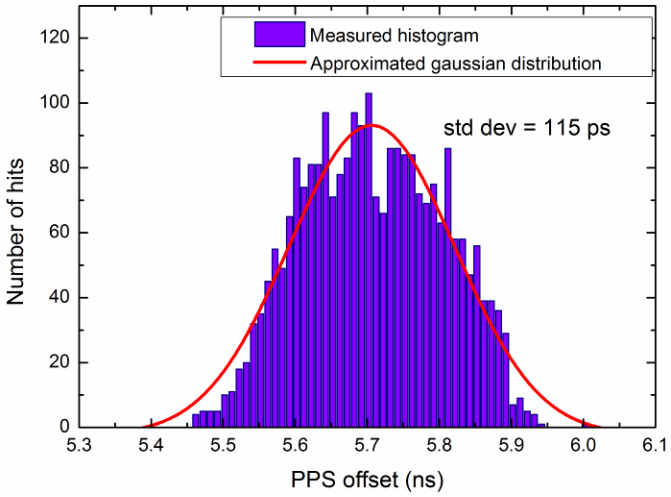

Fig. 4. Measured histogram of PPS offset between SPEC and the WR switch

The standard deviation may partly result from the jitter of the single ended PPS signal and thus a differential PPS signal may improve the test result.

B. Ethernet Loopback Test

An Ethernet loopback test has been setup as shown in Fig. 5. The CUTE-WR buffers the UDP packets coming from a laptop and sends them back after modifying the header information. The returned packets data will be checked by the laptop. A 12 port gigabit switch is used as a copper cable to optical fiber convertor.

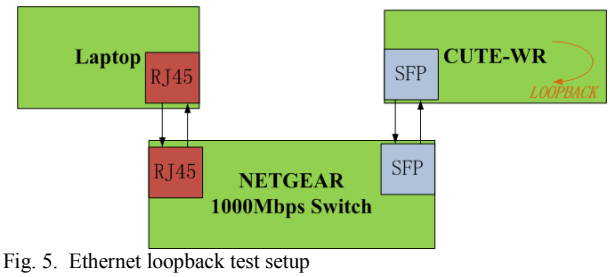

Fig. 5. Ethernet loopback test setup

The Ethernet data path of WR PTP Core (WRPC) [3] is shown in Fig. 6. The WRPC is designed to be capable of both time synchronization and user defined Ethernet communication. It contains a fabric redirector module which is used as a multiplexer/demultipexer for PTP messages and other Ethernet packets. The acceptable Ethernet frame types should be specified and any unrecognized frame will be dropped by the WR endpoint module. Since a UDP frame is encapsulated in an IP frame, the reception of IP frames is enabled in our test. A UDP loopback module, which

communicates with the Fabric Redirector through a pipelined wishbone interface, is designed for this test.

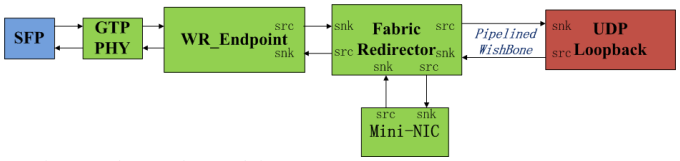

Fig. 6. Ethernet data path in WRPC

A typical test bench program running in Linux laptop sends 500,000 packets to CUTE-WR and reads them back. Setting the concurrent number of UDP send program will change the data throughput rate. With an average packet size of 1116.5 bytes including header and CRC, the maximum transfer rate that the laptop can handle is 323.9Mbps, when its CPU load reaches 99%. No packets were lost or corrupted during the test.

It is believed that the WRPC should have much higher capacity of UDP data throughput rate.

However, currently the CUTE-WR doesn't handle any application layer protocol, such as UDP and TCP. This could be done with another LM32 core while leaving the existing one dedicated for White Rabbit Protocol untouched. For the application with high transmission rate requirement, an IP/UDP process module without CPU is required [5].

IV. Possible Applications

The Large High Altitude Air Shower Observatory (LHAASO) project, consisting of approximately 10000 ground detectors over an area of 1km^2, is designed to trace cosmic gamma ray sources [6]. To reconstruct cosmic ray arrival directions, a uniform clock and synchronized timestamp is required for all the detectors. The WR protocol will be used to recovery clock from WR network and deliver precise time information to different types of frontend electronics which are specific to the detectors [7]. A possible distributed architecture of clock synchronization for LHAASO with help of CUTE-WR is shown in Fig. 7.

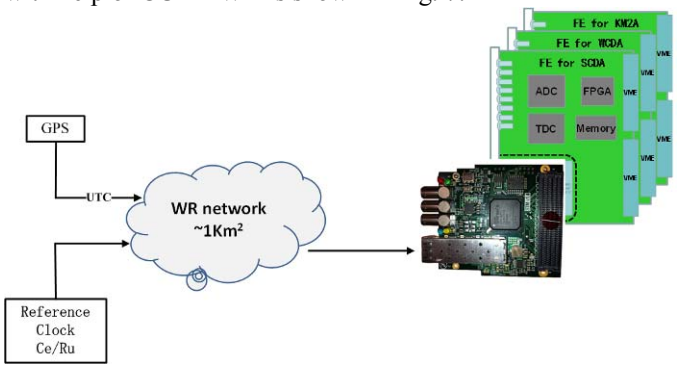

Fig. 7. Clock synchronization architecture for LHAASO. KM2A, WCDA and SCDA are detector arrays in LHAASO project.

China JinPing Deep Underground Laboratory (CJPL) is a low background laboratory with more than 2400km rock overburden [8]. It is a platform for low backgrounds experiments, such as China Dark matter Experiment (CDEX). The CUTE-WR is able to provide a uniform clock for each individual experiment in this deep underground laboratory.

This technology will also be applied in the upgrade of clock distribution system for Daya Bay reactor neutrino experiment.

V. Conclusion

A compact universal timing endpoint based on the White Rabbit is designed. Based on the minimum hardware required for a WR node implementation, this module is designed to be universal for different applications. A preliminary test shows that the CUTE-WR has a comparable timing performance with the SPEC and the standard deviation of PPS skew between the master and the slave is 62ps. An Ethernet loopback test verifies the function of high speed data communication.

For future work, a UDP based data transfer will be implemented and the CUTE-WR will be tested in conjunction with the frontend boards for LHAASO project. Timing performance of the whole system including detectors and frontend electronics will be evaluated.

Acknowledgment

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