WR PTP Core
status and plans

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Outline

• What is WR PTP Core
• Supported platforms
• Main features of v4.2
• Plans for future release
White Rabbit network

In this presentation we focus on WR Nodes
WR Node

WR PTP Core is essential part of every WR Node
WR PTP Core overview

- Gigabit Ethernet MAC HDL module
- ... with WR features
- Provides time to user cores
- Can send and receive user-defined Ethernet frames
WR PTP Core overview

- Implemented in the FPGA
- Using VHDL language
- You don’t need to know WR internals
- You need to know FPGAs to use it
• LatticeMico32 runs WR PTP daemon
WR PTP Core interfaces

- Clocks / reset
- DACs output
- PHY I/F
- Flash/EEPROM
- UART / LEDs

Fabric I/F
Control WB
Timecode I/F
Aux Clk I/F

Hardware interfaces

User interfaces

WR PTP Core
WR PTP Core interfaces

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WR PTP Core interfaces

Configuration memory

- Clocks / reset
- DACs output
- PHY I/F
- Flash/EEPROM
- UART / LEDs

WR PTP Core

- Fabric I/F
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Simple shell / LEDs
WR PTP Core interfaces

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Tx/Rx application frames
WR PTP Core interfaces

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WR PTP Core

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Access to all registers and memory

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WR PTP Core interfaces

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WR PTP Core

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TAI time, 1-PPS
WR PTP Core interfaces

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WR PTP Core interfaces:
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DAC → VCO
Where to start?

• Main WRPC wiki page
  https://www.ohwr.org/projects/wr-cores/wiki/wrpc-core

• User manual for the last stable release (v4.2)

• \textit{wr-cores} git repository
  git://ohwr.org/hdl-core-lib/wr-cores.git

• \textit{wrpc-sw} git repository (optional)
  git://ohwr.org/hdl-core-lib/wr-cores/wrpc-sw.git
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Officially supported hardware

- Reference design for every stable release
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- SPEC – PCIe, Xilinx Spartan 6
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- SVEC – VME, Xilinx Spartan 6
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- VFC-HD – VME, Altera Arria V
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- VFC-HD – VME, Altera Arria V
- FASEC – “pizzabox”, Xilinx Zynq
Officially supported hardware

- SPEC – PCIe, Xilinx Spartan 6
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- VFC-HD – VME, Altera Arria V
- FASEC – “pizzabox”, Xilinx Zynq

For all these, use one of Board Support Packages.
Board and Platform Support Package

- **Board Support Package (BSP)**
  - WR PTP Core
  - VCO DAC controller
  - Reset logic
  - Differential clock buffers
  - Platform Support Package

- **Platform Support Package (PSP)**
  - Deterministic GbE Serdes module
  - PLLs for main and DMTD offset clock

BSP glues WRPC with all required FPGA modules for a given hardware
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Main features of v4.2

• Vivado synthesis support
• Reference designs for Zynq, Artix-7, Kintex-7
  • Artix-7 and Kintex-7 designs contributed by Nikhef

• WRPC Shell command to format Flash/EEPROM with SDBFS
  • Host tool no longer required
• VLANs support
• SNMP for monitoring and configuration
  • “WRPC Failures and Diagnostics” document
SNMP support

• Very minimalistic SNMP implementation, exports raw values
• The agent does not provide status tree like for the WR Switch
• SNMP manager has to analyze errors according to the instructions in: “WR PTP Core: Failures and Diagnostics”
• SNMP SET support for calibration values (SFP database)

```
$ snmpwalk $SNMP_OPT wrpcSfpTable
WR-WRPC-MIB::wrpcSfpPn.1 = STRING: AXGE-1254-0531
WR-WRPC-MIB::wrpcSfpPn.2 = STRING: AXGE-3454-0531
WR-WRPC-MIB::wrpcSfpDeltaTx.1 = INTEGER: 180750
WR-WRPC-MIB::wrpcSfpDeltaTx.2 = INTEGER: 180750
WR-WRPC-MIB::wrpcSfpDeltaRx.1 = INTEGER: 148326
WR-WRPC-MIB::wrpcSfpDeltaRx.2 = INTEGER: 148326
WR-WRPC-MIB::wrpcSfpAlpha.1 = INTEGER: 72169888
WR-WRPC-MIB::wrpcSfpAlpha.2 = INTEGER: -73685416
End of MIB
```
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Plans for future release

- New FPGA platforms: Virtex-5, Kintex Ultrascale
- New supported boards: Cute-WR-DP
- Absolute calibration support
- Expanded SNMP SETs for configuration
  - *init* script
- Link Layer Discovery Protocol (LLDP) support
New Board Support Package

- CUTE-WR-DP – Xilinx Spartan 6
- Contribution by Tsinghua University
Summary

- WR PTP Core implements White Rabbit for the node
- Provides WR time for user-defined HDL modules
- The simplest way to use it is through Board and Platform Support Packages

- You don’t need to know WR internals to use it
- You need to know FPGAs to use it