White Rabbit clock characteristics

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White Rabbit (WR)

- Accelerator’s control and timing
White Rabbit (WR)

- Accelerator’s control and timing
- Open hardware & software
White Rabbit (WR)

- Accelerator’s control and timing
- Open hardware & software
- Ethernet network with two services:
  1. High accuracy synchronization
  2. Deterministic and reliable data delivery
     - Sub-ns accuracy and < 50ps precision

Protocol: WR extension to IEEE1588-2008 (PTP)
Implementation: timestamps and Layer 1 synchronization
White Rabbit (WR)

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  - Implementation: timestamps and Layer 1 syntonization
Applications
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This article focuses on Layer 1 syntonization

Applications with specific frequency transfer requirements
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Applications with specific frequency transfer requirements

- Telecommunication-related applications:
  - New technologies need both frequency and time
  - L1 syntonization using SyncE
  - Legacy requirements
This article focuses on Layer 1 syntonization

Applications with specific frequency transfer requirements

- Telecommunication-related applications:
  - New technologies need both frequency and time
  - L1 syntonization using SyncE
  - Legacy requirements

- National Time Laboratories:
  - Backup/replacement for Satellite-based transfer
  - Extremely precise frequency transfer requirements
1. Introduction to White Rabbit
2. L1 Syntonization in White Rabbit
3. Current L1 Syntonization Characteristics
4. Improvement of L1 Syntonization
5. PTP Synchronisation with the Modified L1 Syntonization
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PTP Synchronization and L1 Syntonization

PTP port in the **master** state

Local PTP Clock

PTP port in the **slave** state

Local PTP Clock

PTP synchronization

L1 syntonization

medium

time
PTP Synchronization and L1 Syntonization

Usual PTP implementation:

- PTP port in the **master** state
- PTP port in the **slave** state
- Master time messages
- Local PTP Clock
- Time control
- PTP synchronization
- Medium

L1 Syntonization
PTP Synchronization and L1 Syntonization

PTP Telecom Time & Phase Profile:

- PTP port in the **master** state
- Local PTP Clock
- Master time
- PTP synchronization
- L1 syntonization

- PTP port in the **slave** state
- Local PTP Clock
- Time control
- Master time
- Medium
PTP Synchronization and L1 Syntonization in WR

White Rabbit:

PTP port in the **master** state

Local PTP Clock

Master time

PTP messages

PTP synchronization

L1 syntonization

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time

PTP port in the **slave** state

Local PTP Clock

Master time

Time control

Phase shifting DDMTD-based WR PLL

$x_{rx,B}$
PTP Synchronization and L1 Syntonization in WR

White Rabbit:

PTP port in the **master** state

Master time

Local PTP Clock

PTP synchronization

L1 syntonization

PTP port in the **slave** state

Time control

Local PTP Clock

Phase shifting DDMTD-based WR PLL

\[ x_{rx_B} \]
Digital Dual Mixer Time Difference (DDMTD)

**Input:**
- frequency $f_{in} [\text{Hz}]$
- phase $\phi_{in} [\text{rad}]$

**Zooming effect:**
$$x_{in} [\text{ns}] = \frac{1}{1 + 2N} x_{out} [\text{ns}]$$
Digital Dual Mixer Time Difference (DDMTD)

- **Input:**
  - frequency $f_{in}[Hz]$  
  - phase $\phi_{in} [\text{rad}]$

- **Output:**
  - proportionally lower frequency $f_{out}[Hz]$  
  - equal phase $\phi_{in} [\text{rad}]$
Input:
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- phase $\phi_{in} [\text{rad}]$

Output:
- proportionally lower frequency $f_{out}[\text{Hz}]$
- equal phase $\phi_{in} [\text{rad}]$

Zooming effect: $x_{in}[\text{ns}] = \frac{1}{1+2^N} \cdot x_{out}[\text{ns}]$
DDMTD-based White Rabbit Phase-Locked Loop

External components

FPGA

Software in embedded CPU inside FPGA

DDMTD

DMTD clock signal

Local PTP Clock signal

L1 rx clock signal

Ext. ref. clock signal

counter

tag

tag

tag

input clock signals
DDMTD-based White Rabbit Phase-Locked Loop

External components

FPGA

DDMTD

counter

tag

tag

tag

tag

DMTD clock signal

Local PTP Clock signal

L1 rx clock signal

Ext. ref. clock signal

\[ f_{\text{DMTD}} = \frac{f_{\text{REF}}}{2^N / (\Delta + 2^N)} \text{ [Mhz]} \]

VM53S3

FRETHE025

Local PTP Clock signal

DAC

DAC

Software in embedded CPU inside FPGA

Helper PLL

Main PLL

Based on PTP offsetFromMaster

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White Rabbit clock characteristics

12/34
DDMTD-based White Rabbit Phase-Locked Loop

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White Rabbit clock characteristics 12/34
DDMTD-based White Rabbit Phase-Locked Loop

- **Introduction**
- **L1 Syntonization**
- **Current L1 Characteristics**
- **Improvement of L1**
- **PTP Synchronisation with modified L1**
- **Conclusions**

**DDMTD**

- **External components**
- **FPGA**
  - $f_{\text{REF}} [\text{Mhz}]$
  - $f_{\text{DMTD}} = f_{\text{REF}} 2^N/(\Delta+2^N) [\text{Mhz}]$

- **Software in embedded CPU inside FPGA**
  - **DDMTD**
    - **counter**
  - **PI controller**
    - $k_{ip}, k_{pf}$
  - **Helper PLL**
  - **Main PLL**
    - $k_{ip}, k_{pf}$

- **Based on PTP offset From Master**

**M. Lipiński**

White Rabbit clock characteristics 12/34
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Current L1 Characteristics

Frequency transfer using L1 syntonization in White Rabbit:

1. SyncE characteristics: ITU-T G.8262 recommendation
2. Frequency domain: phase noise measurement
3. Time domain: Allan Deviation
Characterised according to ITU-T G.8262

<table>
<thead>
<tr>
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MTIE: Maximum Time Interval Error
TDEV: Time Deviation
Characterised according to ITU-T G.8262

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Characterised according to ITU-T G.8262

White Rabbit
- Bandwidth: 30Hz
- Phase gain: 3.3dB at 16Hz

SyncE (ITU-T G.8262)
- 1-10Hz (op-1) & 0.1Hz (op-2)
- 0.2dB

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White Rabbit clock characteristics
### Characterised according to ITU-T G.8262

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Phase Noise Measurement

- Measured at:
  - 1Hz-10Hz
  - 1Hz-2kHz
  - 1Hz-100kHz
- RMS jitter:
  - GM: 4.7ps, 9.0ps, 9.1ps
  - SW1: 7.1ps, 11.0ps, 11.0ps
  - SW2: 8.8ps, 14.0ps, 14.0ps

- Grand Master, Switch 1, Switch 2
- Phase noise leaking from voltage-controlled oscillator
- Gain peaking

Phase Noise Measurement

L1 Syntonization

Current L1 Characteristics

Improvement of L1

PTP Synchronisation with modified L1

Conclusion

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Allan Deviation

Measured at | Allan Deviation (ADEV)
--- | ---
| \( \tau = 0.01 \text{s} \) | \( \tau = 0.1 \text{s} \) | \( \tau = 1 \text{s} \) | \( \tau = 10 \text{s} \) | \( \tau = 100 \text{s} \)
GM | 9.2e-10 | 1.3e-10 | 1.3e-11 | 1.3e-12 | 1.3e-13
SW1 | 7.4e-10 | 1.6e-10 | 1.9e-11 | 1.9e-12 | 1.9e-13
SW2 | 6.9e-10 | 2.1e-10 | 2.7e-11 | 2.6e-12 | 2.6e-13
Current L1 Syntonization - conclusions

There is clearly room for improvement
There is clearly room for improvement

Measurements according to ITU-T G.8262 show need for:
- improvement of transfer function
- acceptance of more jitter and wander
Current L1 Syntonization - conclusions

- There is clearly room for improvement
- Measurements according to ITU-T G.8262 show need for:
  - improvement of transfer function
  - acceptance of more jitter and wander
- Phase noise and ADEV analysis show:
  - phase noise leaking from VCO
  - poor syntonization to external source
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Phase Noise improvement by WR PLL tuning

- Modelled the impact of phase leaking from VCO
Phase Noise improvement by WR PLL tuning

- Modelled the impact of phase leaking from VCO
- Modified bandwidth of WR PLL to 200Hz
Phase Noise improvement by WR PLL tuning

- Modelled the impact of phase leaking from VCO
- Modified bandwidth of WR PLL to 200Hz
- Removed phase noise accumulation in 1Hz-10Hz range

![Graph showing phase noise improvement](image)

**Removed phase noise accumulation**

![Graph showing phase noise improvement](image)

**Graph**

- Grand Master
- Switch 1 (standard)
- VCO noise from model
- Switch 1 (modified)
Phase Noise improvement by GM modification

- Original Grandmaster input stage:
  - Internal FPGA PLL to up-convert 10MHz to 62.5MHz
  - WR PLL (SoftPLL)

![Graph showing phase noise improvement]

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<th>GM</th>
<th>SW1</th>
<th>SW2</th>
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<tr>
<td>τ=0.01s</td>
<td>Original 9.2e-10</td>
<td>Modified 1.2e-11</td>
<td>Original 1.9e-10</td>
</tr>
<tr>
<td>τ=0.1s</td>
<td>Original 1.3e-10</td>
<td>Modified 1.3e-12</td>
<td>Original 1.6e-10</td>
</tr>
<tr>
<td>τ=1s</td>
<td>Original 1.3e-11</td>
<td>Modified 4.1e-13</td>
<td>Original 1.9e-11</td>
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<tr>
<td>τ=10s</td>
<td>Original 1.3e-12</td>
<td>Modified 7.7e-14</td>
<td>Original 1.9e-12</td>
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Original Grandmaster input stage:
- Internal FPGA PLL to up-convert 10MHz to 62.5MHz
- WR PLL (SoftPLL)

New Grandmaster input stage:
- External AD9516 PLL

**Phase Noise improvement by GM modification**

![Graph showing phase noise improvement](image)

**Table: Allan Deviation (ADEV)**

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<th>(\tau=0.1\text{s})</th>
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Phase Noise improvement by GM modification

Original Grandmaster input stage:
- Internal FPGA PLL to up-convert 10MHz to 62.5MHz
- WR PLL (SoftPLL)

New Grandmaster input stage:
- External AD9516 PLL

Result:
- better phase noise profile < 1kHz
- spurs visible above 1kHz
- GM and WR PLL modifications together significantly improve Allan Deviation

**Allan Deviation (ADEV)**

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Improvement at lower frequencies
Spurs at higher frequencies
Modifications to achieve SyncE compliance

Software modifications of the WR PLL

- Reduced bandwidth to 5Hz
- Implemented Multiple Unit Interval tracking of error when large zero-mean wander
## SyncE-compliment ITU-T G.8262 characteristics

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<td>Wander transfer</td>
<td>Passed (op-1)</td>
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**Image:**
- [Calnex Paragon-X](image1.png)
- [CNT-91 Time Interval Counter](image2.png)
- [Agilent 33250A traffic generator](image3.png)
## SyncE-compliment ITU-T G.8262 characteristics

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SyncE-compliment ITU-T G.8262 characteristics

**White Rabbit**
- Bandwidth: 5Hz
- Phase gain: < 0.2dB at 0.7Hz

**SyncE (ITU-T G.8262)**
- Bandwidth: 1-10Hz (op-1)
- Phase gain: 0.2dB
# SyncE-compliment ITU-T G.8262 characteristics

<table>
<thead>
<tr>
<th>Test name</th>
<th>Test name</th>
<th>Measured values</th>
<th>Measurement device</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency offset</td>
<td>Passed</td>
<td>4.256ppm</td>
<td>Calnex Paragon-X</td>
</tr>
<tr>
<td>Pull-in range</td>
<td>Passed</td>
<td>8ppm</td>
<td></td>
</tr>
<tr>
<td>Hold-in range</td>
<td>Passed</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pull-out range</td>
<td>Passed</td>
<td>8.8ppm</td>
<td></td>
</tr>
<tr>
<td>Jitter generation</td>
<td>Passed</td>
<td>pk-pk: 0.01UI RMS:&lt; 0.01UI</td>
<td></td>
</tr>
<tr>
<td>Jitter tolerance</td>
<td>Passed</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wander generation</td>
<td>Passed</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wander tolerance</td>
<td>Passed</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wander transfer</td>
<td>Passed</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- Measurement device: Calnex Paragon-X
- Measurement device: CNT-91 Time Interval Counter
- Measurement device: Agilent 33250A traffic generator
SyncE-compliment ITU-T G.8262 characteristics

MTIE: Maximum Time Interval Error
TDEV: Time Deviation
Outline

1. Introduction to White Rabbit
2. L1 Syntonization in White Rabbit
3. Current L1 Syntonization Characteristics
4. Improvement of L1 Syntonization
5. PTP Synchronisation with the Modified L1 Syntonization
6. Conclusions
Synchronisation in a Long Cascade of WR Switches

Mean offset from master

Standard deviation

GM: current | modified
Currently used SoftPLL:
200Hz bandwidth SoftPLL:
SyncE-compliant SoftPLL:
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White Rabbit clock characteristics
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White Rabbit clock characteristics 32/34
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Conclusions

Frequency transfer using L1 Syntonization in WR:

- Phase noise: significantly improved
- SyncE characteristics:
  - compliance with op-1 achieved (VM53S3 ±2.5ppm)
  - only software modifications
  - sub-ns accuracy possible
- Results considered in new WR hardware designs, thus further improvements are expected
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L1 Syntonization characterised with to ITU-T G.8262

1. Cs → Paragon-X (P1, P2) → DUT (WR Switch 1)
   - Cs
   - 10 MHz
   - 1 GbE over fiber

2. Cs → Paragon-X (P1, P2) → DUT (WR Switch 1)
   - Cs
   - 10 MHz
   - 1 GbE over fiber

3. Cs → CNT-91 (REF, IN) → DUT (WR Switch)
   - Cs
   - 10 MHz
   - 1 GbE over fiber

4. Cs → CNT-91 (REF, IN) → DUT (WR Switch)
   - Cs
   - 10 MHz
   - 1 GbE over fiber

   Agilent 33250A
   - 10 MHz
   - Phase-modulated

   Grandmaster
   - 10 MHz
   - SFP

   DUT (WR Switch)
   - 10 MHz
   - SFP

   DUT (WR Switch)
   - 10 MHz
   - SFP