White Rabbit
a PTP Application for Robust Sub-nanosecond Synchronization

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What is White Rabbit?

- Accelerator’s control and timing (GSI, CERN),
- Based on well-known technologies/standards,
- Open Hardware and Open Software,
- International collaboration,
- Main features:
  - transparent, **high-accuracy** time distribution,
  - low-latency, **deterministic** data delivery,
  - designed for **high reliability**,
  - plug & play.
Synchronization with **sub-ns** accuracy over fiber,
Combination of
  - Precision Time Protocol (**PTP**) synchronization,
  - Synchronous Ethernet (**SyncE**) syntonization,
  - Digital Dual-Mixer Time Difference (**DDMTD**) phase detection,

**WR Link:**

![Diagram of WR Link](image)
Time Distribution in White Rabbit

A White Rabbit Network

grandmaster clock

WR boundary clock

WR ordinary clock

WR boundary clock

WR ordinary clock

WR boundary clock

WR ordinary clock

WR boundary clock

WR ordinary clock
PTP is OK but ...

What are the issues... and ... how we address them

PTP-base syntonization ⇒ SyncE

limited precision and resolution ⇒ SyncE

unknown link asymmetry ⇒ DDTMD phase detection

WR extension to PTP \(\text{WRPTP}\) for extra data exchange and logic
**Link Delay Model**

\[ \text{delay}_{ms} = \Delta_{txm} + \delta_{ms} + \Delta_{rxs} \]
\[ \text{delay}_{sm} = \Delta_{txs} + \delta_{sm} + \Delta_{rxm} \]

**Relative Delay Coefficient (\(\alpha\))**

for 1000base-X over a Single-mode Optical Fibre

\[ \delta_{ms} = (1 + \alpha) \delta_{sm} \]
Link Delay Model: fiber optic solution

Solution for Ethernet over a Single-mode Optical Fiber

\[
\text{asymmetry} = \Delta_{tx} + \Delta_{rx} - \frac{\Delta - \alpha \mu + \alpha \Delta}{2 + \alpha}
\]
Fine Delay Measurement

Solution for Ethernet over a Single-mode Optical Fiber

\[ \text{asymmetry} = \Delta_{txm} + \Delta_{rxs} - \frac{\Delta - \alpha \mu + \alpha \Delta}{2 + \alpha} \]
Fine Delay Measurement

Introduction
Why not standard PTP?
Link Delay Model
H/W for WR
WRPTP
Status
Conclusions

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Fixed Delays Measurement

Solution for Ethernet over a Single-mode Optical Fiber

\[ asymmetry = \Delta_{tx} + \Delta_{rx} - \frac{\Delta - \alpha \mu + \alpha \Delta}{2 + \alpha} \]
Fixed Delays Measurement

- PHY
- RxCLK
- TxCLK
- Buffer
- Δ rx
- Δ tx
- Phase detector
- 125 MHz
White Rabbit extension to PTP (WRPTP)

- WR-peers recognition,
- Calibration,
- Exchange of WR-data,
- Support of redundancy.
Exchange of WR-data

- WR Announce MSGs
  - Announce TLV
- WR Signaling MSGs
  - Header TLV
- Request-response MSGs

PTP Master

PTP Slave
WR Link Setup

- Frequency locking
- Calibration
- Exchange of WR-parameters
- WR Finite State Machine (FSM)
- WR Signaling Messages
Clock Recovery System and modified BMC

WR Clock Recovery System

Reference channels

DDMTD

DDMTD

DDMTD

Feedback channel

Phase and freq error detection

Phase and freq error detection

MUX

PI

VCTCXO

ref clk

ref clk 1

ref clk N

WRPTP phase shift

Switch-over

Switch

GPS

Switch

Switch

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Test bed

stable oscillator

Symmetricom CS4200 Cesium beam clock

WR Switch (master)

10 MHz

WR Switch (slave 3)

UP0

REF clock

PPS out

WR Switch (slave 2)

DP0 UP0

REF clock

PPS out

WR Switch (slave 1)

DP0 UP0

REF clock

PPS out

hot-air gun

5 km - long rolls of fiber G.652

CH1 CH2 Ch3 Ch4

LeCroy WavePro 7300A oscilloscope

clock offset analysis

IN

PSD

Agilent E5052 Signal Source Analyzer

phase noise analysis

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Test results

Histogram of offsets between master and each slave

- Slave 3 (C4)
  - mean = -135.25 ps
  - sdev = 6.14 ps

- Slave 2 (C3)
  - mean = 24.67 ps
  - sdev = 5.30 ps

- Slave 1 (C2)
  - mean = 161.86 ps
  - sdev = 5.45 ps

Matlab plot of collected data

Oscilloscope screenshot

<table>
<thead>
<tr>
<th>Measure</th>
<th>P1: skew(C1,C2)</th>
<th>P2: skew(C1,C3)</th>
<th>P3: skew(C1,C4)</th>
</tr>
</thead>
<tbody>
<tr>
<td>value</td>
<td>176 ps</td>
<td>42 ps</td>
<td>-117 ps</td>
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<tr>
<td>mean</td>
<td>161.86 ps</td>
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<td>3 ps</td>
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<tr>
<td>max</td>
<td>183 ps</td>
<td>48 ps</td>
<td>-109 ps</td>
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<tr>
<td>sdev</td>
<td>5.45 ps</td>
<td>5.30 ps</td>
<td>6.14 ps</td>
</tr>
<tr>
<td>num</td>
<td>5.9764e+3</td>
<td>5.9764e+3</td>
<td>5.9757e+3</td>
</tr>
</tbody>
</table>

Timebase: 0 ps
200 ps/div
20.0 S
10 GS/s
White Rabbit Switch (V2)

- Central element of WR network
- Fully custom design, designed from scratch
- 10 1000Base-LX ports
- capable of driving 10 km of SM fiber
WR-compliant Hardware Kit

Co-HT FMC-based Hardware Kit:
- FMCs (FPGA Mezzanine Cards) with ADCs, DACs, TDCs, fine delays, digital I/O
- Carrier boards in PCI-Express, VME and uTCA formats
- All carriers are equipped with a White Rabbit port
Conclusions

- Promising results
- Robust synchronization:
  - high precision - rock solid synchronization
  - support of seamless switchover
- Benefits from compatibility with standards:
  - wide support
  - commercial feasibility
  - hybrid networks
  - general-purpose solution
- Great interest from many institutes and companies
thank you

Any questions?