FPGA with 'White Rabbit PTP Core'

FPGA GTP

FPGA I/O

Clock generator

Detailed information see "http://www.ohwr.org/projects/white-rabbit"
**VCCO_0 = 2.5V or 3.3V**

IC100A
XCS6LX45T-3FGG484C

**FPGA bank 0**

**System:** White Rabbit Node Reference Design (upgrade of existing system)

**Board:** -

**Created:** 07-MAR-2012, Daniel Florin  
**Revision:** -

**Modified:** 08-MAY-2012, Daniel Florin  
**Sheet:** 4 of 5

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Based on Simple PCIe FMC carrier (SPEC), http://www.ohwr.org/projects/spec

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