

White Rabbit status

Javier Serrano

CERN, Geneva, Switzerland

14 April 2011

- 1 Background
 - Basic intro
 - Some words about the collaboration
- 2 Ongoing efforts
 - WR switch
 - WR node
 - Other
- 3 Stakeholders
- 4 Outlook
 - Short term
 - Medium term

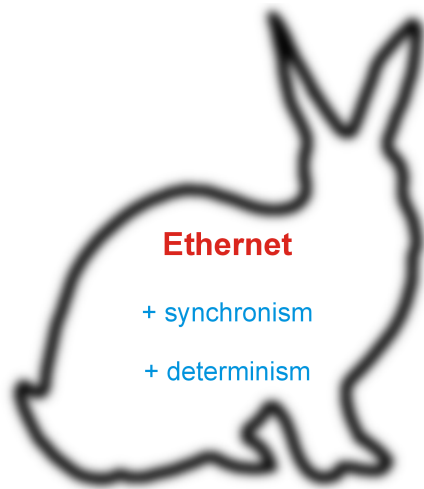
Disclaimer

This is starting to be a really big project. If I forget your name in some contribution, just shout.

Outline

- 1 **Background**
 - Basic intro
 - Some words about the collaboration
- 2 Ongoing efforts
 - WR switch
 - WR node
 - Other
- 3 Stakeholders
- 4 Outlook
 - Short term
 - Medium term

What is White Rabbit?



What is White Rabbit?

An **extension** to **Ethernet** which provides:

- **Synchronous mode** (Sync-E) - common clock for physical layer in entire network, allowing for precise time and frequency transfer.
- **Deterministic routing** latency - a guarantee that packet transmission delay between two stations will never exceed a certain boundary.

Design goals

Scalability

Up to 2000 nodes.

Range

10 km fiber links.

Accuracy and precision

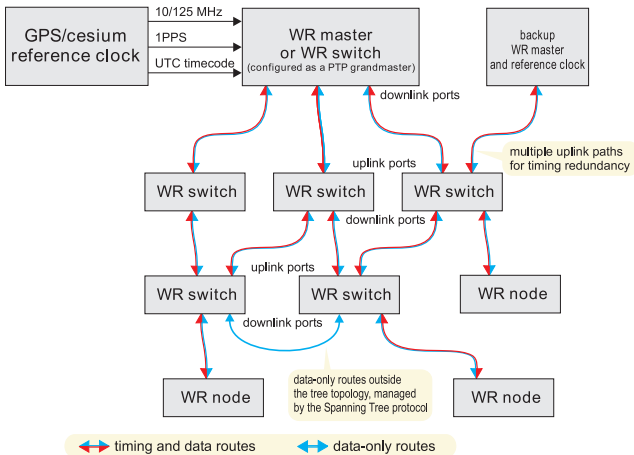
1 ns time synchronization accuracy, 20 ps jitter.

Technologies used in White Rabbit

Sub-nanosecond synchronization in WR is achieved by using the following three technologies together:

- Precision Time Protocol (IEEE1588).
- Synchronous Ethernet.
- DDMTD phase tracking.

Network topology



Quick background on the collaboration

Started by CERN, then others joined

- GSI came on board very soon.
- Spanish government funded two companies to work with us.
- Other companies, EU projects, etc. have expressed interest (more later).

A collaborative open effort from the start

- Uses the Open Hardware Repository.
- Big effort to keep communication flowing (mailing list, jabber meetings . . .).

Decision process

Very much inspired by FOSS

- One benevolent dictator. Well, not even.
- Anybody can choose not to follow.
- People pick what they want from OHR.

Some strong recommendations

- Publish specs and documentation.
- VHDL and C coding guidelines.
- PCB development practices.
- Open source tools whenever possible.
- Common HW platforms for development.
- CERN Open Hardware Licence for PCBs, LGPL for HDL, GPL v2 for Linux kernel code.

Benefits and losses

Benefits

- Huge pot of manpower available. Largely offsets management effort invested.
- Many nice unexpected surprises in terms of external talent.
- Great reality check for lack of CERNness, GSIness, etc. in solutions: this is important for companies, which are key in the OH concept.
- Fun.

Losses

∅

Outline

- 1 Background
 - Basic intro
 - Some words about the collaboration
- 2 Ongoing efforts
 - WR switch
 - WR node
 - Other
- 3 Stakeholders
- 4 Outlook
 - Short term
 - Medium term

Switch v3 hardware

MCH by Seven Solutions

- Schematics finished, PCB layout started.
- Talk by Javier Díaz.

Minibackplane by Tomek

- Will support both fiber and copper.
- Someone needs to work on copper (volunteers?!). This is important because SFPs are expensive and not always needed.
- Talk by Tom.

Switch SW and testing

See talk by Alessandro

Code clean-up

- A standard software kit people can download and install easily.
- Things done in kosher Linux way.
- A Git repo in a dedicated sub-project in OHR.

The Octopus

- Send frames to ports of a switch and see how it behaves.
- Add time-tags later for measuring latencies.
- Port to switch v3 when it becomes available

Switch management

See talk by Integrasys

Specification

- Follow the appropriate standards (IEEE, RFCs ...).
- Focuses on fault, configuration and performance management.

Future developments

- Command Line Interface for local management.
- SNMP agent for remote management.

WR node specification

Main goals

- Try to see how far we can push common ground. Target: customize behavior only with microcode running on an embedded CPU.
- Many platforms: PCIe, VME64x, PXIe ...
- Start with functional, move to technical spec later.
- Leverage NI experience in providing a nice interface to the users.

Collaboration between Tibor, César and Jean-Claude

- Jean-Claude is in charge of CERN's timing system, Tibor manages GSI's.
- See presentation by Tibor.

WR PTP core

Main goals

- Provide a re-usable core that takes WR on one side and provides phase-compensated time, clock signal and payloads on the other.
- Re-write PTP daemon so same software base can run in the little embedded CPU inside the core and in desktop Linux systems.

People

- Greg D. on the HDL, Alessandro and Marco on the daemon.
- Tom's help on both sides.

Etherbone

Main goals

- Push the customization layer up by introducing another generic layer on top of WR.
- Very elegant: the whole network is one huge memory map. All messages are reads and writes into some node address space.
- Sits on top of UDP/IP. UDP multi-cast behaves as expected, triggering multiple WB accesses at the same time in many nodes.

Started at CERN, now developed in GSI

- Wesley on the spec and C code, César on C++ code, Marcus on the Delphi GUI, Mathias on the HDL.
- See presentation and demo later.

Soft CPU core evaluation

Main goals

- Look for a good candidate to be used as general computing engine in WR nodes.
- Strike a good balance in size (might be instantiated multiple times), speed, openness, gcc support, available debugging tools . . .

Effort taken completely by Wesley

- He's even working on a generic debugging tool.
- See presentation and demo later.

Robustness and FEC

Main goals

- Make sure a frame goes from point A to point B, with no re-tries.
- Needs an understanding of the processes which can impair communication.

Collaboration between César and Maciej

- Maciej focusing on HDL, César on C code.
- Both preparing a comprehensive document (see presentation later).

Plans for a PXIe node from NI

Main goal

- Provide WR interfacing to PXIe users.

Ideas go both ways

- Some ideas from the SPEC board should be applicable.
- NI's experience in providing clean generic APIs to users will be very valuable for us.

Outline

- 1 Background
 - Basic intro
 - Some words about the collaboration
- 2 Ongoing efforts
 - WR switch
 - WR node
 - Other
- 3 Stakeholders
- 4 Outlook
 - Short term
 - Medium term

Different degrees of involvement

Core team or fully committed

CERN, GSI (and Cosylab), Alessandro & co., Integrasys, Seven Solutions, National Instruments, Elproma (with Creotech).

Seriously considering it for future projects

Nikhef (for KM3NeT), Tsinghua University (for LHAASO).

Have shown some interest

ESS Bilbao, ESS Lund, Instrumentation Technologies, CTA, EISCAT (through NI), ITER, Siemens.

Outline

- 1 Background
 - Basic intro
 - Some words about the collaboration
- 2 Ongoing efforts
 - WR switch
 - WR node
 - Other
- 3 Stakeholders
- 4 Outlook
 - Short term
 - Medium term

Fifth workshop after the Summer

- Hopefully with v3 switches in our hands.
- Program of work to be discussed today (15:00-16:00).

Future Outlook

Get more people on board: the more the merrier

- Improves peer review.
- Drives down prices of HW.
- More fun.

Prove COTS and openness are not contradictory

- Strong partnership with companies in the core team.
- Other companies have shown interest in WR-enabling their gear.

Some final thoughts

- The greatest asset of WR is the people. Project success can be attributed largely to good luck, i.e. to stumbling across the right individuals at the right times and places.
- All this has not needed any formal agreement so far, and it would be great to stay that way.