White Rabbit

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CERN BE-CO
Hardware and Timing section

European Frequency and Time Seminar
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1. Introduction to Open Hardware
2. Introduction to White Rabbit
3. Applications
4. Technology
5. Performance
6. Current developments
7. Conclusions
Outline

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There is an OSHW definition!

Check out http://www.oshwa.org/definition/

- Inspired by the Open Source definition for software.
- Focuses on ensuring freedom to study, modify, distribute, make and sell designs or hardware based on those designs.
- Now we know exactly what we mean when we say OSHW!
## Dispelling the commercial vs open myth

<table>
<thead>
<tr>
<th>Open</th>
<th>Proprietary</th>
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<tbody>
<tr>
<td><strong>Commercial</strong></td>
<td><strong>Non-commercial</strong></td>
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<tr>
<td>Winning combination. Best of both worlds.</td>
<td>Whole support burden falls on developers. Not scalable.</td>
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<tr>
<td>Vendor lock-in.</td>
<td>Dedicated non-reusable projects.</td>
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Why we use Open Hardware 1/2

Get a design just the way we want it.
We specify fully the design.

Peer review
Get your design reviewed by experts all around the world, including companies!

Design re-use
When it's Open, people are more likely to re-use it.

Healthier relationship with companies
No vendor-locked situations. Companies selected solely on the basis of technical excellence, good support and price.
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Why we use Open Hardware 2/2

- Dissemination of Knowledge is one of CERN's key missions!
- Spend money where you or your funding agencies want.
- Makes life easier for public institutions.
- Opens the door to smaller companies with good local support.
Why we use Open Hardware 2/2

Dissemination of Knowledge

One of CERN’s key missions!
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White Rabbit: an *extension* of Ethernet

- Bandwidth: 1 Gbps
- Single fiber medium
- Up to 10 km links
- WR Switch: 18 ports
- Allows non-WR Devices
- Ethernet features (VLAN) & protocols (SNMP)
White Rabbit: an *extension* of Ethernet

Two separate services (enhancements to Ethernet) provided by WR:

1. **Synchronization:**
   - accuracy better than 1 ns
   - precision in the tens of ps

2. **Deterministic, reliable and low-latency Control Data delivery**
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White Rabbit application examples

- **Under development:**
  - **CERN and GSI**
  - The Large High Altitude Air Shower Observatory (China)
  - European deep-sea research infrastructure (KM3NET)

- **Under evaluation:**
  - Cherenkov Telescope Array
  - Long distance Time Transfer
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  - **Long distance Time Transfer**
Precision Time Protocol (IEEE 1588)

- Frame-based synchronization protocol.
- Synchronizes local clock with the master clock.
- Link delay evaluated by measuring and exchanging frames with tx/rx timestamps.
Common clock for the entire network

- All network devices use the same physical layer clock.
- Clock is encoded in the Ethernet carrier and recovered by the receiver chip.
- Phase detection allows sub-ns delay measurement.
Digital Dual Mixer Time Difference
DDMTD

\[ f_{PLL} = \frac{n}{n+1} f_{clkA} \]

clk\_A \hspace{2cm} D \hspace{2cm} Q \hspace{2cm} \text{helper PLL}

\[ f_{PLL} \]

clk\_B \hspace{2cm} D \hspace{2cm} Q \hspace{2cm} \text{degilcher & pulse shaping}

\[ \phi \]
Link delay model
White Rabbit Switch

- Central element of WR network
- Original design optimized for timing, designed from scratch
- 18 1000BASE-BX10 ports
- Open design (H/W and S/W)
- Commercially available
Simplified block diagram of WR switch
WR Node: SPEC board

FMC-based Hardware Kit

- All carrier cards are equipped with a White Rabbit port.
- Mezzanines can use the accurate clock signal and “TAI” (synchronous sampling clock, trigger time tag, ...).
White Rabbit PTP Core

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WR time transfer performance: test setup
WR time transfer performance: test results

Histogram of offsets between master and each slave

Master (CH1)

Slave 2 (CH3)
mean = 24.67 ps
sdev = 5.30 ps

Slave 3 (CH4)
mean = -135.25 ps
sdev = 6.14 ps

Slave 1 (CH2)
mean = 161.86 ps
sdev = 5.45 ps

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## Determinism

You know what the frame latency will be because you have the VHDL source of the switch FPGA. IEEE 802.1Q headers supported.

Low latency

Cut-through design. Current latency through the switch is \( \sim 3\mu s \) without much effort. Good for (some) feedback systems.

Suitable for time-based control and data acquisition combining a low upper bound in latency and a good common notion of time.
Deterministic by design

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Standardization
IEEE 1588 just opened the revision process for the PTP standard, which includes an effort on high accuracy. WR is represented in the working group.

Switches and nodes are commercially available
Work for the switch now revolves around better diagnostics and remote management.

Robustness
Based on redundant information and fast switch-over between redundant switches.
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Ethernet Clock distribution a.k.a. Distributed DDS

Distributed Direct Digital Synthesis

- Replaces dozens of cables with a single fiber.
- Works over big distances without degrading signal quality.
- Can provide various clocks (RF of many rings and linacs) with a single, standard link.
Distributed oscilloscope

- Common clock in entire network: no skew between ADCs.
- Ability to sample with different clocks via Distributed DDS.
- External triggers can be time tagged with a TDC and used to reconstruct the original time base in the operator’s PC.
Support for redundancy

WR Clock Recovery System

- Reference channels
  - DDMTD
  - DDMTD
  - DDMTD

- Feedback channel
  - DDMTD

- Phase and freq error detection
  - Phase and freq error detection
  - Phase and freq error detection

- Switch-over
  - WRPTP phase shift

- Feedback clk

- MUX
- PI
- VCTCXO

- ref clk 1
- ref clk N
Summary

A novel networking technology allowing precise synchronization and deterministic data transfer.

A collaborative distributed effort based on open source hardware and software, with an active, enthusiastic community. Everybody is welcome to join!

A versatile working solution for general control and data acquisition systems.

For more information see http://www.ohwr.org/projects/white-rabbit/wiki
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