**White Rabbit**

a PTP application for sub-ns synchronization

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March 2012
Outline

1. Introduction
2. Timestamps
3. Link Asymmetry
4. PTP&SyncE
5. WRPTP
6. Status
7. Conclusions
What is White Rabbit?

- Accelerator’s control and timing (GSI, CERN)
- Based on well-known technologies
- Open Hardware and Open Software
- International collaboration (multi-lab, multi-company)
- Main features:
  - transparent, **high-accuracy** time distribution
  - low-latency, **deterministic** data delivery
  - designed for **high reliability**
  - plug & play.
- Other applications: Gran Sasso, Cherenkov Telescope Array, The Large High Altitude Air Shower Observatory, The Cubic Kilometre Neutrino Telescope
Synchronization with **sub-ns** accuracy over fiber

Combination of

- Precision Time Protocol (**PTP**) synchronization
- Synchronous Ethernet (**SyncE**) syntonization
- Digital Dual-Mixer Time Difference (**DDMTD**) phase detection

**WR Link:**

![Diagram showing Time Distribution in White Rabbit](image)
PTP is OK but ...

What are the issues... and ... how we address them

PTP-base syntonization $\Rightarrow$ SyncE

limited precision and resolution $\Rightarrow$ SyncE

unknown link asymmetry $\Rightarrow$ DDTMD phase detection

WR extension to PTP (WRPTP) for extra data exchange and logic
Fine Delay Measurement

a) Reference clock
   1. Reference clock
   2. Transmitter \( \Delta_{txm} \)
   3. Receiver \( \Delta_{rxm} \)
   4. Slave recovered clock

b) Offset
   1. Offset \( \text{offset}_{MS} \)
   2. Delay \( \text{delay}_{MS} \)
   3. Phase \( \text{phase}_{MS} \)

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WD18PP: White Rabbit 6/24
Link Asymmetry

\[ \mu = \frac{(t_4 - t_1) - (t_3 - t_2)}{2} \]

\[ \text{delay}_{ms} = \mu + \text{asymmetry} \]

\[ \text{offset}_{ms} = t_2 - (t_1 + \text{delay}_{ms}) \]
Link Delay Model

\[
\text{delay}_{ms} = \Delta_{txm} + \delta_{ms} + \Delta_{rxs} \\
\text{delay}_{sm} = \Delta_{txs} + \delta_{sm} + \Delta_{rxm}
\]

Relative Delay Coefficient (\(\alpha\))
for 1000BASE-BX10 over a Single-mode Optical Fiber

\[
\delta_{ms} = (1 + \alpha) \delta_{sm}
\]
Fixed Delays

Asymmetry sources: circuit ↔ SFP ↔ Serdes ↔ fiber
Link Delay Model: fiber optic solution

Solution for Ethernet over a Single-mode Optical Fiber

\[
\text{asymmetry} = \Delta_{tx} + \Delta_{rx} - \frac{\Delta - \alpha \mu + \alpha \Delta}{2 + \alpha}
\]
PTP and SyncE in WR

- Compatibility with PTP verified
- Compatibility with SyncE for further study
- Frequency distribution aligned with PTP’s logic topology
- PTP’s Announce messages used for WR-peers recognition
White Rabbit extension to PTP (WRPTP)

- WR-peers recognition
- Calibration (fixed delays measurement)
- Exchange of WR-data
- Support of redundancy
- Mapping over IEEE802.3/Ethernet
WR-peer recognition and WR-data exchange

Two WR devices

WR and non-WR device
WR Link Setup

- Frequency locking
- Calibration
- Exchange of WR-parameters
- WR Finite State Machine
- WR Signaling Messages
Modified Best Master Clock Algorithm (mBMCA)
Clock Recovery System and mBMCA

WR Clock Recovery System

Reference channels

Feedback channel

Phase and freq error detection

Switch M M

GPS

Switch M M

Switch M M

ref clk 1

ref clk N

反馈 clk

freq error phase error

MUX

PI

VCTCXO

Switch sS pS

Switch sS pS

ref clk
Test bed

stable oscillator

Symmetricom CS4200 Cesium beam clock

WR Switch (master)

REF clock
PPS out

10 MHz

5 km - long rolls of fiber G.652

WR Switch (slave 1)

REF clock
PPS out

WR Switch (slave 2)

REF clock
PPS out

UP0

WR Switch (slave 3)

REF clock
PPS out

UP0

10 M in

CH1 CH2
LeCroy WavePro 7300A oscilloscope

Ch3 Ch4
clock offset analysis

IN

Agilent E5052 Signal Source Analyzer

phase noise analysis
Test results

Histogram of offsets between master and each slave:

- **Slave 3 (C4)**: mean = -135.25 ps, sdev = 6.14 ps
- **Slave 2 (C3)**: mean = 24.67 ps, sdev = 5.30 ps
- **Slave 1 (C2)**: mean = 161.86 ps, sdev = 5.45 ps

Matlab plot of collected data:

<table>
<thead>
<tr>
<th>Measure</th>
<th>P1: skew(C1,C2)</th>
<th>P2: skew(C1,C3)</th>
<th>P3: skew(C1,C4)</th>
</tr>
</thead>
<tbody>
<tr>
<td>value</td>
<td>176 ps</td>
<td>42 ps</td>
<td>-117 ps</td>
</tr>
<tr>
<td>mean</td>
<td>161.86 ps</td>
<td>24.67 ps</td>
<td>-135.25 ps</td>
</tr>
<tr>
<td>min</td>
<td>141 ps</td>
<td>3 ps</td>
<td>-846 ps</td>
</tr>
<tr>
<td>max</td>
<td>183 ps</td>
<td>48 ps</td>
<td>-109 ps</td>
</tr>
<tr>
<td>sdev</td>
<td>5.45 ps</td>
<td>5.30 ps</td>
<td>6.14 ps</td>
</tr>
<tr>
<td>num</td>
<td>5.9764e+3</td>
<td>5.9764e+3</td>
<td>5.9757e+3</td>
</tr>
</tbody>
</table>

Oscilloscope screenshot:
White Rabbit Switch (V3)

- Central element of WR network
- Original design optimized for timing, designed from scratch
- 18 1000BASE-BX10 ports
- Capable of driving 10 km of SM fiber
Conclusions

- Excellent results:
  - $< 1\text{ns}$ accuracy and $< 10\text{ps}$ precision over 15km
- According to ISPCS2010 Plug Fest results:
  
  *White Rabbit is the most accurate PTP implementation in the World!*

- Robust synchronization:
  - high precision - rock solid synchronization
  - support for seamless switchover

- Benefits from compatibility with standards:
  - wide support
  - commercial feasibility
  - hybrid networks
  - general-purpose solution

- Great interest from many institutes and companies
Thank you

Any questions?
Fixed Delays Measurement

11000000111110000001111100

- Buffer
- Δ
- Rx
- Tx
- PHY
- RxCLK
- TxCLOCK
- 125 MHz
- Phase detector
- Δ
- tx
- Δ
- rx

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WD18PP: White Rabbit
Proposed topology of WR network at CERN

- CCR (Prevesin)
  - Data Masters (WR Nodes)
  - Timing Masters
  - Time source

- ISOLDE
  - WR Network Backbone

- LHC Network
  - LIC Network (Meyrin)

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WR-compliant Hardware Kit

Co-HT FMC-based Hardware Kit:

- FMCs (FPGA Mezzanine Cards) with ADCs, DACs, TDCs, fine delays, digital I/O
- Carrier boards in PCI-Express, VME and uTCA formats
- All carriers are equipped with a White Rabbit port