Small or medium-scale focused research project (STREP) proposal
ICT Call 5
FP7-ICT-2009-5

Large-scale Ethernet Control Network Extension

White Rabbit

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<th>Participant no.</th>
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<td>1 (Coord.)</td>
<td>European Organization for Nuclear Research</td>
<td>CERN</td>
<td>International Organisation</td>
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<td>Österreichische Akademie der Wissenschaften</td>
<td>AAS</td>
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<td>3</td>
<td>GSI Helmholtzzentrum für Schwerionenforschung GmbH</td>
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<td>University of Brescia</td>
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<td>Austria</td>
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<td>9</td>
<td>Hirschmann Automation and Control GmbH</td>
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<td>Germany</td>
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Work program topics addressed: ICT-2009.3.5 Engineering of Networked Monitoring and Control systems.
c) Control of large-scale systems

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Abstract

Existing control systems struggle when they need to be used in large and complex networks. They are not scalable to support thousands of nodes and cannot be used over large distances as their real-time performance level would severely be reduced. In addition, these systems do not easily allow dynamic changes to the number of nodes. Consequently, existing systems do not meet the needs of many potential applications such as large scientific instruments, wireless location systems, powerful monitoring systems for energy distribution and structural monitoring.

We propose a system capable of enabling existing and future Ethernet networks with sub-nanosecond synchronization and deterministic traffic handling in more than 2000 nodes with cabling lengths in the order of 10 km. This is achieved by guaranteeing delivery times and timing accuracy at layer 2 of the OSI Reference Model. It will provide a pro-active plug & play platform that can boost the performance of existing higher layer protocols without any configuration effort. These goals can be met by basic research on innovative techniques for increased performance while maintaining standards compliance and interoperability. The resulting architecture allows for the design of flexible large-scale complex control systems while its novel properties open opportunities for developing innovative process control algorithms and monitoring applications.

The project consortium that will develop the solution consists of a carefully selected and complementary team which includes some of the world-leading companies in process automation and data acquisition, as well as large scientific laboratories and specialised SMEs.

The target outcome of this effort will be a tangible modernised networked physical infrastructure that enables the optimal operation of innovative large-scale dynamic systems as aimed for by FP7 Objective ICT-2009.3.5c.
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<tr>
<td>ASIC</td>
<td>Application Specific Integrated Circuit</td>
</tr>
<tr>
<td>COTS</td>
<td>Commercial Off-The-Shelf</td>
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<tr>
<td>CPU</td>
<td>Central Processing Unit</td>
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<td>CRC</td>
<td>Cyclic Redundancy Check</td>
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<td>DCS</td>
<td>Distributed Control Systems</td>
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<tr>
<td>FEC</td>
<td>Forward Error Correction</td>
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<tr>
<td>FPGA</td>
<td>Field Programmable Gate Array</td>
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<tr>
<td>GPS</td>
<td>Global Positioning System</td>
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<td>HDL</td>
<td>Hardware Description Language</td>
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<tr>
<td>IDE</td>
<td>Integrated Development Environment</td>
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<td>IEC</td>
<td>International Electrotechnical Commission</td>
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<td>IGMP</td>
<td>Internet Group Management Protocol</td>
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<td>IP</td>
<td>Internet Protocol</td>
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<td>IPR</td>
<td>Intellectual Property Rights</td>
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<tr>
<td>ISO</td>
<td>International Organisation for Standardisation</td>
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<tr>
<td>LHC</td>
<td>Large Hadron Collider</td>
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<td>LT</td>
<td>Luby Transform</td>
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<td>MAC</td>
<td>Media Access Control</td>
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<tr>
<td>MTU</td>
<td>Maximum Transmission Unit</td>
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<tr>
<td>OHL</td>
<td>Open Hardware License</td>
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<td>OHR</td>
<td>Open Hardware Repository</td>
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<td>OSI</td>
<td>Open Systems Interconnection</td>
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<tr>
<td>PCI</td>
<td>Peripheral Component Interconnect</td>
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<td>PLL</td>
<td>Phase Locked Loop</td>
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<td>PPS</td>
<td>Pulse Per Second</td>
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<tr>
<td>PTP</td>
<td>Precision Time Protocol</td>
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<td>PXI</td>
<td>PCI eXtensions for Instrumentation</td>
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<td>QoS</td>
<td>Quality-of-Service</td>
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<tr>
<td>(R)STP</td>
<td>(Rapid) Spanning Tree Protocol</td>
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<td>SME</td>
<td>Small and Medium Enterprises</td>
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<tr>
<td>STP</td>
<td>Spanning Tree Protocol</td>
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<tr>
<td>TCP</td>
<td>Transport Control Protocol</td>
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<td>TDMA</td>
<td>Time-Division Multiple Access</td>
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<tr>
<td>TTA</td>
<td>Time-Triggered Architecture</td>
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<tr>
<td>TTP</td>
<td>Time-Triggered Protocol</td>
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<tr>
<td>UDP</td>
<td>User Datagram Protocol</td>
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<tr>
<td>UTC</td>
<td>Coordinated Universal Time</td>
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<tr>
<td>VHDL</td>
<td>Very high speed integrated circuits Hardware Description Language</td>
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1 Scientific and/or technical quality, relevant to the topics addressed by the call

Under FP7, ICT research activities cover strategic priorities in the area of European industrial and technological leadership. FP7 ICT Challenge 3 specifically focuses on “engineering cooperative networked control systems and optimisation and decision support methods and tools which are used to modernise physical infrastructures, to control complex processes in manufacturing, or to monitor and control systems performance”.

The White Rabbit project matches this challenge as it will incorporate the advantages of existing industrial real-time networks to build a new, open and standardised system for control and monitoring of large-scale systems.

1.1 Concept and objectives

The White Rabbit project will provide:

- a large-scale monitoring and control network with all nodes synchronised to a sub-nanosecond level even when spread over tens of kilometers.
- a scalable and modular platform that reconfigures automatically.
- deterministic delivery of high-priority messages with a low and strictly limited delay.
- a pro-active method to transmit important messages robustly under fault conditions.

Many application areas for real-time communication systems like factory automation, network control or distributed data acquisition systems require the execution of operations with tight time constraints. This becomes even more complicated in large-scale distributed systems since the large distances between nodes also give long transmission delays. The latter then cause high response times for queries to network nodes and are also the reason for the usage of inefficient guard times to avoid data collisions on a single trunk.

The objective of the proposed project is to overcome the limitations of current real-time networks when targeting physically large-scale distributed control networks. The foreseen achievements will cover a highly accurate agreement of time between the nodes over large areas which allows for precise coordination of action and monitoring of all nodes in a network. Additionally, the architecture will fulfil necessary services to meet the requirements of a control network by guaranteeing timely deterministic delivery of messages.

The project aims for long term availability which is assured by the fact that the well-established Ethernet standard will be used as the basis for the physical layer and the link layer. This also meets the present trend of all modern real-time networks as listed in section 1.2 to be based on Ethernet. The service enhancements of White Rabbit to the Ethernet layers, like the deterministic, low latency packet delivery as well as accurate delay compensated timing distribution, will form a new basis for already existing protocols, thus enabling these technologies to operate with unprecedented performance also in the area of large-scale control systems.

Vision of the project. The driving objective of the project is to establish a set of standard compatible extensions to Ethernet that allow the guaranteed execution of operations in a network node in a highly coordinated way with a high number of other nodes in a large-scale system.

The implementation of an appropriate OSI reference model layer 2 protocol should not imply assumptions on the upper layers related to fulfilling the target objective of determinism and
Figure 1: Typical structure of an industrial real-time network

timing precision. This allows the usage of existing higher layer protocols over the infrastructure while providing zero-configuration event-triggered delivery of special packets. This key technology for the next generation of distributed real-time monitoring and control systems will also integrate the legacy traffic of existing installations. The aim is to avoid the impact of general (unprioritised) traffic on the real-time constraints while dynamically allowing for usage of the maximum bandwidth.

The White Rabbit user will be able to build applications on a reliable real-time communication link and benefit from precise timing in the sub-nanosecond range. There will be no need for complicated configuration which also allows for dynamic network structures. The handling of packets in White Rabbit through individual switching allows real-time guarantees with upper boundaries and pro-active adaptation to changes in the network or when fault conditions start to occur. Furthermore, the dynamic bandwidth adaptation for real-time constrained packets enables Quality-of-Service (QoS) without re-configuration of the network structure.

The success of industrial communication systems heavily depends on the fact that long-term guarantees on the availability of a certain technology can be made. The project aims for implementability of the results for at least some decades. To achieve such a long-term availability the base for the project itself will be drawn from existing Ethernet and timing standards, e. g., IEEE 802.3, IEEE 1588, and Synchronous Ethernet. Building upon the wide spread and internationally standardised technologies the project will supplement them in order to achieve the mentioned performance parameters while keeping the interoperability with legacy nodes.

In general an industrial control network consists of several different devices with various demands regarding real-time, throughput and determinism. Figure 1 shows a typical industrial real-time network with mixed devices organised so that the backbone can be efficiently used in a central way for all applications. This approach avoids the installation of multiple networks for the different purposes in parallel.

As shown in the typical structure, some devices like those used for status monitoring or network management do not require real-time properties of the network. On the other hand, some devices that are dedicated to data acquisition normally tag the data with an accurate timestamp in order to provide a consistent picture of the overall system at a specific moment. Furthermore, some actuators are required to react instantly to decisions taken by a controller, as for example in the case of emergency shutdowns. This asks for a low-latency delivery of control information. The planned event-triggered approach of White Rabbit is able to supply all types of traffic flows with the required properties while not restricting the other communication parameters. A sensor can be supplied with accurate timing while the remaining network is not required to work in a time-slotted communication paradigm. Also time-constrained messages can be delivered without imposing planning effort or restrictions on the overall legacy traffic.
The White Rabbit project will result in:

- a network platform that provides new services to existing higher-level protocols.
- a highly scalable and zero-configuration network.
- allowing unification of until now separate networks.
- the enabling of event-triggered monitoring.
- re-usable products that are compatible with existing platforms.
- superior next generation supervisory control and data acquisition (SCADA) systems.

**Targeted outcome and relevance to the call.** The proposal aims at the objective ICT-2009.3.5 “Engineering of Networked Monitoring and Control Systems”. Particularly addressed are the targeted outcomes of section c: “Control of large-scale systems”.

Currently many industrial users experience the benefit of industrial Ethernet solutions due to the ease of integration with the office level and its wide availability. Nevertheless, all of these solutions lack certain capabilities in different areas. Most of the existing standards have drawbacks related to a high configuration effort, lack the scalability to a high number of nodes or lack accuracy for high-performance real-time systems.

The presented project addresses the issues for large-scale deployments and will show that currently competing properties of a physically wide distributed system can be combined using a clever combination of technologies and original research. Figure 2 illustrates the project goals concerning the different desired properties of a large-scale control system. While standard Ethernet can be deployed without configuration effort to a high number of nodes, it lacks all requirements for control and monitoring systems like determinism, fixed and short response times, or accurate synchronization of the nodes. The industrial Ethernet implementations each address specifically a certain drawback of the standard solution and try to limit the disadvantages for other properties. Still, current implementations require a high configuration effort in order to allow for determinism and real-time packet delivery within the network. In particular, the
network has to be planned and cannot be dynamically adapted to the application needs.

The event driven approach (i.e. immediate start of packet transmission when data is available) of the proposed system allows to send real-time information at the time it is occurring, while still guaranteeing an upper bound for the packet delivery time. This, together with the highly accurate synchronization of the end nodes, will provide a significant performance boost to the network throughput as well as to the real-time parameters. The minimal configuration effort also allows to add and remove nodes dynamically, which gives improvements regarding the scalability while keeping QoS constraints.

Due to the fact that the system combines the advantages of packet-oriented networks (such as fault tolerant switching and dynamic bandwidth allocation) with the predictive behaviour of circuit-switched networks, it can be used to implement pro-active behaviour as found in cell-switched networks. These features can be implemented on protocol layer 2, thus giving improvements to existing Supervisory Control and Data Acquisition (SCADA) systems and Distributed Control Systems (DCS) solutions without adaptation needs. The usage of existing real-time protocols on top of the proposed architecture will allow the system to also handle possible conflicts of high-priority messages on a single network link.

The main focus of the project is monitoring and control of a large-scale system in the range of tens of kilometres. To deploy such systems, the topology of the network has to consider the geographical possibilities much more than for small-scale systems. Moreover, also today’s SCADA and DCS networks have to be extended to support control of those large systems. The research on this topic addressed in White Rabbit is in line with the scope of the call.

Finally, as encouraged in the call, the specifications that will result from the project will be used as input to standardisation efforts. Although the latter are not directly covered by the project, the plan includes an explicit task about dissemination and exploitation. It is driven by main industrial players in the area of automation systems to draw the attention of a large community to the efforts in the project. White Rabbit is targeted at industrial environments such as backbones for industrial wireless systems, accelerators and many other industrial applications. Already during the preparation of the proposal the involvement of large international parties, like CERN, GSI, National Instruments, and Hirschmann attracted significant attention of other users of real-time systems with special needs regarding system dimensions and performance.

**Architectural features.** As a wide area control and monitoring network, White Rabbit aims for re-use of existing investments. Therefore it allows to integrate existing network infrastructures based on Ethernet. The proposed architecture has the capability of transparently transporting legacy traffic although there might be some performance degradation in favour of the real-time traffic. Through traffic classification and a tree topology it will even be possible to configure real-time features for certain legacy nodes without the need for any modifications.

Quality-of-Service (QoS) will be implemented by prioritisation of messages. Besides existing implementations with different queues and queuing schemes, White Rabbit will implement a special packet type for time critical messages. Transmission interruption of standard traffic will allow for an upper bound of the delivery time for this type of messages. The upper bound can be determined in advance by an automatic investigation of the network hierarchy. As an example nodes can be controlled with timely deterministic high-priority messages sent by a managing node, while each node is able to use standard traffic to report back measurement data.

The event driven approach for high-priority control messages allows for a great reduction in the configuration and maintenance effort. The network architecture and protocol does not require a pre-planning in order to fulfil real-time constraints. Furthermore, the architecture is made in such a way that adding nodes does not degrade the performance of the network and therefore can be done in a plug-and-play manner. Basically all required information can be provided by the network through an auto-discovery mechanism that allows to run a zero-configuration strategy as far as the user is concerned.
Event-triggered architecture. Currently existing real-time protocols in the area of industrial Ethernet are time-triggered systems based on a Time Division Multiple Access (TDMA) channel access strategy. The downside of TDMA is that it transmits signals at specific time intervals whether or not there is a node that needs to transmit over the network. This makes TDMA inefficient compared to event-triggered approaches, wasting bandwidth capacity on unnecessary or unused transmission slots. While the event-triggered approach can deliver the information always within a certain delay, data in the time-triggered approach additionally has to wait for the assigned transmission time (communication slot). This fact is illustrated in figure 3 showing the temporal behaviour of both approaches for the same sequence of events. The advantage of the TDMA approach is that the extensive pre-planning of communication allows offline analysis to check whether deadlines are obeyed. Further, fault tolerance analysis and implementation is eased because of the fixed communication schedule. The latter on the other hand makes TDMA inefficient. To overcome such pre-planning issues, a reservation system has to be implemented in which time slots can be assigned in a more dynamic way giving nodes the possibility to reserve a slot only when it is needed for transmission.

The above mentioned approaches to make TDMA more flexible lead to the idea of avoiding the overhead completely. Consequently, the event-triggered architecture of White Rabbit is expected to enable smarter resource exploitation as well as a faster delivery time. Thorough response time analysis can generate similar statements about the real-time performance for this type of systems as static schedules can for time-triggered systems. Both methods are suitable to ensure deadlines also in peak load scenarios and require detailed knowledge about the timing constraints of the controlled real-time object. Hence, neither time-triggered systems nor event-triggered systems are to be preferred with respect to analysability.

The already mentioned higher efficiency regarding bandwidth utilisation as well as the fact that the communication planning is not needed (allowing for more flexibility), strongly argue for an event-triggered approach in White Rabbit. Based on this method the system can also provide a low configuration effort easing extensibility which is important for a large-scale and dynamic control system.

Pro-activeness. The packet-oriented and event-triggered architecture of White Rabbit allows easy and dynamic reconfiguration of the system. Due to the fact that the real-time behaviour of the system is not dependent on a special pre-configuration, the network architecture can quickly react on faults in network links. The aimed features of the physical layer will allow for accurate timing by an embedded clock frequency distribution. Therefore, the network elements permanently maintain and monitor a connection even when no data is transferred. The physical properties of a link can consequently be continuously monitored and alternative routing can be chosen based on the measured quality parameters.

The low configuration effort and the ability to monitor the network links including the current status of the network structure allows for dynamic addition and removal of nodes without
affecting the existing communication. The distribution of absolute time gives all nodes the
ability to perform real-time operations without dependency on other network elements. This
distributed approach removes single points of failure which commonly come from a dedicated
single element organising the traffic to reach real-time performance. While not being the main
focus of the project, the event-driven approach allows for a simple dynamic connection and
participation in a real-time network while other techniques always demand the knowledge of
some configuration or need to reconfigure.

Finally, one of the major novel approaches which are proposed in the project is to support
pro-activeness by the integration of test and measurement capabilities into the network itself.
For example, it is possible to use the exact time information available at the MAC layer of
White Rabbit in order to debug large-scale networks with, in terms of occurrence time, precise
monitoring capabilities. Also the early detection of increased error rates allows the network to
auto-reconfigure and to provide predictive warnings.

Optimised operation of large-scale systems. In order to enable optimal operation of large-
scale control systems the projected architecture will supply the network nodes with a precise
time. This allows synchronized measurements of events as well as the execution of coordinated
commands with an accuracy in the sub-nanosecond range. The operating network will allow
to spread timing information fully automatically over the entire span of the system which is
targeted to have links up to 10 km long.

Besides the wide spatial distribution of the project vision, it is also planned to support a large
number of nodes in the range of two thousand. The challenging issue is to constantly supply
all end-nodes with a high-precision absolute time. On one hand this requires the network to be
capable of running bidirectional communication in order to automatically calibrate propagation
delays on the transmission media. This self-activated feature is not common to state-of-the-
art timing infrastructures. In addition it also has to support the compensation of asymmetric
transmission delays. This is especially important since the demand for high accuracy requires a
much better mechanism than the common round-trip delay measurements.

Out-of-band methods such as carrier clock phase measurements and on-board delay auto-
calibration can be used to guarantee zero-traffic sub-nanosecond synchronization.

The proposed approach will in general improve TDMA based systems by a combination of
event-triggered time-constrained messages plus accurate timestamping of events and execution
of commands in the nodes. This is the high-performance basis for large-scale systems where
a majority of the nodes do not require the delivery of messages in real-time but need just
an accurate timebase for performing local operations. Furthermore, this approach improves
on existing real-time technologies as the layer 1 and layer 2-based communication services of
White Rabbit also provide a more exact timing interface than available today. Consequently,
existing protocols can benefit from it rather than synchronizing the clocks with the conventional
protocol-based schemes. This architectural interface allows a very flexible and transparent
use of the system.

The timing and especially the outstanding precision of White Rabbit are important operatio-
nal aspects of monitoring and control systems, allowing for completely new process automa-
tion algorithms. The White Rabbit project will therefore be an enabling technology for
new applications requiring high accuracy, like localisation of wireless nodes using the time-
difference-of-arrival method. Other use-cases include structural monitoring of large buildings,
monitoring meteorological events and particle accelerators.

These new architectural features and their integration into existing real-time communication
technologies are indicated in figure 4. As described in the next section the system concept
can easily be integrated into state-of-the-art industrial communication technologies that will
therefore be significantly improved.
Figure 4: Proposed architecture and its integration into existing real-time communication technologies. White Rabbit provides accurate time and improves message delivery at the MAC and Switch layers (dotted lines).

1.2 Progress beyond the state of the art

The state of the art of today’s real-time networks can be best seen by looking at fieldbus developments. These typical real-time networks converged from serial, specifically tailored physical layers to Ethernet based protocol suites. The reason for this trend, which was mainly pushed by the factory and process automation, is the fact that physical layer devices from the consumer electronics mass-market are cheap. This well-standardised and widely distributed technology has the additional advantage that the physical layer is compatible with the IT infrastructure from the office level of an enterprise network. Furthermore the components are offered by many producers, which guarantees long term availability. Therefore, for a network infrastructure such as proposed in this document the basic functionalities of real-time Ethernet fieldbuses have to be analysed and significantly extended. This section discusses the main objectives of the proposed project beyond the currently available technologies.

Real-time Ethernet categories. In principle, three different basic types of real-time Ethernet protocols are currently used:

1. **Unmodified protocol** stacks are used by real-time networks that control processes with low requirements. Several applications exist where the application layer directly uses the standard Ethernet/IP/UDP stack. Due to the lack of real-time support of these stacks, cyclic update times that can be reached are in the range of 100 ms. Typical representatives of this group of networks are MODBUS/TCP [3] and Ethernet/IP [4].

2. **Prioritising protocol** stacks try to overcome the deficiency of the first approach by assigning higher priorities to real-time messages. With this, it is at least ensured that non-real-time traffic, such as configuration data or low priority messages, do not interfere with the real-time communication. Typical representatives of this approach, like PROFINET IO Conformance Class C [5], can use Quality-of-Service extensions of standard Ethernet such as IEEE 802.1q. Such protocols may achieve cycle times which are in the range of 1 ms.
3. **Scheduling protocols** intervene directly at the Media Access Control (MAC) layer in order to ensure time-slotted access to the switched medium. This kind of arbitration obviously gives the best performance in terms of cycle time, which can be seen in some commercial products, such as PROFINET IRT [5], Ethernet POWERLINK [4] or EtherCAT [6]. Commonly reached accuracy, measured in terms of communication jitter, can be better than one µs.

White Rabbit progresses beyond the state of the art by modifying the MAC to work preemptively like modern operating systems. As long as there are no high-priority messages, the message flow is like for normal Ethernet. The occurrence of an important, high-priority message in a separate queue of the MAC causes a “task switch” that will interrupt the standard communication and will send the high-priority packet with a much lower latency than possible with existing systems.

The decision on which packets are classified as important low-latency packets can be based on manual sorting, QoS measures, e.g. IEEE 802.1q, or on the Ethernet type field. In addition, the system provides a highly accurate time to all nodes independently of the traffic, which allows to separate the need for coordinated actions (e.g., command execution or acquiring a measurement) from packet delivery with time constraints. Existing protocols can be integrated with White Rabbit to take advantage of the features it offers.

Unmodified protocol stacks can be integrated in White Rabbit without any changes to the actual protocol stack. This concept, shown in figure 5, uses the standard compliant behaviour of White Rabbit. Due to the usage of standardised communication paths, the performance of the protocol will obviously stay untouched. If there is a unique way to still identify real-time data, the MAC could be adapted to enhance this communication by sorting it transparently to the high-priority queue. Also the scheduling protocols can be integrated, as illustrated in figure 6. In this case, the already existing separation between best effort and real-time traffic can be used by the White Rabbit MAC to prioritise the latter.

One of the most important goals of White Rabbit is bringing real-time to large-scale systems. So far, a time scheduled network suggests the best results in terms of real-time capability. Nevertheless, scalability has to be considered and points out some major problems.
This technology, as used in PROFINET IO Conformance Class C or TTEthernet, needs a modified MAC in order to support the timely scheduled arbitration of the media access. This is indicated by the overlap between the White Rabbit MAC and the scheduler. Left: original implementation; right: integrated with White Rabbit.

This rather complex collection of traffic flows with different requirements suggests a **priority and a traffic shaped approach** more than a time-slotted approach. This technique, as chosen for White Rabbit, allows to cope with the different demands of the various concurrent traffic flows that state of the art cannot handle.

For distributed measurements as the aforementioned example, i) a high amount of time-stamped, but not timely delivered measurements can be used instead of real-time with delivery guarantees\(^1\). In addition, ii) for critical messages low-latency delivery is required which has to be prioritised over the high volume of iii) non-real-time (legacy) traffic. White Rabbit allows the mix of all these traffic types.

The distributed control character of a complex system is currently not covered by the state of the art. The common approaches are founded on the use of IEEE 802.1q, which prioritises

---
\(^1\)In many cases the precise time tagging provided allows the application to remove the real-time requirements.
Figure 7: Integration of real-time prioritising protocol technologies. This technology is used in some flavours of PROFINET IO Conformance Class A and B that need support for higher prioritised messages.

Left: original implementation; right: integrated with White Rabbit.

messages on different packet queues in the MAC layer. This prioritisation is done without packet preemption and therefore the worst case of a high priority packet delivery is in a rough approximation defined by the Maximum Transmission Unit (MTU) and the link speed of the physical layer. The MTU, however, which is nowadays typically 1500 Bytes, has to be multiplied with the number of switching network units the packet has to travel through. This increases the maximum delay until a high priority message can be delivered to the target MAC to $n \cdot (MTU + IFG + \Delta_{SW})$, where $n$ is maximum depth of the hierarchy, IFG the inter-frame gap (96 bits), $\Delta_{SW}$ the switching delay, and $C$ the communication bandwidth. In the case of the proposed preemption based prioritisation, the maximum delay is dramatically reduced as the packets can be interrupted, e.g. 2µs per switch in the suggested system. This enhancement will not solve the problem of quality of service aware networks in general, but will provide the first approach for a system in a scale this large.

Figure 7 shows the advantage that can be drawn out of such a stack in connection with the proposed architecture: the existing real-time communication architecture does not need to be modified and can take seamlessly advantage of the prioritisation. The preemptive nature of the approach will significantly improve the performance of the considered protocols. An overview of the typical performance parameters of the protocols discussed in this section can be seen in table 1. Most of the protocols are standardised in IEC61784-2 [7] (and in the related IEC61158), from which the values are taken.

Real-time communication and timing performance. One of the first comparison criteria of a protocol suited for the control of a system is the real-time communication performance. Typically one defines a cycle time as the time it takes for a process variable to be updated, i.e. transmitted from the sensor to the control instance or from the latter to an actuator. The second important parameter is the communication jitter, that defines the precision in time with which a node will react. Typically this is the precision of the moment of sampling of a value or of the moment of updating of the state of an actuator. The cycle time involves the transmission mechanism of information, while the communication jitter is subject to clock synchronization mechanisms.

For the protocols listed in table 1, the current available technology can be summarised as having a cycle time in the 200 – 500µs range. This value is dependent on the packet size, the allocated bandwidth and, most importantly, the number of nodes. Most protocols state the
Table 1: Ethernet-based real-time protocols. Typical performance figures.

<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Ethernet/IP</td>
<td>IEEE 802.3</td>
<td>Frame prior.</td>
<td>Soft</td>
<td>P/C</td>
<td>Line, ring, star</td>
<td>Yes</td>
<td>100 Mbps</td>
<td>1024</td>
<td>&lt; 20.4 ms</td>
</tr>
<tr>
<td>- time sync</td>
<td>IEEE 802.3</td>
<td>Clock sync</td>
<td>Hard</td>
<td>P/C</td>
<td>Star</td>
<td>Nodes only</td>
<td>100 Mbps</td>
<td>90</td>
<td>&lt; 190 µs</td>
</tr>
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<td>PROFINET IO Class A,</td>
<td>IEEE 802.3b</td>
<td>Frame prior.</td>
<td>Soft</td>
<td>P/C</td>
<td>Line, ring, star</td>
<td>Yes</td>
<td>100 Mbps</td>
<td>60</td>
<td>≤ 128 ms</td>
</tr>
<tr>
<td></td>
<td>IEEE 802.11</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>IEEE 802.15.1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Class C</td>
<td></td>
<td>Time scheduling</td>
<td>Hard</td>
<td></td>
<td></td>
<td>No</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ethernet</td>
<td></td>
<td>Time-slicing</td>
<td>Hard</td>
<td>M/S</td>
<td>Line, star</td>
<td>Yes</td>
<td>1 Gbps</td>
<td>20</td>
<td>1100 µs</td>
</tr>
<tr>
<td>POWERLINK</td>
<td></td>
<td>polling</td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MODBUS[7] TCP, RTPS</td>
<td>IEEE 802.3</td>
<td>Clock sync</td>
<td>Soft</td>
<td>M/S&lt;sup&gt;TCP&lt;/sup&gt; P/C&lt;sup&gt;RTPS&lt;/sup&gt;</td>
<td>Line, ring</td>
<td>Yes</td>
<td>n/a</td>
<td>Topology dependent</td>
<td>Topology dependent</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Event-based&lt;sup&gt;c&lt;/sup&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TTEthernet[7]</td>
<td>IEEE 802.3</td>
<td>Time scheduling</td>
<td>Hard</td>
<td>M/S</td>
<td>Line, tree</td>
<td>Yes (low performance)</td>
<td>1 Gbps</td>
<td>Virtually unlimited</td>
<td>n/a</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Frame prior.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SERCOS III</td>
<td>IEEE 802.3</td>
<td>Time scheduling</td>
<td>Hard</td>
<td>M/S</td>
<td>Line, ring</td>
<td>No</td>
<td>100 Mbps</td>
<td>≤ 251</td>
<td>&lt; 1 ms</td>
</tr>
<tr>
<td>White Rabbit</td>
<td>IEEE 802.3</td>
<td>Event-based</td>
<td>Hard</td>
<td>n/a</td>
<td>Tree</td>
<td>No</td>
<td>1 Gbps</td>
<td>&gt; 2000</td>
<td>&lt; 15 µs</td>
</tr>
</tbody>
</table>

<sup>a</sup>P/C: Producer/Consumer, M/S: Master/Slave
<sup>b</sup>Conformance class A uses all, conformance classes B and C use only IEEE 802.3
<sup>c</sup>TCP uses both, RTPS only event-based
number for the best case, i.e. a low number of nodes and not for the full span. As an example, with the SERCOS III protocol [3], with packets of just 8 – 12 bytes, cycle times down to 31\(\mu\)s can be measured when only 7 slaves are used. However, this cycle time goes up to 500\(\mu\)s when 122 slaves are used or even to 1 ms for 251 slaves. As White Rabbit is an OSI layer 2 protocol, as such it does not define a cycle time. However, with the preemptive nature of its high-priority packet transmission, the end-to-end delivery time is much lower than any other layer 2 protocol. This, combined with the presence of a precise time at each node, allows the implementation of cycle times that may be as short as the end-to-end delivery time (e.g., 15\(\mu\)s with a one km cable and three switches).

Besides cycle time, the communication jitter is important. In time-slotted systems it is defined by the slot time jitter and thus by the jitter of the clock synchronization. Using the state-of-the-art clock synchronization approaches like IEEE 1588 (e.g., as utilised by PROFINET IO), a best case jitter is in the range of typically 100 ns. Again, in special configurations some protocols reach up to 35 ns when having only one dedicated master. Research results show that the quality in such a timing hierarchy deteriorates with the number of cascaded clocks, which are in a first approach necessary to propagate timing through a switch [8]. Similar effects also occur with the cascading of Phase Locked Loops (PLLs) when used for clock recovery in communication systems. Nevertheless, these issues are already tackled in several applications like in power delivery [9] or Synchronous Ethernet and the telecommunications industry [10]. All of these systems claim communication jitter to be less than 1\(\mu\)s, with some of them claiming even lower under certain conditions [11]. For EtherCAT, however, maximum jitter depends on many boundary conditions (e.g., number of nodes, network length and temperature change), so its value is given as much smaller than 1\(\mu\)s. TTEthernet’s specification also claims less than 100 ns, but in practice its accuracy is shown to be in a range of 1 – 10\(\mu\)s [12], which is achieved only with non-standard hardware. White Rabbit targets much better performance parameters.

The goal set for White Rabbit is below 1 ns for the jitter, to meet the requirements of timestamped data collection. Using the Ethernet 1000 BASE-LX physical layer standard data rates of 1 Gbps over a distance of 5–10 km are possible [13]. Additionally, White Rabbit will improve the cycle time enabling update times of process relevant values in less than 15\(\mu\)s.

As shown in the pictures above, if a real-time protocol is integrated into the White Rabbit infrastructure, it can be improved and can take advantage of the timing services. The goal of the proposed project is, however, not to provide a timing system on its own, but to facilitate the use of the infrastructure as such. It aims at establishing a novel communication network, which is suited to be used for transfer of non-critical and real-time data as well as a timing infrastructure. Nevertheless, as the White Rabbit system can be also used without preemption of packets, it is also useable for the aforementioned real-time protocols. These protocols can benefit from the time service of White Rabbit by using the clock synchronization service rather than their own (less accurate) timing strategies.

The idea behind the timing concept is that the communication infrastructure itself provides the means for the clock synchronization which is illustrated in figure [8]. This is one of the major achievements beyond the state of the art as currently all clock synchronization schemes are dislocated among several layers in the communication stack.

For example in typical IEEE 1588 nodes, a hardware based “timestamper” takes messages near the physical layer. This data is combined with a message identification tag from the MAC layer and then processed with the protocol data at the application layer. Finally, a clock is
adjusted, which is typically done in hardware for accuracy. This spreading among several layers will be overcome by White Rabbit by concentrating it to the physical layer, which then provides a synchronized clock as a service for the applications and also for protocols residing in higher OSI protocol layers.

**Topology.** Another area to look for considerable differences between real-time Ethernet implementations is the flexibility to adapt to different topologies. In small-scale systems the topology is not critical as the wiring can easily be adapted, but for large-scale systems the allowed topology becomes more relevant. Various technologies can support different topologies: a star or a complex tree topology can be implemented by either using real-time Ethernet devices with more than two ports or by using standard Ethernet switches (at the expense of some more jitter) [5].

For instance, this is true for PROFINET IO, EtherCAT, and POWERLINK, that allow the usage of line, tree, star, and drop-line topologies. With PROFINET IRT, however, the maximum number of nodes is limited, and performance is strongly influenced by the topology used [3]. POWERLINK has limitations caused by hub delay accumulation and allows up to 240 networked real-time devices in one network segment [14]. Many other commercial products have similar properties.

Since White Rabbit is driven by enhanced switching devices, the topologies used can be the same as for switched Ethernet. This means that in general a tree topology is used and that alternative structures can be implemented through the usage of RSTP (Rapid Spanning Tree Protocol). This progress beyond the currently available technologies is important as complex systems with large spatial distribution can not adapt to the possible network topologies due to geographical and (building-) infrastructural circumstances. So by using enhanced switches White Rabbit provides the flexibility of complex topologies as required by large-scale installations.

**Unification of separate networks.** Currently, high-precision physically large distributed systems such as particle accelerators often require the control network to be built up out of two separate networks. One is used for real-time control data and timing, while the other one is used for transferring diagnostics and large configuration data. The reason for this is the fact that no real-time network is able to provide high-precision to large-scale installations nor are timing networks able to provide the required bandwidth when compared with today’s data networks. For example, WorldFIP which is suited for timing defines 2.5 Mb/s for copper wire physical layer over a distance of 500 m–1.5 km [15].

White Rabbit allows to unify the real-time and data networks, combining them on a single network. On first order this will reduce the installation and maintenance effort by half, as will be the power consumption of the network.
Configuration flexibility. One of the major challenges for protocols with defined end-to-end timing features is flexibility. Traditional real-time protocols assume a work flow where a network is configured with a fixed topology and node structure. For example, the origin of a sensor value in an automation system will neither change the MAC address nor the position within the topology. This configuration is usually done in the engineering phase, where communication relationships are defined and an overall resource planning is done. During runtime such networks accept no changes in the resource requirements.

The complex planning of a system is the crucial issue of PROFINET IO CC-C when link reservation is activated. For each node all communication relationships have to be known in advance and scheduled and there are strong interdependencies among the schedules. Therefore, system planning is a complex, recursive optimisation problem, without a straightforward solution. Even with fairly simple topologies a small change in configuration, such as adding just a single node, requires the re-scheduling of all traffic and may result in significant changes in network performance. As another example, Ethernet/IP needs a router with multicast/broadcast control, but in order to have an optimised network, it is recommended to utilise an infrastructure which possesses specific features, such as IGMP (Internet Group Management Protocol) snooping, aiming to minimise end-device and switch loading with unwanted traffic. This requires a complex, non-standard configuration, but once installed correctly, requires little maintenance [16]. Finally, in EtherCAT the configuration is simplified only if the process data of all nodes combined fits inside a single Ethernet packet.

As shown in other projects [17], this paradigm will likely be broken. The problem is that if one includes mobile nodes with real-time demands on the factory floor, it is not possible to predict the position in the network in advance, as they might roam around different access points. Investigations show that – due to efficiency considerations – it is not reasonable beyond a certain network size to arbitrate these nodes in a timely equal schedule. The result of this demand of the factory of tomorrow is that also the wired networks need to adapt to dynamic re-configuration seamlessly and in real-time. Some investigations [18] attempt to overcome this problem with QoS-aware Ethernet. This, on the other hand, reduces the applicable real-time protocols and time guarantees to a subset of the state of the art.

The White Rabbit project will tackle these problems and widen the state of the art on the basis of preemption support to enhance the control of complex systems. This additional degree of freedom in terms of data exchange allows to run such networks without a predefined topology or schedule. In addition, this will not restrict to time-scheduled protocols such as POWERLINK as those approaches can still be operating on top of the White Rabbit infrastructure. Of course, for a guaranteed real-time behaviour of such a system an arbitrary degree of freedom cannot be given, as even with the prioritising preemption approach the network can only be loaded up to its communication bandwidth until the loss of latency guarantees for high-priority messages. Therefore, a system wide planning has to be done just for peak load cases during engineering. This planning only has to cover the required resources rather than their consumption in the per-se undefined network topology and can be easily achieved using traffic shaping or reporting the gathered delay to decide on the usability of the information.

Communication models. Traditional approaches to control large-scale systems define communication relationships. These relationships are an important part of the overall communication model. For example a trend from the strictly master-slave based approach to multi-master use-cases can be observed. All systems support slave-to-slave communication. Topology-dependent slaves within EtherCAT can insert data “upstream” which can be read “downstream” by all other nodes. In applications in which relations are known at the network planning stage, they can be handled accordingly. When this is not possible, there is also a topology-independent slave-to-slave communication method, which requires two cycles (the data is relayed by the master). Therefore, performance is typically similar to that offered by PROFINET IO CC-C.
and SERCOS III, which also has topology independent slave-to-slave communication within the same cycle, gained by the dual processing in slave devices [19]. Using the consumer/producer model, POWERLINK and Ethernet/IP are gaining very efficient slave-to-slave communication over broadcast, but are not escaping the drawbacks of this approach.

Since from a communication point of view, White Rabbit does not have a master device, it also allows direct node-to-node communication. The data exchange is done via the switches between the involved nodes. Consequently, also multiple concurrent communication links can be handled without affecting each other which is a major improvement of the proposed architecture to state-of-the-art networks.

Still, traffic shaping or the utilisation of a higher layer protocol has to ensure that no congestion can occur on real-time traffic in order to respect deadlines in peak-load cases. It is assumed that node-to-node communication has, in most use-cases, no real-time constraints or timestamping the information is considered to be sufficient. Therefore it does not require planning at all.

Fault-tolerance. Due to the fact that the nodes and the communication infrastructure of a large system are subject to an increased probability of failures, the matter of fault tolerance has to be addressed specifically. Also, in applications where safety is critical, the use of fault-tolerant systems is obligatory, since a single fault might lead to catastrophic consequences, like injuries or loss of human lives and damage to the environment.

Several methods to achieve high-availability of industrial communication networks (e.g., redundant cabling) have been standardised in IEC62439 [20]. The real-time protocols described in the previous sections often use such methods. This can be achieved with Ethernet/IP, PROFINET IO CC-A and CC-B, by using switches with a Spanning Tree Protocol. An option to POWERLINK enables an implementation of ring, partial ring, cable, and node redundancy. PROFINET IO CC-C offers redundancy based on a ring topology, but the planning algorithm for the redundant topology is so complex that it is of questionable practical value [3]. Both SERCOS III and EtherCAT support cabling redundancy by means of a ring connection. TTEthernet networks can be set up with multiple redundant end systems, switches, and segments so the system remains fully functional even if a failure occurs (supporting a single or double fault hypothesis). The behaviour of TTEthernet is precisely predictable and thus formally verifiable [21].

White Rabbit could be used as a base on which the high-availability protocols as defined in IEC62439 can be applied. Also, the timing properties of White Rabbit could help in quickly discovering of faults and the precise timestamps could be used as selection criteria for solutions based on a ring topology. In addition, the proposed system offers a high reliability with the Forward Error Correction (FEC) mechanism (e.g., Luby Transform (LT) encoding) implemented at OSI layer 3, but also segmented frames for high-priority and link redundancy supplied by Ethernet (e.g., STP and RSTP). White Rabbit will transfer important messages in several smaller parts with redundant information in order to guarantee a correct delivery even when some parts are lost or have errors. This system will not need any retransmission of data that could otherwise break the real-time behaviour. Additionally, all redundancy and fault tolerance measures for Ethernet like link redundancy can transparently be applied.

Fault-tolerance imposes very strict real-time prerequisites: these systems must react to events in the environment within precise time constraints and these requirements call for advanced synchronization techniques. As the system can be either time-triggered or event-triggered, a corresponding timing analysis, which checks the timing requirements, is required. When using a time-triggered model, the schedule is determined at design time. For event-triggered systems the proposed system shows its strength since it can inherently cope with high-priority messages by guaranteeing a maximum latency independent of the network structure.
Table 2: Summary of performance indicators for White Rabbit

<table>
<thead>
<tr>
<th>Performance Indicator</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Communication Jitter</td>
<td>&lt; 1 ns</td>
<td>Standard deviation of the communication jitter compared to perfect (GPS disciplined clock) of repetitively sent real-time packets.</td>
</tr>
<tr>
<td>Clock Jitter</td>
<td>250 ps</td>
<td>Standard-deviation of the output of the synchronized clock, which can be used for upper layer protocols or applications.</td>
</tr>
<tr>
<td>Delivery Time</td>
<td>&lt; 15 µs</td>
<td>End-to-end delay of a real-time message (1 km cable, 3 switches).</td>
</tr>
<tr>
<td>System Size</td>
<td>10 km</td>
<td>Maximum distance between two arbitrary nodes.</td>
</tr>
<tr>
<td>Number of nodes</td>
<td>&gt; 2000</td>
<td>Number of nodes attached to the White Rabbit infrastructure, all being able to issue real-time messages.</td>
</tr>
</tbody>
</table>

Performance comparison of the state of the art and aimed features. It is in many cases difficult to compare protocols against each other as many performance indicators are significantly dependent on the actual configuration. For example, in a lot of use-cases the number of nodes and the deployed topology directly influences the cycle time in real-time Ethernet. However, a rough comparison is given in table 1.

In this table the bottom row shows the intended performance of the White Rabbit infrastructure. The performance shown is for a full scale cascaded tree network of 2000 nodes with several links of 10 km long.

One can see that the combination of features that White Rabbit offers (number of end stations, cycle time and jitter) are much better suited to large-scale systems than each of the currently available technologies solutions can provide. In fact in many cases White Rabbit improves at least one of the parameters by a factor of 10 to 100 or even a factor of 1000 compared to those of individual solutions. With the parameters of White Rabbit (as summarised in table 2) one can build innovative applications that go well beyond of what is possible with state-of-the-art technologies.

Related research. The time-triggered architecture is the subject of several ongoing investigations. This architecture can be effectively deployed in safety-critical transportation systems (automotive, aerospace, railway), and as its key advantages offers composability\(^2\) and a transparent implementation of fault-tolerance.

The EU-funded projects TTA, SETTA, and NextTTA are intended to enhance the structure, functionality and dependability of TTA to meet the austere cost structure of the automotive industry, while satisfying the rigorous safety requirements of the aerospace industry and to push the time-triggered architecture into future vehicles, aircraft, and train systems. With the good sides regarding fault-tolerance of these systems, there are also drawbacks in some other aspects that should not be disregarded. The strict time-triggered architecture significantly increases (re-)configuration effort and decreases scalability. In a non-flexible situation a node has to send its messages at times defined at system start. If the messages do not arrive in time, an error is signalled and recovery can start immediately. In a flexible situation, when a node can send messages at will, the other nodes do not know if a message is sent too late or not at all as they do not have the information that a message should have been sent. The immediate error detection mechanism cannot be used in this case. It is easy to see that flexibility and safety criteria cannot easily be met at the same time. The time-triggered protocol defined in the TTA project does not accept any flexible communication on the network and only allows pre-defined

\(^2\) composability is the ability of different components to work together without endangering the system safety in either the temporal or value domain.
time slots [22]. It should be noted that the mentioned projects put a strong accent to application domains related to transportation systems, while White Rabbit targets large-scale control and monitoring systems, while staying highly scalable.

In the FP7-funded GENESYS project the objective was to develop a cross-domain reference architecture for embedded systems that meet the requirements and constraints documented in the ARTEMIS SRA: composability, networking and security, robustness, diagnosis and maintenance, integrated resource management, evolvability, and self-organisation [23]. The reference architecture supposes to be domain-independent and serves as a template that can be instantiated to concrete platforms for individual application domains (e.g., automotive, avionic, industrial control, mobile, consumer electronics). In the context of White Rabbit the connection to GENESYS has to be seen as the communication interface of the robust embedded system. White Rabbit will enhance the possibilities researched in this project by providing a robust large-scale communication platform for complex systems.

The work presented in [24] investigates approaches to reach stabilisation of large-scale linear time-varying systems. This work basically proposes an algorithm with robust adaptive controllers in order to cope with the drawbacks of the unknown system-wide timebase in the large-scale distributed system. Thanks to its provision of a common notion of time, White Rabbit can be the solution to this type of problems.

The work of [25] describes a distributed network analysis tool and is focused on the problem of logging precisely timestamped data in a real-time Ethernet system. The authors propose a structure which is able to collect messages by observing them on the line. This concept can be broadened with White Rabbit to the scope of a large-scale system again with the use of the common timebase and the foreseen concept of the integrated monitoring capability.

An interesting research on the general issue of real-time in large distributed systems [26] shows that during the design of a higher level protocol many influences from the lower layer protocol have to be considered. The paper considers the abstraction of the communication means as a generalised interface on top of which the real-time control is set up. This interface can be enhanced with the concept of the distributed timebase and real-time communication of White Rabbit and thus significantly simplified.
1.3 S/T methodology and associated work plan

This section starts with the overall strategy of the project and an overview of its global work plan. Subsequently all individual work packages will be described in detail together with their intended results (deliveries) and interconnections. Also provided are the overall time schedule and principal interconnections between the work packages.

i) Overall strategy of the work plan

One main idea behind the overall project scope and its work plan is to prove on a short time scale of 30 months the viability of the White Rabbit network and its concepts. One constraint necessary to meet this boundary condition is that for the verification of the developed concepts the project will use a single node hardware platform. In order to fit the project to the overall schedule, different tasks will be started as soon as the first viable results from its predecessors have been produced. These draft results will intensively be used for internal project tracing in the scope of risk minimisation and the early start of individual tasks. The illustration of this level of detail is out of the scope of this document.

The project has been divided into eight clearly separated work packages where one of them is the project management. The two work packages responsible for the “system architecture” and “system concept and specification” need a high involvement of most project partners and are therefore led by partners with expert knowledge and experience in these tasks.

In the first stage of the project a detailed system requirements analysis together with an analysis of the state of the art is made. To find a large number of representative use-cases, care has been taken to achieve a balanced European representation of institutes, universities and industry. The participants share comparable work on the system architecture in work package 1 and the resulting architectural specification will be published after a project duration of six months.

In the next project stage this specification will lead to detailed functional specifications of the hardware needed, namely network switches and nodes while making use of existing standards wherever possible. This work package also needs the involvement of most project partners. At the end of this stage, that coincides with the end of work package 2, the system concept is frozen and about half of the project time has passed. At this time other work packages already will have run for up to ten months and have been prepared in a way that they immediately can start with the detailed implementation of the specifications. Especially all preparatory work for the network simulations is finished and the hardware implementation can start.

While the hardware implementation is done in work packages 4 and 5, the simulation of the complete system is continued. Also the validation is started in a way that hardware prototypes can already be completely tested in a test bed. In the last months of the project the same test bed will be used to validate all project concepts and specifications using final hardware deliveries.

Throughout the whole project duration three pillars will be built, linked and checked against each other for mutual benefit and overall consistency, namely: a) specification, b) hardware development, and c) system simulation and hardware validation.

ii) Timings of work packages and their components

In figure 9 the work packages are shown on a time axis relative to the project start. Only the main predecessors of work packages are visualised to get a general overview of the complete project. For detailed interdependencies please see the comprehensive project Gantt chart illustrated in figure 10.
Figure 9: Overview of the project work packages relative to the project start. Main dependencies are also shown.

Figure 10: Detailed Gantt chart
iii) Detailed work description divided into work packages

Work package list. The list of all work packages is shown in Table 3 together with the short name of the institution or company leading each individual work package. Also the beginning and end of each work package relative to the project start (m1) is given.

Table 3: Work package list

<table>
<thead>
<tr>
<th>WP No.</th>
<th>Work package title</th>
<th>Type of activity</th>
<th>Lead part. no.</th>
<th>Lead part. short name</th>
<th>Person months</th>
<th>Start month</th>
<th>End month</th>
</tr>
</thead>
<tbody>
<tr>
<td>WP 1</td>
<td>System Architecture</td>
<td>RTD</td>
<td>5</td>
<td>ZHAW</td>
<td>34</td>
<td>m1</td>
<td>m6</td>
</tr>
<tr>
<td>WP 2</td>
<td>System Concept and Specification</td>
<td>RTD</td>
<td>4</td>
<td>UniBS</td>
<td>77</td>
<td>m4</td>
<td>m15</td>
</tr>
<tr>
<td>WP 3</td>
<td>Network Simulations</td>
<td>RTD</td>
<td>2</td>
<td>AAS</td>
<td>40</td>
<td>m6</td>
<td>m30</td>
</tr>
<tr>
<td>WP 4</td>
<td>Switch Design</td>
<td>RTD</td>
<td>1</td>
<td>CERN</td>
<td>81</td>
<td>m12</td>
<td>m25</td>
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<td>WP 5</td>
<td>Node Development</td>
<td>RTD</td>
<td>3</td>
<td>GSI</td>
<td>64</td>
<td>m13</td>
<td>m26</td>
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<td>WP 6</td>
<td>Validation</td>
<td>RTD</td>
<td>7</td>
<td>COSY</td>
<td>27</td>
<td>m19</td>
<td>m30</td>
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<tr>
<td>WP 7</td>
<td>Dissemination and Exploitation</td>
<td>RTD</td>
<td>6</td>
<td>NI</td>
<td>12</td>
<td>m1</td>
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<td>WP 8</td>
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<td>MGT</td>
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<td></td>
<td></td>
<td>350</td>
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1RTD = Research and technological development; MGT = Management of the consortium.

Deliverables list. All deliverables for this project are summarised in Table 4 where the nature of each deliverable is given together with its due date. Details about all deliverables are given in the subsequent work package descriptions.
Table 4: List of deliverables (in order of delivery date)

<table>
<thead>
<tr>
<th>Del. no.</th>
<th>Deliverable name</th>
<th>WP no.</th>
<th>Nature</th>
<th>Dissemination level(^1)</th>
<th>Delivery date (month)</th>
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<tbody>
<tr>
<td>1.1</td>
<td>System Requirements Analysis Report</td>
<td>1</td>
<td>report</td>
<td>PU</td>
<td>m3</td>
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<td>7.1</td>
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<td>report</td>
<td>CO</td>
<td>m3</td>
</tr>
<tr>
<td>1.2</td>
<td>Constitutive System Design and Architecture Specification Report</td>
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<td>report</td>
<td>PU</td>
<td>m6</td>
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<td>2.1</td>
<td>Standard Compliance Report</td>
<td>2</td>
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<td>PU</td>
<td>m9</td>
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<tr>
<td>7.2</td>
<td>Projected Exploitation Plan</td>
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<td>report</td>
<td>CO</td>
<td>m9</td>
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<tr>
<td>2.2</td>
<td>White Rabbit Technology Evaluation Report</td>
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<td>report</td>
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<td>m12</td>
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<tr>
<td>8.1</td>
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<td>report</td>
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<td>2.3</td>
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<td>2</td>
<td>report</td>
<td>PU</td>
<td>m14</td>
</tr>
<tr>
<td>3.1</td>
<td>Simulation Software and Core Technologies</td>
<td>3</td>
<td>report</td>
<td>PU</td>
<td>m14</td>
</tr>
<tr>
<td>2.4</td>
<td>Switches and Nodes Specification</td>
<td>2</td>
<td>report</td>
<td>PU</td>
<td>m15</td>
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<tr>
<td>7.3</td>
<td>Intermediate Dissemination Report</td>
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<td>report</td>
<td>CO</td>
<td>m18</td>
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<tr>
<td>3.2</td>
<td>System Simulation Scenarios and Limiting Factors</td>
<td>3</td>
<td>report</td>
<td>PU</td>
<td>m19</td>
</tr>
<tr>
<td>4.1</td>
<td>Switch Design Documentation</td>
<td>4</td>
<td>report</td>
<td>PU</td>
<td>m23</td>
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<tr>
<td>5.1</td>
<td>Node Functional blocks</td>
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<td>m24</td>
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<td>8.2</td>
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<td>m24</td>
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<td>4.2</td>
<td>Switch Hardware</td>
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<td>m25</td>
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<tr>
<td>4.3</td>
<td>Switch Simulations and Test Report</td>
<td>4</td>
<td>report</td>
<td>PU</td>
<td>m25</td>
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<td>5.2</td>
<td>PCIe Node</td>
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<td>RE</td>
<td>m26</td>
</tr>
<tr>
<td>6.1</td>
<td>Test System Description and Test Scenarios</td>
<td>6</td>
<td>report</td>
<td>PU</td>
<td>m27</td>
</tr>
<tr>
<td>3.3</td>
<td>Performance Analysis and Large-Scale Scenarios</td>
<td>3</td>
<td>report</td>
<td>PU</td>
<td>m30</td>
</tr>
<tr>
<td>6.2</td>
<td>System Behaviour and Simulation Comparison</td>
<td>6</td>
<td>report</td>
<td>PU</td>
<td>m30</td>
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<tr>
<td>7.4</td>
<td>Final Dissemination Report</td>
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<td>7.5</td>
<td>Final Exploitation Report</td>
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<td>report</td>
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<td>m30</td>
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<td>Final Project Report</td>
<td>8</td>
<td>report</td>
<td>RE</td>
<td>m30</td>
</tr>
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</table>

\(^1\)Dissemination level: \(\text{PU} = \text{Public}\), \(\text{RE} = \text{Restricted to a group specified by the consortium (including the Commission Services)}\) or \(\text{CO} = \text{Confidential, only for members of the consortium (including the Commission Services)}\)
List of milestones Table 5 shows the list of the milestones of the project.

Table 5: Summary of milestones

<table>
<thead>
<tr>
<th>Milestone number</th>
<th>Milestone name</th>
<th>Work packages involved</th>
<th>Expected date</th>
<th>Means of verification</th>
</tr>
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<tr>
<td>1</td>
<td>Architectural Spec.</td>
<td>1</td>
<td>m6</td>
<td>Deliverable 1.2</td>
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<td></td>
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<td>2</td>
<td>System Concept Freeze</td>
<td>1,2</td>
<td>m15</td>
<td>Deliverables 2.2/2.3/2.4</td>
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<tr>
<td>3</td>
<td>Implementation Finished</td>
<td>3,4,5</td>
<td>m26</td>
<td>Deliverables 4.2/4.3/5.2</td>
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<td>4</td>
<td>Project End</td>
<td>all</td>
<td>m30</td>
<td>Deliverables 3.3/6.2/7.4/7.5/8.3</td>
</tr>
</tbody>
</table>

Work packages descriptions. On the following pages detailed descriptions about all work packages, their objectives, tasks and deliverables are given. For the latter also the due date is given as summarised in the list of deliverables (table 4). Each work package description also briefly explains the role of the individual project partners.
**Objectives.** This work package sets up a system architecture and specification that defines the direction of the research and development in the further work packages.

In work package 1 the requirements of the large-scale control network are defined. Input will be collected from partners that have specific requirements for their future real-time control systems and for projected potential applications for clients of some of the project partners. Following this, the work package will generalise the collected requirements to make the system exploitable to the largest possible extent. This includes research of state of the art to check for existing solutions that can be integrated or adapted and to evaluate to what extend existing systems can benefit from the features offered by the White Rabbit network.

As a next step the overall system and subsystems architecture and the definition of the external interfaces of the various integrating modules will be defined. This comprises providing the architecture and global specifications of White Rabbit, including the definition and description of the modules and subsystems inside it.

In summary, the objectives of this work package are:

- To collect and organise all technical and functional requirements.
- To break down the system into functionally independent modules and subsystems; define their relationships to each other, to the environment and the principles guiding their design and evolution.
- To specify consistent interfaces between subsystems that allow the integration of functional modules and define interfaces to devices that can be connected to the system.
- To specify the representation of the system including mapping of functionality onto hardware and software components.

**Task 1.1: System Requirements Analysis.** This task will collect all requirements from the consortium partners regarding their intended use of the system. Also projected potential industrial applications for clients of some of the commercial project partners will be taken into account. Other potential applications such as those in astronomy, ITER, and the Austrian therapy accelerator may be considered to give input to the generalisation of the found requirements that will make the system exploitable to the largest possible extent.

**Task 1.2: State of the Art Analysis.** In task 1.2 state-of-the-art real-time systems, concepts, and algorithms will be evaluated with special focus on determinism and reliability. The project will adopt, merge and alter the ideas of Synchronous Ethernet and Precision Time Protocol to bring it to the next level. In addition, a good understanding of existing standards is needed in order to evaluate the possibility to enhance them with White Rabbit’s
functionality. This analysis will give input to task 1.3 to formulate additional requirements needed for compatibility reasons.

**Task 1.3: Architectural Design and Specification.** The result of this task is one of the main project documents and specifies the complete White Rabbit architecture and protocol from a functional point of view. The detailed hardware and technical specifications will be worked out in work package 2.

**Contribution of consortium partners.** All project partners will be involved in this constitutive work package. ZHAW leads this work package due to its extraordinary role in one of the basic standards used, namely Precision Time Protocol. All partners will take part in the collection of requirements and in the iterative specification and review process to ensure that a true generic architecture is found with a multitude of possible applications.

**Deliverable 1.1: System Requirements Analysis Report (m3).** This report lists and compares all requirements gathered from all project partners. Also requirements from potential future users are included in this document. Furthermore, these requirements are condensed with respect to special topics, e.g., one necessary clock synchronization accuracy that meets all requirements will be given.

**Deliverable 1.2: Constitutive System Design and Architecture Specification Report (m6).** The final system design and architecture specification is the complete description of the system's representation, functionalities and behaviour. It will include the analysis of the state of the art to help understand the rationale behind the developed specification. The resulting specification is the base for all detailed technical and hardware specifications and will be finished already in month 6 of the project.
**Objectives.** The defined tasks in this work package will generate the concepts for the different technologies required in this project, like clock synchronization, scalable real-time support and fault tolerance.

Starting from the results of work package 1 about current systems and standards, the specification of the key elements of the White Rabbit protocol and system is detailed. One of the goals of work package 2 is the definition of a beyond-state-of-the-art solution regarding clock synchronization, since it is the basis on which the real-time support of White Rabbit networks is built. All relevant aspects are treated, including the physical layer.

In the definition of the White Rabbit Protocol there are three crucial points: i) the fault-tolerance is very important when building large systems where fault conditions may lead to injuries or economic losses; ii) the adaptive behaviour when responding to dynamic changing of the nodes; and iii) the seamless scalability of the network up to at least two thousand nodes.

Having in mind these strategic properties of the network, the White Rabbit specifications will be defined and the first two layers of the protocol, the different network nodes and the switch will be specified in terms of characteristics and architectures. This will in turn be input to work packages 4 and 5 where the detailed implementations of the node and switch are developed. Also early draft test system descriptions will be produced to provide input to the system simulation in work package 3.

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**Task 2.1: Interoperability and Standard Compliance.** For interoperability reasons the system to be designed has to be developed following the relevant IEEE and IEC standards. The aim of this task it to give input to the White Rabbit protocol specification task (task 2.4) by evaluating the impact of the detailed extensions to and choices within these existing standards when designing the White Rabbit protocol. The final interoperability and standards compliance will be evaluated and reported in the Standard Compliance Report (deliverable 2.1).

**Task 2.2: Clock Synchronization and Real-Time Support.** This task cares about technology and hardware necessary to reach the set goal to push clock synchronization beyond state-of-the-art achievements for a large Ethernet compliant network. One important condition is that it should be possible to use cheap and easily available hardware components in order to come to solutions that will result in competitive designs. Another important component of this task is research on physical layer solutions and a delay model with the aim of achieving complete delay symmetry in two-way data transmission, a key requirement for high-precision transmission delay compensation. In addition, the subject of avoiding clock quality degradation due to the cascading of many Phase Locked Loops will be analysed in this task. Lastly, the real-time support will be developed in order to satisfy the request for high repetition rates (application cycles) in large-scale systems.
Task 2.3: Fault-Tolerance and Adaptive Network Management. The foreseen applications in large physical facilities will use messages in whole or in part consisting of extremely critical information that can damage expensive systems if corrupted or lost. Furthermore, loss of valuable beam time of accelerators or downtime of production lines could be the result of lost messages. Due to the high real-time demands of the application cases, no handshake is possible between individual nodes upon communication for such special types of message exchange. Fault-Tolerance has to be achieved using special forms of Forward Error Correction (FEC) with extreme requirements to it in the order of $10^{-15}$ allowed communication loss. As a consequence, this task has to evaluate and design appropriate algorithms; fast predictive diagnostic tools will be evaluated to recognise and manage possible potentially dangerous situations. Because of high bandwidth loads foreseen in special use-cases much thought has to be given to specify an intelligent, powerful, zero-configuration network management design.

Task 2.4: Scalability Concept and Protocol Specification. This task defines the “White Rabbit layer 2 Protocol Specification”. Necessary inputs are the results from tasks 2.1 to 2.3 as well as the “Constitutive System Design and Architecture” report (deliverable 1.2). The description of necessary integration and adaption of both Synchronous Ethernet and Precision Time Protocol is the main work within this task. In addition care has to be taken to specify both concept and protocol in a way that seamless scalability up to several hundred connected switches and up to at least two thousand connected nodes is given without any restrictions. This implies that all formulated requirements have to be met by all possible system configurations up to that size compliant with the architectural specification. The concept of plug-and-play will be investigated and defined, because a change in the node number or in the topology of the network should be accepted by the network itself within a limited and known time.

Task 2.5: Switch Specification. This task takes the specification of the White Rabbit layer 2 protocol and defines the functional behaviour of the switches. Switches are a key element of White Rabbit installations and should manage privileged high-priority messages in a transparent way. Special services should be implemented in the switch to support White Rabbit synchronization and to recognise and correctly manage special messages. The switch, for instance, could be programmed to dynamically and statistically recognise the topology and consequently manage the timestamps of actions according to transparent strategies. In this way, nodes that are not enabled with high-priority messages do not require any special driver. For this reason this task should be performed in a strict conjunction with task 2.6 and take advantage from the first results of tasks 2.2 and 2.3.

Task 2.6: Network Node Specification. This task deals with the functional specification of layer 2 of the White Rabbit network nodes. A White Rabbit node will be defined with the capability of incorporating different levels of “intelligence” ranging from simple layer 2 trigger units (capable to generate events based on the common time reference distributed in the White Rabbit network) up to highly integrated devices or interface cards that exhibit full standard Ethernet compliance. Also the functional description of the software interface toward upper layers will be defined in this task.

Contribution of consortium partners. Except for Cosylab, all project partners will be involved in this major work package defining and specifying the further work in the project. ZHAW will provide the input on interoperability and standard compliance. The exact task will be to monitor ongoing activities to meet the compliance requirements defined in the architectural specification. The industrial partners are intended to also deliver input on
the compliance issue as well as support the three main partners (CERN, AAS, GSI) in establishing the specification for the node and the network switch. Further, AAS will take the task of defining the clock synchronization and real-time support of the network. The leader of this work package is UniBS which will support the definition of the protocol as well as the scalability concept with their profound knowledge of real-time networks.

**Deliverable 2.1: Standard Compliance Report (m9).** In this report the attention will be paid to the description of backward compatibility to mature and well accepted standard solutions, as worked out in task 2.1.

**Deliverable 2.2: White Rabbit Technology Evaluation Report (m12).** This report will summarise the preparatory work used to develop the White Rabbit technology. Starting from results of tasks 2.2 and 2.3 it will describe the theory and background information to the developed features in White Rabbit such as the precise timing, real-time support, fault tolerance, and scalability concept.

**Deliverable 2.3: White Rabbit Protocol Specification (m14).** This report, available at the end of the task 2.4 activity, will summarise the characteristics of the White Rabbit technology. Starting from results of deliverable 1.1, the complete specification of the White Rabbit protocol will be created, covering layers 1 and 2 of the OSI communication model.

**Deliverable 2.4: Switches and Nodes Specification (m15).** This report, available at the end of work package 2 activities, will give summarised and detailed functional specifications of both switches and nodes. Following the contents of deliverable 2.1, also hardware characteristics of such devices will be detailed. In particular, this document will describe the different capabilities of devices using the White Rabbit technology (according to their complexity and implemented functions). The differences with traditional and legacy devices will be highlighted and tools for the integration of White Rabbit facilities into existing systems will be provided.
Objectives. The conception and specification will be accompanied by this work package with appropriate focused simulation scenarios to verify the developed concepts against the requirements as defined in work package 1. Simulations in the early stage are intended to get timely feedback to the system architecture about the performance of the developed concepts before the system concept freezes. The main challenge for the simulation software is to properly describe the system’s behaviour according to the architectural and conceptual specification and its hardware implementation. The first developed simulation software and simulation scenarios will concentrate on the unique and customised combination of line embedded frequency carrier, clock synchronization, and special channel access schemes to perform proof-of-concept simulations on small architectures with only essential switch and node interior simulation.

In contrast to that, elaborated simulation software as an enlargement of the afore mentioned will reflect complete switch and node interior behaviour down to all necessary details. It will be capable of simulating realistically scaled architectures with at least two thousand nodes connected and one focus will be simulating already known use-cases at CERN, GSI and existing scenarios of other protocol implementations. Also use-cases in common small and large industrial architectures/environments completely integrated in normal Ethernet networks will be simulated.

Finally, the simulation results are intended to benefit from the small-scale real implementation of the validation work package 6. By modelling realistic traffic flow parameters and verifying the already established models against the test system results the simulation activities will allow upscaling the number of nodes. The gained simulation environment will then predict large-scale performance, design and optimisation. The system simulation will input reference values for the test bed and – in close collaboration with work package 6 – will be updated on a regular basis to incorporate test system results.

Task 3.1: Focused Simulation for System Specification. In the first task of the work package, existing and state-of-the-art simulation tools have to be adapted for the project and simulation modules must be developed to resemble the system specification. Simulation scenarios will be defined in close collaboration with the early test system descriptions worked out in work package 2. In order to find out about the main influences of the intended features, only a small number of nodes will be simulated, which allows focusing the effort on evaluating the main ideas of the project and their feasibility.

The system concept and specification work package (WP2) will provide the necessary inputs for early simulation runs, which will then give answers to scalability and performance. Furthermore, the task is meant to deliver information about possible architectural limitations and the feasibility of the core technologies. The early stage of the available modules will be reflected in only implementing the most important functionalities to allow for a fast feedback to the specification process.
Task 3.2: Core Service Performance Simulation. In order to early identify possible bottlenecks and requirements for the node and switch implementation, special attention will be paid to simulation scenarios that include a representative number of stress tests. These include high bandwidth load simulations, huge amount of both normal Ethernet and time-critical White Rabbit traffic as well as simulations of high bit error rates. All three types will evaluate the system in extreme situations to find out about the network behaviour under critical conditions and the respective fault tolerance and automatic recovery.

Besides the required simulation models for the interconnection of the basic network models, also simulation scenarios for the counter measures (e.g., forward error correction) have to be developed. The latter are necessary since delay-critical real-time traffic does not allow for any kind of handshake and therefore techniques for delivery with very high probability have to be designed. As a result of these simulations first corrections to switch standard parameters or even the implementation are foreseen. Simulation scenarios have to cover the complete range of switch functionality with focus on layer 2 as well as network architectures with tens of nodes as expected for the validation in work package 6.

Task 3.3: System Simulation. The aim of this task is to simulate realistic scenarios regarding the number of switches, nodes and topologies used. The work will be done in very close relation to WP6 by using different simulation scenarios and comparing the results of the identical setups in the test system to the simulation output. The validation of the implementation against the simulation gives essential input in order to upscale the simulation scenario to a high number of nodes, allowing to identify important network parameters for large-scale control systems. It is of special importance to also simulate these large-scale simulation scenarios in extreme situations and conditions in order to ascertain real values for reliability, clock synchronization or throughput, which can then be checked against all requirements. Tuning of switch internal resources and system parameters will be an important aim of this task. System simulations also include standard test scenarios using for example realistic traffic shapes recorded from the validation setup, start-up and fault behaviour, as well as theoretical tests to examine influences on the overall system performance.

Contribution of consortium partners. AAS will lead this work package and contribute its existing broad knowledge regarding simulation of large-scale clock synchronizing networks. This know-how will be extended in the course of the first task of work package 3 by the necessary background information about simulation of real-time networks. Models for accurate simulation of oscillators in discrete event simulators – developed in the course of previous AAS projects – will be used to verify the high-accuracy constraints. In addition existing simulation setups can be used as a quick start to check early ideas on communication techniques against the requirements gathered in task 1.1. Cosylab will support the activities by providing information about realistic simulation and test scenarios using their knowledge on different accelerator facilities worldwide including design studies they worked out for CERN and GSI. The consortium will install a validation test bed setup at Cosylab that will provide important feedback about matching simulation and real world scenarios. Additionally, the large involvement of Cosylab in work package 5 together with their leadership of work package 6 allows for code re-usage in simulation models. Cosylab will therefore take part in the development process of models for protocol and hardware simulation. The expertise in designing real-time protocols is an important part of the simulation provided by UniBS. Their contribution to the work package will include the development of models for real-time protocols and accompanying support on optimising the real-time parameters of the designed protocol by appropriate definition of simulation scenarios. UniBS will notably support the identification and examination of peak load scenarios.
Deliverable 3.1: Simulation Software and Core Technologies (m14). This deliverable contains the first validated simulation software version needed for early stage feedback where there are still restrictions to the simulation of detailed hardware and scalability. It includes the decision for the necessary software and all required information to set-up and run individual simulation scenarios. The performance will be evaluated on layer 2 of the network including a few number of nodes and at least one switch, depending on the requirements of the scenario. Furthermore the deliverable will show and document the feasibility of the chosen core technologies specified in work package 1 justifying the design decisions made.

Deliverable 3.2: System Simulation Scenarios and Limiting Factors (m19). This report will describe the limiting factors for the overall performance of the system, based on a detailed system simulation including the input from the switch and node specification work packages. I.e. the used simulation models of task 3.1 will be expanded by specific implementation parameters such as queue lengths, memory sizes, and processing speed, in order to gain significant results on the network capabilities with given resources. The results and found insights will also be used in task 6.1 to define meaningful validation test scenarios.

Deliverable 3.3: Performance Analysis and Large-Scale Scenarios (m30). This deliverable contains the final version of the simulation environment. It includes all software necessary. A detailed discussion of the obtained results as well as the comparison between the implemented validation setup and the corresponding simulation scenario will be given. The close interaction with the work package on validation will allow realistic scenarios even for large-scale control systems. The final results given in this deliverable are meant to prove the applicability of the system on the scenarios defined in the system requirements analysis.
Objectives. As the central element in an Ethernet based network special attention has to be paid to the switch. In White Rabbit, the switch will be responsible for timing distribution and controlling data transfer to guarantee short and deterministic latencies between nodes, while at the same time fully respecting the Ethernet standard. For this purpose, the different building blocks specified in work package 2 need to be implemented in hardware and software depending on criticality and complexity, respectively.

This work package will also implement the actual functional block for packet relaying, which includes the implementation of the actual Media Access Control (MAC) protocol for the switch. The MAC block will be reused in the real-time node implementation.

Task 4.1: Packet Relaying and Protocol Implementation. The packet relaying structure includes a MAC block with precise time-tagging capabilities for both incoming and outgoing traffic. It also encompasses the fast hardware fabric to deterministically relay packets between the different switch ports. Within this task also more complicated and less time-critical functions like the Rapid Spanning Tree Protocol are implemented in firmware.

Task 4.2: Timing Hierarchy. The switch timing functional block includes:

- Clock recovery from its uplink.
- Internal clock conditioning and phase shifting.
- Clock distribution for internal logic and downlink ports.

In addition, special care must be put on the implementation of the different Phase Locked Loops in the switch because cascading Phase Locked Loops in a non-controlled way may lead to instabilities or at least serious clock quality degradation. In this regard, results from task 2.2 will be used and confronted with reality.

Task 4.3: Platform Development. Once tasks 4.1 and 4.2 have delivered the designs of the key functional blocks, the switch must be implemented using a hardware platform which guarantees clock signal quality, appropriate power supplies and cooling, easy servicing and monitoring, and extensibility. Task 4.3 deals with these choices and with the actual development and fabrication of a switch. This task starts well before the end of tasks 4.1 and 4.2 with the development of principles specified in deliverables 1.2, 2.1, 2.2, and first results from task 4.1.

Task 4.4: Hardware Simulation and Implementation Test. The switch is a complicated system integrating hardware and software. In order to validate its behaviour under different traffic scenarios, it is important to be able to simulate the whole system and to test the final hardware to make sure simulation and reality match.
Contribution of consortium partners. The development of the switch is the most essential hardware ingredient in the White Rabbit network. CERN will take the lead and appeal to other consortium partners for specific knowledge and contributions within this work package. More specifically, AAS, ZHAW and UniBS will help in design aspects related to cascading Phase Locked Loops and to Ethernet compliance. CERN and GSI will carry out the complete implementation, while HAC and OREG will impact the platform choice with considerations on industrialisation and manufacturability.

Deliverable 4.1: Switch Design Documentation (m23). This includes the complete schematics and layout files along with a design description document justifying the technical choices and explaining the switch internal workings. It also contains the IP core for the MAC block.

Deliverable 4.2: Switch Hardware (m25). This deliverable concerns the actual switch, presenting together the results of task 4.2 and task 4.3, due to their interdependence. More specifically, the delivery of three switches to be used in the tests for deliverable 4.3 and in the validation test bed of work package 6.

Deliverable 4.3: Switch Simulations and Test Report (m25). This includes the complete documentation of the hardware simulation system and a report presenting simulation results along with actual testing data, thus establishing the validity of the simulation results.
Objectives. The aim of this work package is to implement the network end nodes for timing and data transfer so that the theoretical concepts can be verified. This requires appropriate hardware as well as software modules and matching drivers. The hardware of the network nodes will be developed as re-usable modules in order to support various bus interface systems and configurations as specified in work package 2. To reduce design time the actual implementation to be delivered in this work package will target the commonly used PCIe bus standard. Along with the hardware this work package will deliver all software needed to use and test the cards.

Task 5.1: IP-Cores. This task is concerned with the development of all the Intellectual Property (IP) cores needed in the end nodes, except for the White Rabbit MAC developed in work package 4. These cores will include a dedicated fully deterministic lightweight CPU with a reduced instruction set whose purpose will be interfacing the hardware part of the nodes with the non-deterministic host software.

Task 5.2: Drivers, Software and Libraries. This task includes the low-level software needed to control the nodes: CPU assembler, device drivers and libraries. The device drivers will be developed for the Linux operating system while the rest of the code will be completely portable to other software platforms. In addition, this work package includes a test program in user space allowing a complete test of the cards after manufacturing and also for debugging purposes.

Task 5.3: Node Module Implementation. The node will be implemented in the PCIe form factor using a standard Ethernet chipset and Field Programmable Gate Array (FPGA) technology. Special care will be devoted to the clock management section of the design where PLLs have to be fine-tuned to guarantee optimal phase noise resulting in minimal jitter. The clock synchronization technology developed in task 2.2 will provide the means for high precision phase measurements on a standard FPGA via a digital PLL. The node’s own CPU will cover the necessity for timing protocols over Ethernet to complete the time synchronization process in the same way as the White Rabbit switch.

Contribution of consortium partners. With its extensive design and implementation experience GSI will lead this work package. Since this work package demands substantial amounts of manpower, CERN will also participate in design and implementation at all levels. COSY will contribute HDL design know-how, integration and subsystem testing. OREG will participate in design reviews and ensure that the final product is optimal in terms of manufacturability, testability and price/performance ratio.
### Deliverable 5.1: Node Functional blocks (m24)
This deliverable includes the full documentation of the IP-cores and software developed for implementing the White Rabbit node. It will contain a detailed description of the rationale behind all implementation choices for both HDL code and software.

### Deliverable 5.2: PCIe Node (m26)
This deliverable concerns the actual hardware boards and its documentation, merging results of task 5.2 and task 5.3, considering their high interconnection. Ten units, along with the three switches delivered in work package 4, will be delivered to set up a complete system test environment in work package 6. The accompanying report will include complete schematics, layout and manufacturing files.
Objectives. In this work package achieved project results have to be verified against the goals that were defined in work package 1. To accomplish this, appropriate test scenarios will be developed and organised to challenge the developed switch (WP4) and node hardware (WP5) from intended use-cases to extreme situations on a small test bed. In work package 3 test scenarios will have been developed on the basis of system requirements that were formulated in work package 1. In addition to that, test scenarios will include stress tests regarding for example network load, link error statistics and environmental conditions. Furthermore, all test scenarios and the network simulations from work package 3 will complement one another for mutual feedback. Real test execution starts as soon as first hardware prototypes are available and from then on the test bed will continually grow in order to test all developed hardware. Also the interplay with selected standard components will be tested.

The main aim of this work package is to integrate all the systems, components, hardware and software modules that have been developed in work packages 4 and 5 into a complete system in order to evaluate, fine-tune and demonstrate the overall objective of the project in a real network environment using all topologies from deliverable 1.2. The measured values will be used as feedback for the system simulation for upscaling the results.

Feedback of the validation will be used to fine-tune and optimise the systems and to confirm it is behaving as required.

Task 6.1: Test System Modeling and Validation Specification. A validation model will be conceptualised and constructed to objectively measure compliance with requirements defined in work package 1. Validation will be confirmed against i) the needs of an end user of a synchronization and event distribution network, and ii) the compliance with base standards (work package 2). Following the construction of the validation model testing procedures will be defined to allow repetitive measurements and compliance tests with requirements specified in work packages 1 and 2. Special attention will be given to covering end-user use-cases while at the same time system-performance simulation results will be challenged to provide consistent results.

Task 6.2: Testbed Integration. System integration will be done based on deliveries of the work packages 4 and 5 to allow execution of testing procedures under all test scenarios defined in task 6.2. Besides switches, nodes (work packages 4 and 5) and normal standard Ethernet devices (to prove compliance, as defined in task 2.1) this will also involve the integration of the aforementioned front-end controller.

Task 6.3: Test Execution and Result Assessment. Tests defined in task 6.2 will be performed on the test-bed built in task 6.3. Extensive testing will be done to validate high precision and long-term stability (node to node via several layers of switches). This will require the integration of special equipment for automated measurement and postmortem data processing.
Contribution of consortium partners. The test system will be defined, programmed and
set up at COSY. Important input and mutual iterative advancements will be performed with
the simulation results achieved in work package 3 provided mainly by AAS. Switch and node
hardware will be delivered from CERN and GSI (deliverables 4.2 and 5.2, respectively).

**Deliverable 6.1: Test System Description and Test Scenarios (m27).** The test system
description will comprise documents covering the test bed setup, including representative
end-user use-cases and testing procedures. Documents will allow any of the partners to
rebuild the test bed with repetitive results. Testing procedures and validation points will be
traceable back to system requirements defined in work packages 1 and 2. The documentation
will be in pdf format and/or system modelling tools like for example Enterprise Architect. An
automated measurement and post-mortem data analysis will be done to provide statistical
results for the synchronization between nodes, reaction times and other important system
parameters. Stress will be put in the performance of the individual switches and nodes.
The results will be analysed and presented in a requirements-compliance document that will
include multiple use-cases.

**Deliverable 6.2: System Behaviour and Simulation Comparison (m30).** This report
summarises the results of the complete behaviour under the different test conditions applied
to the integrated test bed and concentrates on overall performance and scalability issues,
rather than on individual switches and nodes addressed in deliverable 6.1. Simulation results
achieved in work package 3 will be challenged against real system performance. It lists
meaningful parameter values and gives advice regarding possible system optimisation or
possible required changes of specification details.

Apart from dissemination and exploitation this report is the last project document to be
delivered and will prove the validity of the project’s architectural and functional specification.
### Objectives.

This work package establishes the planning, design and dissemination of the project and its foreground IP. A swift and effective dissemination is an important task that will contribute to make potential customers and developing partners understand and appreciate the technology. Besides normal scientific dissemination tools (publications in conferences and workshops), special dissemination activities will be planned and promoted to address selected user groups and non-technical audiences. The exploitation of White Rabbit in research facilities is guaranteed and activities conducted by the industrial partners will encompass market considerations.

Dissemination and exploitation activities will be opened at the very beginning of the project and will remain active for the whole duration.

<table>
<thead>
<tr>
<th>Work package number</th>
<th>7</th>
<th>Start date or starting event:</th>
<th>m1</th>
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<tbody>
<tr>
<td>Title</td>
<td>Dissemination and Exploitation</td>
<td></td>
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<td>Activity type</td>
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<tr>
<td>Short Name</td>
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<td>AAS</td>
<td>GSI</td>
</tr>
<tr>
<td>Person-Months</td>
<td>1</td>
<td>2</td>
<td>2</td>
</tr>
</tbody>
</table>

**Task 7.1: Dissemination.** The promotion and dissemination of the project is divided in two actions according to the communication platforms used, namely digital and conventional media. In pursuit of optimising the dissemination effort in a general way, two target audiences have been defined as the project interest: the scientific community and the technical industry.

Digital media, where the main source of information lies in the web site, will provide updated information regarding project objectives, technical designs, progress, achievements, demonstrations and promotional material. In order to reach the target audience, press release articles about the project on on-line first-rate publications will be distributed.

Conventional media dissemination will focus on the production of info material to display and disseminate project concepts and achievements together with participation in fairs and workshops. In order to match with the particular interest of every audience the activities will be adapted.

The scientific community will know about the project through the participation at important events, conferences and workshops. The project results also will be published in scientific papers.

The industrial market is always a challenging task for dissemination and will be addressed by participating in trade fairs and individual participation in industrial related events of each partner. At the same time the industrial partners will provide information of the project through their commercial network to their customers and partners.

The open source license scheme proposed to distribute the developed knowledge and IP is in itself a powerful strategy of dissemination, since this model eases the collaboration with industry and allows SMEs, big companies and the scientific community cheap adaptation of the technology.

**Task 7.2: Exploitation.** Exploitation of the results is expected within a short time by the research institutes GSI and CERN, since they will embrace the technology developed in the project for their research facilities. The new knowledge obtained in the project will increase...
the technical value of the companies in the market and expand their business horizon by putting White Rabbit into practice.

**Contribution of consortium partners.** NI will lead this work package. It’s capabilities in marketing technologies across multiple industries will give a professional direction to the dissemination and exploitation efforts. Most other participants will also participate in global and individual efforts to make the results of the project known and used. Section 3.2 explains these plans in detail.

**Deliverable 7.1: Projected Dissemination Plan (m3).** This plan will describe the map for dissemination which will follow the project progress. Intended dissemination steps will be listed such as conference participations. This plan will give a good illustration about the White Rabbit intended level of dispersion.

**Deliverable 7.2: Projected Exploitation Plan (m9).** In this deliverable a detailed exploitation plan is presented. It will display intentions regarding placing White Rabbit technology into the industry and institutions and will enlist the potential users that will be targeted by the project.

**Deliverable 7.3: Intermediate Dissemination Report (m18).** This report will describe the dissemination effort and achievements accomplished during the project’s flow. All achieved dissemination steps will be listed and referenced, like publications or participated conferences. After half of the project’s runtime and system concept freeze, this report will give an illustration of the spreading of White Rabbit.

**Deliverable 7.4: Final Dissemination Report (m30).** In this deliverable, the report of deliverable 7.3 will be updated and will summarise a referenced list of dissemination steps.

**Deliverable 7.5: Final Exploitation Report (m30).** This deliverable will summarise exploitation achievements for White Rabbit, showing industrial and institutional acceptance. This report will also list the users that have adopted White Rabbit or are planning to use it in the future.
**FP7-ICT-2009-5**  
**23/10/09 v1**  
**STREP proposal**  
**White Rabbit**

<table>
<thead>
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<td>AAS</td>
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<td><strong>Person-Months</strong></td>
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<td>1</td>
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</table>

**Objectives.** The aim of this work package is to provide the project management and the overall coordination of the technical activities, the financial and technical planning and the control functions needed to ensure that the project objectives are met. This work package, via the person of the Project Coordinator, provides the principal point of contact between the project and the Commission as well as to interested parties who are not part of the project. It also addresses any issues concerning the membership of the project, including the case where partners join or leave the project during its duration. It is assisted in its tasks by other bodies established as part of the management structure.

**Task 8.1 Project Coordination.** The management structure used for the project is described in section 2.1 of this document. The Project Coordinator will liaise with the Commission and will be the contact point between the project and the Commission. The Project Manager will carry out overall project management in close consultation with the members of the Project Management Committee and the Technical Committee. The membership and roles of the Project Management Committee and Technical Committee are defined in the Consortium Agreement, as are the rules for distributing the advance payment and the settlement of subsequent cost claims.

Work Package Leaders will be responsible for technical work done within their work packages. They will supervise work packages and task progress and communicate the content and progress of project deliverables to the Project Manager. This work package will first establish the structures and procedures necessary for the project management. It will then ensure that the contractual requirements of the project are met in accordance with the work plan and the allocated budget. Work package 8 will also manage the process of handling internal disputes, dealing with non-performing partners and any changes of project partners.

The work to be performed consists of the following tasks:

- **Establishing project management procedures:**
  - Prior to signing the contract, the Project Management Committee will formally establish the roles of the main “actors” in the management of the project which are documented in the Consortium Agreement; the Project Coordinator, the Project Manager, the Project Management Committee, the Technical Committee and Work Package Leaders.
  - Rules for distributing advance payments and settlement of subsequent cost claims.
  - Establishing the procedures for reporting, collecting and collating reports and sending them to the Commission.

- **Performing project management duties:**
  - Controlling project scheduling and achievements.
– Producing regular progress reports and resource expenditure reports.
– Organisation of the Full Project Meetings and meetings of the Project Management Committee, the Technical Committee as well as Review Meetings.
– Handling the cost claim procedures and maintaining the budget status of each partner.
– Maintaining the technical description of the work and the Consortium Agreement.
– Approving and validating the visible outputs, such as deliverables, presentations, papers, etc., thus adding a level of quality assurance to the project.
– Managing intellectual properties and patent requests.
– Supervising the project website and maintaining project e-mail lists.

**Contribution of consortium partners.** As CERN will provide the Project Coordinator and the Project Manager it will lead this work package. All other participants will be concerned as the project management structure depends on the involvement of all project partners.

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**Deliverable 8.1: Periodic Report (m12).** This document will cover all management-related information after one year of the project’s runtime.

**Deliverable 8.2: Periodic Report (m24).** This document will cover all management-related information after two years of the project’s runtime.

**Deliverable 8.3: Final Project Report (m30).** In this final report all management-related issues of the project will be summarised. Horizontal project related issues including gender, science and society related aspects will also be covered in this deliverable.
Summary of effort. In table 6 the summary of the project partners efforts is shown. Note that this amount of person-months only accounts for the amount necessary to achieve the aspired EU funding. Actually the committed resources will be considerably higher as described in section 2.4.

Table 6: Summary of Effort

<table>
<thead>
<tr>
<th>Partic. no.</th>
<th>Partic. short name</th>
<th>WP1</th>
<th>WP2</th>
<th>WP3</th>
<th>WP4</th>
<th>WP5</th>
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<td>-</td>
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<td>-</td>
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<td>-</td>
<td>-</td>
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<td>64</td>
<td>27</td>
<td>12</td>
<td>15</td>
<td>350</td>
</tr>
</tbody>
</table>

The bold numbers identify the work package leaders.

iv) Work package tasks interdependencies

Figure 11 gives a graphical presentation of the dependencies between individual work package tasks. The critical project path is marked in bold.

v) Risks and associated contingency plans

Risk assessment. While the organisation of the risk management structure is described in section 2.1, all possible significant risks to the project are listed in table 7. They have been identified and classified according to their likeliness and impact to the project based on present assessment. One main goal of work packages 1 and 2 is to further minimise the likeliness of technical risks through proper consideration, specification and design. Only those risks are included where the influence to the project is at least moderate or serious and all result only in project delay since no risk with the danger of project collapse could be identified. Indeed during workshops feasibility considerations were already discussed in depth.

In the following sections each of the identified risks is discussed in terms of its possibility and seriousness. Also the associated contingency plans are described.

1. Negative simulation results regarding scalability. Especially in large networks most parameters like load overhead, throughput or performance do not scale. Therefore today it is likely that concepts and specifications starting with a bottom-up approach meet unanticipated problems. One main goal of work packages 1 and 2 is to identify such problems and to solve them already in the beginning through thorough analysis and specifications. The risk is identified as moderate since it is known from the beginning and a period of one year of simulation precedes the milestone “System Concept Freeze”.

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Figure 11: Dependencies between the individual work package tasks. The critical path is marked in bold.
Table 7: Significant project risks

<table>
<thead>
<tr>
<th>No.</th>
<th>Risk</th>
<th>Likeliness</th>
<th>Influence</th>
<th>Impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Negative simulation results regarding scalability</td>
<td>likely</td>
<td>moderate</td>
<td>delay</td>
</tr>
<tr>
<td>2</td>
<td>Testbed execution shows insufficient system behaviour</td>
<td>possible</td>
<td>serious</td>
<td>delay</td>
</tr>
<tr>
<td>3</td>
<td>Considerable delay in individual project tasks</td>
<td>possible</td>
<td>moderate</td>
<td>delay</td>
</tr>
<tr>
<td>4</td>
<td>Cancellation of an individual project member</td>
<td>possible</td>
<td>moderate</td>
<td>delay</td>
</tr>
<tr>
<td>5</td>
<td>Insurmountable problems regarding standard compliance</td>
<td>improbable</td>
<td>moderate</td>
<td>delay</td>
</tr>
<tr>
<td>6</td>
<td>Impossibility to implement accuracy requirements</td>
<td>improbable</td>
<td>serious</td>
<td>delay</td>
</tr>
<tr>
<td>7</td>
<td>Impossibility to implement reliability requirements</td>
<td>improbable</td>
<td>serious</td>
<td>delay</td>
</tr>
<tr>
<td>8</td>
<td>Cancellation of a project partner</td>
<td>improbable</td>
<td>serious</td>
<td>delay</td>
</tr>
</tbody>
</table>

In case unforeseen problems in this area arise, more manpower resources will be needed despite the fact that already now more than 10% of the project’s manpower is foreseen exclusively for the simulation work package.

2. Testbed execution shows insufficient system behaviour. The impact of this risk is serious because the validation work package is the last to start due to the necessity of a finished hardware implementation. Therefore any unrecognised problems showing up during test executions bear the danger of considerable project delay and additional budget and manpower needs. To minimise this risk, care will be taken that the simulation models truly resemble the system and that all possible error sources or scalability problems are accounted for in the simulation scenarios and in early hardware implementation tests.

If unforeseen problems arise, more engineering resources will be put in to detect and correct the reasons for discrepancies between simulations and actual hardware behaviour.

3. Considerable delay in individual project tasks. The influence of this risk is moderate. In a detailed individual task analysis only six tasks are on the critical project path (cf. figure 11). With the exception of task 1.1, they have durations between six and twelve months. The Project Manager and all work package leaders focus on those tasks and make use of known project management tools for task supervision and control.

As contingency plan certain tasks could need additional resources from other partners or external help could be called in in the form of partnerships or commercial outsourcing.

4. Cancellation of an individual project member. It is not uncommon for a project with several industrial partners and institutes involved that one or more persons will leave his or her job within the project time. Therefore care will be taken that all project knowledge is documented and shared among all project partners and among themselves.

In case of loss of a project member at an early stage a suitable successor has to be found internally or hired for the job. At a late stage the work will be distributed among the partners.

5. Insurmountable problems regarding standard compliance. This risk is classified as improbable with only moderate influence. The whole project is based on well-known standards and the consolidation of the two selected standards fits nicely together as preparatory work already showed. Since there exists no standard for the project’s
aim because it is beyond state-of-the-art technology, the only care to be taken is that all adaptations follow their individual standards to the maximum possible extent.

In case it actually proves to be impossible to fully comply to existing standards, we may have to drop the compliance requirement. However, in most cases it will be possible to limit the effects of this. E.g., as in a White Rabbit network each node is connected to a White Rabbit switch, this switch may be (re-)designed to convert or hide any traffic that would not be compatible to existing connected equipment.

6. **Impossibility to implement accuracy requirements.** Preliminary tests have shown that the required timing accuracy can be met on a single link, while the cascading of several PLLs has been done successfully in particle physics detectors. All other delay measurements are implemented digitally. The likeliness is therefore considered low.

In case the accuracy requirements were not reached within the allocated project time, the influence would be serious as it may need additional resources for the development of new approaches in phase and frequency locking and innovative circuit designs.

7. **Impossibility to implement reliability requirements.** With existing and proven algorithms for Forward Error Correction there are known ways to reduce error-proneness through proper parameterisation, higher redundancy factors or adaptations of the used algorithms themselves. The usage of the Gigabit Ethernet link layer is of considerable importance regarding the mentioned enlargement of redundancy factors that would not be possible on slower connections.

In case it appeared that it is impossible to implement reliability requirements, one will have to find the actual cause for it, which will be in the area of signal quality, EMC, connectivity or fibre-optics. The partners do have knowledge in these fields.

8. **Cancellation of a project partner.** This risk can be classified as highly unlikely for CERN and GSI since they have the responsibility to develop and renovate their large-scale facilities and need White Rabbit as a key technology since no alternatives exist. The same holds for COSY since they will be official in-kind contributor for the FAIR facility at GSI. All partners have an intellectual or commercial interest in the success of the project and made commitments to participate in the project for its duration with contributions as described in table 6 and section 2.4. Furthermore all of the partners are financially solid.

Although unlikely in the short project time span, it still is possible that a partner may change the focus of his company or institute. In this case the remaining work has to be redistributed between the remaining partners and tasks may be delayed.

**Risk contingency plans** Since it could be verified that the most serious impact of all listed risks is considerable project delay, the overall strategy in the case of risks occurrence is to concentrate more work on the individual tasks in time or enhance the efficiency of the task under consideration. Even more important is the avoidance of any project delay from the beginning. Therefore not only the projects critical path as shown in figure 11 has been identified but also all tasks interdependencies on a level beyond the scope of this application.

In compliance with the project’s “Management structure and procedures” (section 2.1), the following escalation steps are foreseen:

1. Each person responsible for an individual task has to check its progress on a monthly base for tasks exceeding six months duration. For shorter tasks each fortnight or even once a week. This information will be given to the work package leader to distribute it following the “Information Flow” and “Planning and Reporting” procedures described.
2. As soon as any possible delay is identified, the partners discuss solutions following the “Decision-Making Process” and raise the problem to the Technical Committee if no sufficient solution can be found. In the first level of escalation the internal discussion will be performed via email exchange, phone calls or video conferences between the partners.

3. If the possibility of the project end date being at big risk is identified by any participant, the Technical Committee as well as the Project Management Committee have to be informed immediately. They will decide on further steps to resolve the problems like setting up a “task force” where all relevant experts concentrate their work on the task at risk.

In conclusion, technical risks are minimised thanks to the technical competence and previous experience of the partners. In addition, continuous monitoring of the project as specified in work package 8 will allow the consortium to pro-actively deal with potential problems before they can compromise a technical task.
2 Implementation

2.1 Management structure and procedures

The management structure of this project as shown in figure 12 will ensure the coordinated execution of the various activities within the project. Special attention will be given to the quality and timeliness of the project deliverables, reporting to the European Commission and disseminating results to interested parties. This project will be undertaken by several independent partners whose modus operandi will be based on consensus, with no partner allowed to impose their wishes on the others. The management of the project will be carried out using a simple and proven structure with clearly distributed responsibilities, both vertically and horizontally.

The Project Coordinator and the Project Manager will be provided by CERN. CERN has experience in managing very large research infrastructures and expertise in leading large-scale collaborations involving many institutes from all over the world. The administrative, legal and financial services of the organization will provide support to the Project Coordinator and Project Manager. CERN has participated in more than 60 projects under FP6 and FP7 and has coordinated more than 20 of those.

Project Coordinator

The Project Coordinator (Javier Serrano/CERN) will be responsible for all communication between the members of the project and the European Commission. The Project Coordinator will also be the technical lead of the project and, as such, will be aware of, and involved in, all technical decisions which affect the outcome of the project.

Project Manager

The Project Manager (Erik van der Bij/CERN) will be responsible for all internal project administration tasks. This role will include: project planning and monitoring, the production of progress reports, milestone reports, budgetary overview and reviews. He will also be responsible for the internal distribution of project documents, reports, statements of expenditure, minutes
of meetings and other information from partners. He will be responsible for the control of the project schedule. The Project Manager will report to the Project Coordinator and will be in constant communication with the Work Package Leaders to make sure that their deliverables are on schedule.

Work Package Leaders

A work package (WP) in general consists of several tasks which together represent the work package’s goal. Each work package will be under the control of a Work Package Leader who will be responsible for the technical coordination within the work package. The Work Package Leader also will ensure that the activities of the WP proceed according to the overall project work plan. Each Work Package Leader is responsible for ensuring the production of the agreed deliverables and reports within their WP. They are also responsible for identifying potential risks or potential problems and for bringing these to the Technical Committee when necessary.

To keep a light management structure and as the largest WP needs only an 81 person-months effort, it has been decided to not introduce another management level of so-called task leaders.

Project Management Committee

The Project Management Committee comprises one representative from each partner plus the Project Manager and will be chaired by the Project Coordinator. This committee’s role is to ensure a smooth coordination of the project at both a technical and administrative level. The Project Management Committee will be the ultimate authority, within the project, for all strategic, technical and financial decisions and will also be responsible for the distribution of resources within the project. Any major change in the project e.g. if a partner decides to leave the project, the redistribution of tasks will have to be decided by the Project Management Committee. Decisions will be taken by consensus whenever possible. In the case where a consensus is not possible, the partners will each have one vote. In case of a tie vote the vote of the Project Coordinator can be used as a casting vote. The Project Management Committee will be the final arbitrator for all decisions related to the Intellectual Property (IP) rights of project deliverables. To reduce costs the Project Management Committee will try to carry out its work without the need for formal meetings. The Project Management Committee will nevertheless meet at least once every 12 months, at the time of the Full Project Meetings.

Technical Committee

The Technical Committee will comprise the Project Coordinator and all Work Package Leaders and will be responsible for ensuring that the technical developments are well coordinated and that technical information is available to all partners. The Technical Committee is where the exchange of technical information between work packages will be carried out. The Technical Committee is a forum for technical discussion and where technical decisions are taken. It will not necessarily hold formal face-to-face meetings. Instead, communication within the Technical Committee will take place mostly by e-mail, telephone or by video-conferencing. The Technical Committee will be chaired by the Project Coordinator. The Technical Committee will nevertheless meet at least once every 12 months, at the time of the Full Project Meetings.

Working groups

According to the needs of each work package, Working Groups may be created, in agreement with the Technical Committee, to address specific technical problems that cross work package boundaries. These Working Groups will carry out their agreed task, report their conclusions to the relevant Work Package Leaders and then disband. The Working Groups in figure 12 are shown as example.
Information flow

Many types of information will need to circulate within the project:

- Technical information will be generated within each work package and will be disseminated by each Work Package Leader within the project using the project reporting tools.

- Planning information will be generated within each work package and will be distributed within the project by the Project Manager.

- Information on project deliverables will be distributed within the project by the Project Coordinator.

- Reports for the European Commission will be produced by the Project Manager and transmitted to the Commission by the Project Coordinator.

The tools the project intends to use to distribute such information are:

- Regular progress reports from each work package or from any working group that has been set up to address specific technical problems.

- Technical presentations by the partners at project meetings.

The project will use its web-site and modern tools, e.g. web-based tools like “wikis” and journalled file shares for the project, to guarantee the distribution and availability of all project-related information to interested parties. To simplify project monitoring, each Work Package Leader will be expected to provide regular updates to the Project Manager who will check, collate and store this information so that it is available to all project members.

Planning and reporting

Project planning and progress will be documented in two Periodic Reports and one Final Project Report. These reports are project deliverables and will be sent to the European Commission. These documents will be produced by the Project Manager, and compiled from inputs from the Work Package Leaders. The Project Management Reports will contain information on achievements and the use of resources within the project.

Meetings

In an attempt to reduce costs, formal “face-to-face” Management and Technical meetings will be held infrequently at the project partners. If, when and where such meetings are deemed necessary, they may alternate between the premises of the partners. At least every 12 months a Full Project Meeting will take place during which the Project Coordination Committee and the Technical Committee will meet. The Full Project Meeting will be organised by the Project Manager and Work Package Leaders will be encouraged to hold technical meetings in parallel or attached at the same venue. The organisation of these technical meetings will be the responsibility of the Work Package Leaders but the overall programme of these parallel meetings will be coordinated by the Project Manager to maximise the attendance and ensure that the relevant experts are present.

Decision-making process

The management structure implemented for this project is aimed at achieving consensus on most issues. If this is not possible, a vote will be taken within the Project Management Committee. Each partner will have one vote and can be replaced by a proxy. Decisions will be endorsed
by a simple majority among all the partners. Additionally, specific decisions and corresponding voting procedures may be defined by the Consortium Agreement.

When decisions need to be taken at the level of a work package, the partners involved in the activities of the work package will try to reach an agreement based on technical arguments with the help of the Work Package Leader. If an agreement cannot be reached the problem shall be raised to the Technical Committee for a decision and will only be passed onto the Project Management Committee when no consensus can be reached within the Technical Committee.

**Quality assurance policy**

Deliverables are the outputs of the project and are detailed in section [1.3](#). Their production is the responsibility of the Work Package Leader. To ensure the quality of the work performed an internal review process will be carried out on a task basis under the responsibility of the relevant Work Package Leader. After this review, the document will be sent to the Project Manager who will check the deliverables for consistency and make sure that the results are in agreement with the requirements of the project. Once accepted by the Project Manager, the document will be sent to Project Management Committee for formal approval.

**Risk management**

White Rabbit is a project with ambitious objectives and the Project Management is aware of the risks associated with it. It is the task of the Project Manager to constantly monitor the project progress in order to be able to cope with unexpected situations. The aim of the risk management is:

- To anticipate potential problems arising in the project before they can endanger its goals.
- To ensure that information about potential problems is readily made available to all necessary partners and only to those partners.
- To ensure that potential problems remain controlled in their appropriate instances and do not propagate to other project activities.
- To ease the process of taking corrective actions.
- To ensure the proposed actions do not interfere with other project actions.
- To ensure proper coordination between the different organisations in order to achieve maximum efficiency in the implementation of the corrective actions; i.e. to define clear rules and procedures for the persons and organisations participating in the corrective actions.
- To coordinate the availability of the necessary resources required for the proper implementation of the corrective actions.
- To ensure that the proposed corrective actions are implemented according to planning.
- To learn from past experience and to ensure this experience is adequately disseminated to other project instances and is adequately taken into account in the project planning.
2.2 Individual participants

CERN – European Organization for Nuclear Research

CERN is the world’s largest particle physics centre and is one of Europe’s first joint ventures (1954) for fundamental research and high-tech activities. Currently, around 6000 scientists from 500 institutes from all over the world are involved in the research and technology programme of CERN. In addition to the core programme of fundamental particle physics and its flag-ship mission of LHC, key R&D is performed in applied physics & engineering (including accelerator physics, accelerator and detector R&D) and Information Technology. CERN has experience in managing very large research infrastructures and expertise in leading large-scale collaborations involving many institutes from all over the world. CERN has participated in more than 60 projects under FP6 and FP7 and has coordinated more than 20 of those.

Main tasks and previous experience relevant to these tasks

CERN’s long history in running collaborative projects that are well supported by its financial and administrative services will help to fulfil its role as project coordinator (WP8). With its extensive know-how of developing and deploying large-scale timing and control networks in its accelerator complex, CERN will participate in the workpackages that define the required system architecture and specification (WP1, WP2), while with its experience in hardware and software development CERN will lead the design of the switch (WP4) and participate in the design of the node (WP5).

Profile of principal scientific and technical personnel

Javier Serrano is the Project Coordinator of the WhiteRabbit project. He received a masters degree in electrical engineering from the Institut National des Sciences Appliquées de Lyon in 1998 and a masters degree in physics from Université Claude Bernard Lyon I in the same year. He started working at CERN as an electronics designer in 1998 and since 2006 he is leading the controls Hardware and Timing section. This section specialises in the development of high-performance electronic modules with an emphasis on precise timing and currently employs 15 people including electronics designers, software engineers and PhD students. His research interests focus on high-performance building blocks for accurate phase shifting and measurement, phase noise of clocks, and cost-effective implementations in FPGAs. In addition he has launched the Open Hardware initiative to facilitate design reviews and reuse.

Erik van der Bij is the Project Manager of the White Rabbit project. He holds a masters degree in electronic engineering from the University of Twente. From 2002 until 2008 he managed a group of 40 staff containing a layout office, a detector development and PCB fabrication workshop, an assembly workshop and subcontracting services for the production of electronics for CERN’s detectors and accelerators. In this period the group had an annual turnover of 2.4 M€ and obtained a patent in the domain of particle detector fabrication. Erik has extensive experience with working with industry and technology transfer. With over 20 years of electronics design experience he has technically managed several collaborative projects with industry and physics institutes for the design of electronics for CERN’s experiments.

Julian Lewis has been working for 28 years on CERN’s timing and control systems and has been project leader for 15 years in this field. He currently is technical leader for device driver implementations. Julian has a degree in Maths and Physics from the Newcastle University and a Masters degree in Experimental Physics from the Newcastle Polytechnic.

Pablo Alvarez graduated in 2002 from the Polytechnic University of Valencia in Telecommunication Engineering with emphasis on Telecommunication Electronics. He works at CERN since 2000 and participated in the design of LHC’s timing system where he has obtained expertise in FPGA programming, systems synchronization and precise time transfer techniques.

Various students, fellows and staff members with a background in networking, computing and electronics will work on the project too, notably for the implementation of the switch.
AAS – Austrian Academy of Sciences

The Institute for Integrated Sensor Systems (IISS) of the Austrian Academy of Sciences was founded in 2004 and follows an interdisciplinary and integrative approach to the research and development of modern, integrated sensor systems. Integration in this context comprises functional, systemic and circuit design aspects. The institute combines three research teams with long-lasting experience in the areas of sensor technology, ASIC design and communication technology. The focus of the research is on biomedical, environmental, and automotive sensors, integrated scalable controllers and advanced signal processing techniques for limited computing resources, and networking issues for sensors including real-time and wireless aspects. In the area of sensor networks, particular emphasis is on security problems in large-scale ad-hoc networks with limited communication bandwidth and resource-limited nodes. Another topic is high-accuracy clock synchronization and related real-time aspects in distributed systems.

Main tasks and previous experience relevant to these tasks

The role of AAS within the White Rabbit project is to significantly contribute to the system simulation in WP3 as a work package leader. This is also the context for the integration into the validation work in WP6 where the simulation results are checked against the results of the physical validation. Besides these tasks AAS is involved in the system architecture and specification (WP1, WP2) in order to contribute their part to the analysis of the state of the art and the system definition.

Profile of principal scientific and technical personnel

Patrick Loschmidt received the Dipl.-Ing. degree in electrical engineering from the Vienna University of Technology, Vienna, Austria, in 2002. From 2001 to 2002, he was a research assistant at the Institute of Communication Networks, Vienna, working in the area of FPGA design for high-speed optical network nodes. Since 2004, he is with the IISS. Currently he is leading research projects in the area of network-based high-accuracy clock synchronization. Besides his main interest on hardware design, supporting software drivers and stacks are as well part of his daily work. Current activities focus on his PhD thesis dealing with enhanced clock synchronization performance through dedicated Ethernet hardware support.

Georg Gaderer received his master degrees in electrical engineering and informatics both with honours from Vienna University of Technology in 2002 and 2004, respectively. In 2008 he finished his PhD thesis. After finishing his studies in 2002, he became a research assistant at the Institute of Computer Technology, Vienna. During that time he did research for various industry projects focused on remote energy meter reading and clock synchronization in powerline networks. In 2005 he joined the IISS where he is currently head of the clock synchronization group, leading several clock synchronization related national and international research projects. Georg is coordinator of the FP7 ICT STREP flexWARE project, program co-chair of the ISPCS 2007 and 2009 conferences, and active member of the IEEE P1588 standardisation group. Moreover, he is part-time lecturer at the University of Applied Sciences FH-Campus Wien.

Nataša Simanić received the Dipl.-Ing. degree in 2008, from the Faculty of Technical Sciences, University of Novi Sad, Serbia, with a mainstream of her studies in the field of microcomputer electronics. She is with IISS since August 2008 and works in the area of network simulation and hardware design with special focus on implementing clock synchronization in Ethernet. The focus is on hardware designs for IEEE 1588 and appropriate simulation models for evaluation of large-scale systems.
GSI – Helmholtzzentrum für Schwerionenforschung GmbH

GSI operates a large accelerator facility for heavy-ion beams in Darmstadt, Germany and was founded in 1969. Its research program covers a broad range of activities from nuclear and atomic physics to plasma and materials research to biophysics and cancer therapy. It has a yearly budget of about 85 M€, 1050 employees including 300 scientist and is visited by over 1000 scientific facility users each year. GSI cooperates with about 400 institutes from 50 countries.

GSI has significant competence in the area of control systems and continually further develops its systems to meet current requirements. The Facility for Antiproton and Ion Research (FAIR) to be built at GSI bases on the experience and developments of the existing facility and has to incorporate new technological concepts, in particular for its control and timing distribution system. The Accelerator Electronics Department (AED) consists of 40 persons in the field of software and electronics engineering. The present real-time control system – that is developed in-house – operates more than 2500 individual devices using 270 interconnected device control processors.

Main tasks and previous experience relevant to these tasks

AED has proven experience in frontend hardware (FPGA/VHDL) development including PCB design, especially with respect to real-time requirements. Current developed frontend controllers interface e.g. radio-frequency cards via dedicated backplane buses and host function generators necessary to output frequency ramps with low jitter and sub-µs accuracy. Present AED developments on state-of-the art nodes run native Linux OS on COM Express modules interfaced by PCIe which is also the form factor to be delivered in WP5. AED’s IT department together with the general GSI IT department complement this with deep knowledge on distributed networks, protocol standards and management of different high-performance large-scale networks used for the accelerator itself or simulation environments. With its know-how on timing distribution and timing receivers GSI will lead WP5 (Node development) and will be strongly involved in WP4 (Switch design).

Profile of principal scientific and technical personnel

Tibor Fleck finished his PhD Thesis 2005 at the University of Karlsruhe on non-linear semiconductor optics and acquired knowledge on nanosecond time domain and simulation models. Since 2005 he is scientific research fellow at GSI’s Accelerator Electronics Department. Until 2008 he was the technical responsible for the control system at the new tumour therapy accelerator facility in Heidelberg and person in charge of its specification including all real-time aspects. He was also heavily involved in project management, risk assessment and the interface to the medical device. Since 2008 he is responsible for the timing distribution system for the new FAIR facility at GSI.

Mathias Kreider joined the hardware group of GSI’s Accelerator Electronics Department in February 2009. In 2008 he graduated from the University of Applied Sciences in Darmstadt in Electrical Engineering/Telecommunications with specialisation in data processing. During his studies, his work at the institute of graphical data processing concerned multi agent systems for negotiation purposes and their timing system. His diploma thesis was on real-time applications as part of the control interface for medical X-ray devices. His work at GSI consists of HDL design and FPGA implementation for the FAIR Timing System.

Cesar Prados completed his Electronic Engineer Master Degree 2006 at the University of Alcalá de Henares, Madrid. In 2006 and 2007 he developed research activities in the company “Ingegneria dei Sistemi, IDS” Italy, on Finite Element Methods in electromagnetic simulations. After that he worked as Electronic Engineer at Indra Company and as junior researcher at the University of Alcalá on Zigbee Technology and Wireless Sensor Networks. Since 2009 he is working on his PhD thesis about the FAIR timing system and develops VHDL code and driver software.
UniBS– University of Brescia

The research will be carried out by the Sensor and Electronic Instrumentation research group in the Wireless Sensor Networks Laboratory (WSNLab) of the Department of Electronics for the Automation (DEA), University of Brescia. Founded in 1982, DEA is involved in many research fields, from electronics, to telecommunications and informatics.

The group provides technical management of the Italian PROFIBUS and PROFINET Competence Center that is accredited by Profibus International and has several collaborations with industrial partners. It also actively participates in national and international committees for protocol standardisation like sub-committee MT9, WG16 and WG17 of the IEC SC65C (Industrial networks), and the WirelessHART consortium. UniBS has organised international conferences relevant to the White Rabbit project such as the ISPCS 2009 IEEE International Symposium on Precision Clock Synchronization for Measurement, Control and Communication.

Main tasks and previous experience relevant to these tasks

The current research topics of UniBS that are relevant to the project aims are: development of new protocols and communication systems based on Real-Time Ethernet and wireless technologies like WirelessHART, IEEE 802.15.4, and IEEE 802.11, development of measurement methods and distributed instrumentation for wired and wireless fieldbuses and sensors signal conditioning and processing.

The scientists involved in the project will be work package leader to the system concept and specification work package (WP2) and will contribute to the network simulations done in WP3. Furthermore the group will contribute to the implementation of the switch and provide input to the system architecture (WP1).

Profile of principal scientific and technical personnel

Alessandra Flammini after graduation in 1985, was employed in Ansaldo Industria, Milano, working in the research and development section of Motor Drives department. Since 1995, she has been a researcher in electronics and since 2002 she has been an associate professor of Electronic Measurements at the Faculty of Engineering of the University of Brescia. Since 2002 she is the responsible of the electronics laboratory and of the WSNLab. Since 2004 she is the head of the PROFIBUS and PROFINET laboratory. Her research activity mainly deals with: electronic instrumentation and digital processing of sensor signals; sensor networks and Real-Time Ethernet and wireless sensor networks based on different technologies. She is the author of more than 100 international papers (scientific journals and conference proceedings) and co-inventor of four patents.

Daniele Marioli is a full professor with the University of Brescia. He is responsible for the Sensor and Electronic Instrumentation research group and director of DEA. His research interests include the design, realisation, and test of sensors, instrumentation, signal processing circuits and embedded systems. He is the author of over 200 scientific papers.

Paolo Ferrari (PhD) is a full time researcher with the University of Brescia. His research activity deals with digital processing of sensor signals and sensor networking by means of embedded systems based on microcontrollers, DSP and FPGA. The most important activities are the realisation of instruments and algorithms for wired and wireless fieldbuses.

Emiliano Sisinni (PhD) is a full time researcher. His main research topic deals with the development and the performances analysis of industrial communication systems, with particular attention towards wireless fieldbuses. Further topics of interest are the standardisation process and real-time respect by means of network synchronization mechanisms.

Alessandro Depari (PhD) is a full time researcher. His main research topic deals with the development of new sensor interfaces for electronic noses. Recently, he has been involved in the design of new instruments for wireless sensor networks based on FPGA.
ZHAW – Zürcher Hochschule für Angewandte Wissenschaften

The Zürich University of Applied Sciences is a Swiss university founded on tradition, experience and success. It was inaugurated in September 2007 and represents the merger of four previously independent institutions: the Zürich University of Applied Sciences Wintertthur, the University of Applied Sciences Wädenswil, the School of Social Work and the School of Applied Psychology in Zürich. The ZHAW now comprises eight Schools. The School of Engineering is structured in institutes of which the Institute of Embedded Systems (InES) is one.

With a staff of around 40 persons, including 4 professors and lecturers directly involved in international research projects in the field ZHAW-InES is a recognised expert in the field of industrial communications and real-time Ethernet communications.

Main tasks and previous experience relevant to these tasks

ZHAW-InES has proven itself as an international competence centre for various industrial Ethernet orientated protocols including IEEE 1588 (PTP), PROFINET, POWERLINK and various high availability protocols such as PRP, HSR, and MRP. ZHAW-InES is competence centre for PROFINET since 2003 and owns a certification laboratory for POWERLINK.

With its experience in system design and industrial Ethernet the group at ZHAW will be work package leader of the system architecture work package (WP1) that will form the basis of the project. It will also ensure the standard compliance and interoperability addressed in WP2. Furthermore, ZHAW contributes with switch implementation work in WP4.

Profile of principal scientific and technical personnel

Hans Weibel is professor for communication technology at the ZHAW. He studied at the Swiss Federal Institute of Technology (ETH) in Zürich and worked for more than 20 years in the communication industry in different positions. Since 1999 he is lecturer, researcher and vice-head of the InES. His main R&D focus is on industrial communications, with emphasis on real-time and resilient Ethernet communications. He is active in different standardisation bodies such as in the IEEE 802.1 working group and acts as vice-chair of the IEEE 1588 working group. In the IEC committee he is expert in TC 65C.

Martin Renold received a Masters degree in Electrical Engineering and Information Technology from the ETH Zürich in 2008. He worked in the field of robotics at Neuronics AG for over a year, with focus on PID motion control. Since August 2009 he is working at the InES on IEEE 1588 clock synchronization and network redundancy protocols.

Fredi Gemperli received a Bachelor degree in Information Technology from the ZHAW in 2007. Since then he is member of staff at InES and has started a master study in 2008.
NI – National Instruments

National Instruments has over 5000 employees and develops modular off-the-shelf technologies for measurement, automation and embedded control applications. Specific products include Development Software (including graphical programming with LabVIEW, FPGA and real-time programming environments), Platforms (cRIO, cFP, PXI), and Modular Instrumentation. Notably, NI led the standardisation of PXI which enables Timing and Synchronization and other integration capabilities for a modular PCI or PCIe-based platform. Customers rely on the flexible integration of Development environments, Platforms and Modular vision, motion, DIO, precision, high speed instruments and bus interfaces using high-end PC technologies.

NI has a long history of leading and participating in standards including IVI, IEEE 488, HS488, PXI, VXI, IEEE1588, VISA and others. NI’s customers are very diverse with no single industry making up more than 10% of revenue. This allows for an expertise in applying technology to satisfy multiple markets’ requirements.

Main tasks and previous experience relevant to these tasks

The background and technical expertise of NI will help provide perspective during the specification of the White Rabbit platform in work packages 1 and 2. NI’s history and capabilities in marketing modular technologies across multiple industries will be a major contribution to work package 7 which seeks to disseminate and ensure adoption of the White Rabbit technology.

Profile of principal scientific and technical personnel

Adam Ullrich has a Bachelors in Electrical Engineering. With a background as a Project Engineer at Advanced Micro Devices, he is the Timing and Synchronization Group Manager at National Instruments where he has worked since 2003. NI’s Timing and Synchronization group drives technologies and strategies enabling tight timing integration across NI’s products and platforms. Implementations leverage advanced software, specialised data bus interfaces, FPGA, and precise clock generation technology. The group has used technologies including GPS, IEEE 1588, IRIG and others to enable these systems in both closely and widely-distributed systems.

Rodney Greenstreet is the Technical Lead of the Timing and Synchronization group at National Instruments. He started working at National Instruments in 1992 in the GPIB Hardware group where he implemented the firmware for NI’s first USB device and designed the first CompactPCI board which served as an impetus to the PXI platform. In 2000 he transitioned into a software development role where he led a group of engineers in the creation of a device side software Application Programming Interface that abstracts the communication bus from device-specific firmware, allowing the preservation of firmware investments when adding additional communication buses. This product is used in Test and Measurement devices such as Tektronix’s instruments. In 2006, he transitioned into the Timing and Synchronization group as Technical Lead.
COSY – COSYLAB d.d.

Cosylab is one of the leading companies for the development and implementation of challenging computer-based control systems worldwide and is partnering with corporations such as Siemens, Varian, Thales, Clemessy, Astrium (EADS), Atos Origin and National Instruments. Cosylab is a global market leader in the field of control systems for large experimental physics facilities, e.g., particle accelerators, synchrotron light sources, experimental fusion reactors, and radio telescopes. Cosylab’s customers are approximately 30 of the world’s largest and most well-known projects and include particle accelerators in Europe, the USA, Japan, Taiwan, and Australia. Cosylab is a spin-off of Slovenia’s largest research institute, the Jožef Stefan Institute. Through high-quality work in large accelerator labs, Cosylab became a market leader specialising in solutions from system engineering, custom development services of software and hardware, to turn-key control systems.

Main tasks and previous experience relevant to these tasks

Through consulting projects for CERN, GSI, ITER, and Oak Ridge National Laboratories (ORNL), Cosylab has gained understanding of requirements and detailed knowledge of the architecture of timing systems in large experimental physics facilities, which it will contribute to WP1. Cosylab also has extensive experience designing and verifying FPGA-based embedded systems using approaches such as software-hardware co-design and tools such as SystemC.

With the FP6 project “Dependable Distributed Systems” (DeDiSys) Cosylab already demonstrated its capability to lead a work package. In this project Cosylab will lead the validation work package (WP6) and will be complemented by AAS and Hirschmann in this task. Furthermore Cosylab will contribute to the simulations done in WP3. With its experience in implementing embedded systems Cosylab will contribute significant resources to WP5, the node development.

Profile of principal scientific and technical personnel

Jože Dedič is the lead engineer of hardware and electronics development at Cosylab. Apart from managing a team of 5 engineers, Jože is also a product manager in charge of Cosylab’s microIOC family of products. Jože has extensive experience in project-based system-level integration and development, embedded system integration, and electronic printed board design. He has detailed knowledge of operation of particle accelerators gained through experience on sites in Europe and USA. One of his most recent projects was the redesign of the accelerator timing system master for the Spallation Neutron Source, located at ORNL. Jože has a PhD in electronics.

Mark Pleško has over 25 years of experiences with software development and has worked with internet technologies for 20 years. Originally programming physics applications and control systems for nuclear accelerators, he now acts among others as a project manager and system analyst for distributed computing systems for such diverse fields as nuclear accelerators, radio telescopes, automotive electronics, embedded systems, architecture databases, and geographical information systems. Mark is a technology visionary, having introduced into his teams relational databases in the early eighties, distributed computing in 1989, Java in 1996 and WebServices in 2001. Mark has led projects in sizes up to 20 person-years for customers all over Europe, the USA, and Japan. Mark has a PhD in physics and an MBA degree.

Klemen Žagar is a senior systems architect and requirements analyst at Cosylab. As a member of the team since 1999, Klemen has gained experience through projects such as defining the architecture of the Atacama Large Millimeter Array’s control system, leading work packages in the DeDiSys project and consulting to ITER on high-performance networks. Klemen has a BSc degree in physics and is pursuing a PhD degree in computer science.

Rok Tavčar is a skilled developer of embedded systems for control and automation. Among his projects are implementation of heating, ventilation and air-conditioning system for hospitals, and regulation of chemical processes for the oil industry. Rok has a BSc degree in electronics.
ORE - Oregano Systems - Design & Consulting GmbH

Oregano Systems Design & Consulting was founded in 2001 as a spin-off from the Vienna University of Technology. Its main areas of business and expertise lie in the design of digital and mixed-signal custom integrated circuits and embedded systems. Oregano Systems offers design services to customers both in Austria and on an international basis, focusing its business primarily on telecom and industrial electronics and on control and automation applications. Oregano Systems offers a complete set of services ranging from system specification down to the complete design and series production of embedded systems. In the latter case Oregano Systems not only takes care of sub-contracting of assembly plants and semiconductor distributors, but is responsible for the production testing as well.

In close co-operation with the Vienna University of Technology, the University of Applied Sciences Technikum Wien and with the Institute for Integrated Sensor Systems of the Austrian Academy of Sciences, Oregano has developed both the underlying technology and a set of IP cores for extremely accurate clock synchronization via high speed Ethernet (100 & 1000 Mbps) following the IEEE 1588 standard. Oregano Systems is a member of the IEEE 1588 standardisation committee. Aside from IP cores that are bundled with the required drivers and software stacks, Oregano Systems offers several demonstration and evaluation systems for enabling customers to build clock synchronization systems that are highly accurate and fault tolerant.

Main tasks and previous experience relevant to these tasks

Within the White Rabbit project Oregano Systems will focus on enhancing its technology to sub-nanosecond accuracy within large-scale networks with special emphasis on network components like transparent clocks. Extremely high resolution timestamping methods suited for implementation into FPGAs of various vendors shall be investigated in detail. Furthermore, mixed analog and digital servo loops for the end nodes which are required to achieve the goals of the project, will be analysed as well.

The contribution of Oregano Systems to White Rabbit can be seen in the specification and architecture of the clock synchronization in WP1 and WP2. Furthermore, the involved researchers of Oregano Systems will contribute to WP4 and WP5 (timing platform implementation and IP core development, respectively).

Profile of principal scientific and technical personnel

Nikolaus Kerö received his master degree in communication engineering in 1984. Since then he worked at the Vienna University of Technology as a research assistant. Starting from the mid 1990-ies he led the ASIC design division at the Institute of Industrial Electronics and Material Science and later on at the Institute of Computer Technology with up to 10 design engineers. He was responsible for a significant number of research and industry related projects during this time. Together with colleagues he founded Oregano Systems in 2001. His research interests are mixed signal ASIC design for telecom, industrial automation, and automotive electronics. Within Oregano Systems he is responsible for the clock synchronization activities both with respect to research and development and marketing.

Hannes Muhr holds a master degree in Electrical Engineering and a PhD in Computer Technology from the Vienna University of Technology. From 2001 on he was Research assistant at the Institute of Computer Technology (TU Wien) and worked in various industrial and research projects in the areas of computer aided design. Mr. Muhr joined Oregano Systems in 2003 conducting various projects of hardware/software co-design, simulation and embedded system implementation.
HAC – Hirschmann Automation and Control GmbH

As a specialist in automation and networking systems, Hirschmann Automation and Control offers a complete, integrated structure for data communication in companies. Since 2007 Hirschmann belongs to the US-American company Belden Inc. Belden is a leader in the design, manufacture, and marketing of signal transmission products for data networking and a wide range of specialty electronics markets including entertainment, industrial, security and aerospace applications.

The product range extends from network components and fibre interfaces for different field bus systems through electrical actuator and sensor connectors to systems for load indication and load moment limitation for cranes and various other mobile applications.

Main tasks and previous experience relevant to these tasks

Hirschmann is working in the field of Ethernet networking since 25 years and is one of the pioneers in Industrial Ethernet applications. By actively working in several groups of IEEE and IEC, Hirschmann made significant contributions to Real-Time Ethernet protocols, precise time synchronization and high-availability communication networks.

Hirschmann contributes to the project in WP1 (state of the art analysis, architecture) and WP2 (concept and specification) with a special focus on standards compliance and fault tolerance. Furthermore Hirschmann commits resources in the platform development and the test of White Rabbit (WP 4 and WP6).

Profile of principal scientific and technical personnel

Andreas Dreher received his master degree in Electrical Engineering in 1987 from the University of Stuttgart (Germany). He joined Hirschmann in 1989 and worked in several positions in R&D management for communication networks. Since 2006 he is responsible for strategic technology management, research projects and new technologies. His main focus is on industrial communications, including time synchronization, real-time systems, highly available networks and switching architectures.

Oliver Kleineberg holds a degree in computer engineering from the University of Applied Science in Esslingen (Germany). He has detailed knowledge in software engineering, communication protocols and system theory.
2.3 Consortium as a whole

The White Rabbit project requires a great variety of talents for its success, so great care has been taken in the selection of the most appropriate partners to form a high-performance balanced team. Broadly speaking, the project needs:

- Good academic partners who can study the problem of timing accuracy and determinism, and propose an optimal solution based on network theory, the best analysis tools and state-of-the-art current practice.

- Experienced system designers with an overview of the technical solution space and the skills needed to partition the complete system into manageable pieces, specify each of the parts and monitor their progress while ensuring overall coherency.

- A team of bright hardware designers to implement the chosen solutions in a modern platform, mastering subjects such as low noise design, high speed differential signalling, firmware and gateware.

- Commercial companies whose task is to focus the project on deliverables which are actually needed by society, to make sure the designs can be efficiently manufactured and tested in an industrial setting and to help in the dissemination of the technology.

In order to form a successful team, each partner must at least provide one of these skills to the project. While each of the partners has a speciality, all of them bring in this project at least two such talents, easing communication among partners and giving an additional degree of flexibility to the project management team.

On the academic front, ZHAW has a well established reputation as a centre of excellence in networking technologies in general and protocol specifications in particular, with members actively involved in standardization bodies. It is therefore a perfect institution to manage WP1, where the place of White Rabbit in the landscape of networking solutions is fixed and an overall system architecture is proposed. In addition, ZHAW’s engineers have experience in designing complete networking solutions in collaboration with industry. This guarantees that real-life considerations such as cost/performance trade-offs and manufacturability will be taken very seriously from the outset of the project.

Complementing ZHAW on the academic side of the partnership we have UniBS, which brings to the project a very interesting blend of theoretical knowledge and applications of real-time networks for distributed sensors. UniBS will coordinate WP2, which is the heart of the White Rabbit project. Their experience with distributed sensor networks will be a very important reality check for the concepts developed in WP1 and WP2 and their strict scientific approach to design will be a key asset for the project in general and WP2 in particular. The fact that UniBS has organised the most important international conference on network synchronization in 2009 (ISPCS), speaks about the importance timing is taking in distributed applications and is completely in line with the overall philosophy of the project.

Halfway between academic and applied partners we have AAS, which has since a long time identified the key role of synchronization in sensor networks, and has extensive experience in the current state-of-the-art techniques. This mastership is certified by their development of very precise PTP nodes, breaking world records in accuracy. In addition, AAS is specialised in complex network simulation and this experience will be a great start for their work coordinating WP3. The hardware design background of some of the members of the AAS group will ensure that simulation and reality match as closely as possible and that WP6 benefits from the simulation results in an efficient way.

The consortium stems out of an original idea developed at CERN, which is a privileged place to get trained in the management of big and complex projects. Some of the members of the
CERN group have experienced this first-hand and will contribute these skills to the project in WP8. In addition, CERN has a very wide view of the application space in the domain of large scientific installations. Finally, being in the middle of a campus where hundreds of electronics designers develop the hardware of current and future accelerators, the CERN team is very well equipped for hosting hardware design and development work such as that specified in WP4.

GSI is another large scientific institution with a challenging design task ahead. The GSI team brings in a formal approach to design and development tasks learned in past experiences concerning highly critical medical applications. GSI is also a hub of hardware design activity for the FAIR project and as such it is well placed to coordinate WP5. In addition, their long-standing collaboration with Cosylab will ensure that WP5 and WP6 run together smoothly.

The four commercial companies in the consortium include small enterprises and large corporations, with different backgrounds and interests. Cosylab has extensive experience in collaborating with many scientific facilities around the world in the design and development of distributed control systems. They bring into the project software and hardware development expertise at all levels plus a detailed knowledge of the needs of all their customers. Their broad knowledge on state-of-the-art control systems has been acknowledged by organisations such as ITER which mandated Cosylab to conduct a survey of available technologies to fulfil its control system needs. Part of these surveys is demonstrating performance through a test bed and Cosylab’s experience in this domain makes it an ideal candidate to coordinate WP6.

Oregano is the other SME in the consortium and their focus is mainly on IP core design and development for network synchronization applications. Their skills are very complementary to those of AAS as their long-time partnership confirms. In addition to covering the high-tech design skills needed for this task, as a commercial company they must add a deep concern for manufacturability, ergonomics, and optimal price/performance ratio.

NI is one of the world leaders in distributed instrumentation and will bring in hardware design knowledge and a large dissemination effort. Its large customer base and its involvement in many different distributed networking scenarios make NI the most appropriate coordinator for WP7.

The other large corporation in the consortium is Hirschmann, one of the leaders in applications of Ethernet to industrial automation. They bring into the project a large experience in the design of real-life complex networks and will focus on robustness and reliability as required in harsh industrial environments. Consequently all of the partners have the required knowledge and resources to perform the work assigned and therefore none will subcontract any of the work.

The consortium described above has its members based in EU Member states or Associated countries. Together they represent a balanced mix of skills in order to tackle the problem that the White Rabbit project has set out to solve: enabling complex large-scale Ethernet networks with the capability of synchronizing nodes precisely and guaranteeing safe and timely delivery of messages in a transparent way. This requires a large knowledge of all existing solutions in the complex networking technologies landscape, and the majority of the partners in the consortium have extensive experience in the design and development of networking solutions. The hardware development part of the project is limited to actually proving that the developed concepts indeed work and agree with simulation results and therefore represents a smaller share in the overall effort. However, if this technology is to meet wide adoption in industry and academia, we need strong commercial partners to be closely involved from the beginning, giving feedback early in the design stage and trying out hardware in laboratories to ascertain that White Rabbit has met its objectives. This is the reason to have a strong commercial partner component in the project.

As a reality check for the balance of the consortium and for the complementarity among its members, let’s see for example the individual impacts of each member on one of the key deliverables of the project: the White Rabbit switch.
ZHAW will give a place to the switch in the overall scheme, specifying its role in the propagation of synchronization and in the transmission of data.

UniBS will deliver the functional specification of the switch, i.e. a clear definition of all its interfaces to the outside world as well as a summary description of its inner workings.

AAS will deliver accurate network simulations based on a detailed model of the switch, establishing whether it fulfils the specifications in terms of latency, throughput and determinism.

CERN and GSI will design the switch with the help of Hirschmann and Oregano in aspects related to making it a commercial product, optimising its price/performance ratio and making sure it targets a wide range of applications.

Cosylab will test the switch extensively in the test bed and correlate the results with those of the AAS simulation.

NI will use it to synchronize distributed systems based on their PXI platform and will promote it through its extensive commercial network and its presence in multiple forums, shows and conferences.

In conclusion, the membership of the consortium has been taken very seriously in this project, and we believe that the proposed project team is not only capable of meeting all the project goals but also to do so in a well-structured and balanced way.
2.4 Resources to be committed

While the total cost is estimated to be 2858 k€, the requested funding for the project is 2093 k€. The funding will mainly be used for personnel costs for research and development. Only a small representative system that will cost less than 2% of the funding will be made to verify the actual functioning of the concepts. It is the goal of the consortium to use as much pre-existing knowledge and development equipment as possible in order to keep the project costs low.

Architectural specification / System Concept. The period to the first milestone is used to define the requirements and start off the project. Consequently, all partners are involved to participate in this conceptual phase and there will be a combined technical and management meeting which will require an estimated total cost of 12 k€ for travelling. A second purely technical meeting will be required in order to finish up the system concept for the second milestone of the project. This will require a second meeting costing 10 k€. It is foreseen that this meeting will coincide with a required Full Project Meeting.

Implementation. The hardware developed will be used to verify the actual functioning of the concepts, will provide real data as input to the system simulation (WP3) and will give a strongly visible output to the project that will ease the dissemination efforts of WP7. The result of pre-studies showing the feasibility will be contributed to the kick-off of the project.

It is foreseen to build two small test systems, each consisting of three switches and ten nodes at two different partners (CERN and GSI). A 75% EU contribution of the cost of 22 k€ for only one of these system is requested. The second system, the one-time development, and prototyping costs for the switch and nodes will be paid for by the partners CERN and GSI on their proper funding (these fixed costs are estimated at at around 46 k€ in total).

Two one-month collaboration visits of two engineers from GSI to CERN are foreseen. This ensures the tight collaboration between the largest contributing partners and for a more profound education of these engineers. The cost for this is 8 k€/month including all daily allowances compliant with FP7 guidelines for stays in Switzerland.

To complement the EU-assisted White Rabbit project, CERN and GSI will invest further in-kind resources into the deployment of the system into existing and upcoming accelerator projects at their sites. This will require the development of other form factors, a higher volume of nodes and the contribution to the industrialisation of the equipment. Additionally, the large industrial partner NI plans to totally fund the design of a White Rabbit implementation for PXI, the highest performance timing platform for these modular instrument applications. NI believes that support on the PXI platform is critical for broad industry adoption.

Simulation / Validation. For simulation, the required software is already available at the involved partners. They will provide the required simulation tools such as OMNe+++, Matlab, and LabView and the computing infrastructure for running the initial evaluations. In order to demonstrate the features for the large scale, additional state-of-the-art hardware will be required since the experience from currently ongoing projects already showed limitations to the existing infrastructure. The massive parallel computing necessary for thousands of nodes will require dedicated simulation servers (∼10 k€) in order to allow for realistic node models to be comparable to the measured input parameters from WP6 (Validation).

The latter includes the full modelling of the test system, integration of the test bed, execution and assessments of the results. For final small-scale gathering of simulation parameters for verification, the different test systems will be grouped together, for which transport and insurance is needed, estimated at 4 k€ for the two-way transport. Also a travel budget is foreseen of 6 k€.

Dissemination and exploitation. For dissemination purposes the partners involved in work package 7 will each spend between one and four person-months over the project duration for producing information material for use on the project web site, for conferences and fairs. This
totals 20 person-months. NI as leader of the dissemination work package (WP7) will also focus its management and marketing engineering resources on the dissemination and exploitation of White Rabbit. NI anticipates to invest more effort in this area than the four person-months for which a 50% EU funding is requested. This will help fund the creation of materials and attendance to industry conferences where White Rabbit may be applicable. Efficient White Rabbit dissemination will be supported and magnified at those conferences where NI already funds a company presence in the form of booths, floor space and sponsorship at a much higher expense.

**Management.** The plan for managing the project as described in section 2.1 is designed to minimise the management costs and provide maximum efficiency in research and development. In order to provide appropriate feedback to the European Commission, the costs include two audits for the partners that exceed the audit limit, making up a cost of 6 k€ in total. As CERN provides the Project Manager and Project Coordinator it requests an EU contribution for 6 person-months. The direct costs for management and dissemination foresees three travels per partner organisation over the project duration estimated at 36 k€.

**Complementary equipment and software provided by the consortium.** The consortium will contribute all the required equipment for performance evaluation. This expensive high-end laboratory equipment includes a high bandwidth (4 GS/s) digitiser with jitter analysis features, a 20 GS/s oscilloscope, a time interval meter with picosecond resolution and an Agilent E5052B phase noise analyser with jitter measurement capabilities in the femtosecond region. Moreover, the partners own very stable frequency sources, including Caesium clocks and several Rubidium-based GPS receivers and have a whole range of RF instruments available, including spectrum and network analysers as well as the necessary environment (laboratories, climate chamber, etc.) to set up appropriate measurements. **There is no request for an EU contribution to any measurement or development equipment.**

Concerning prototype development, the project can use the long experience of the involved partners in the bring-up of leading edge technology. Besides the required hardware tools, the consortium also has access to state-of-the-art hardware development tools, like the necessary software for hardware development with FPGAs from the vendors Altera, Xilinx, and Actel. Additionally, the software products from Mentor Graphics and others allow the simulation of hardware design in early stage to reduce development time. The use of Synplicity Synplify for synthesis of designs is enabled by licenses owned by some of the partners, thus allowing netlist generation for FPGA implementation from the same basis.

The necessary resources for software development will also be provided. The consortium provides experience in developing low-level software like device drivers in Linux. The necessary compilers and IDEs for programming and testing software under Linux or Windows to be developed are also available among the partners. Concluding, there will be no necessity for purchasing any software products for the project.

**Commitment to provide additional resources.** In addition to the budget described above it is important to note that the objectives of the project require significantly higher resources than shown by way of person-months and associated costs in this proposal. Therefore, the consortium, and in particular CERN, AAS, and GSI, are committing themselves to providing additional human resources and material budget in order to achieve the deliverables described in this proposal.
3 Impact

3.1 Expected impacts listed in the work programme

The White Rabbit project’s results are expected to contribute to the impact of the EU FP7 Call ICT-2009.3.5, Engineering of Networked Monitoring and Control systems:

*Strengthened competitiveness of the industry supplying monitoring and control systems through next generation process automation products that are superior in terms of functionality, accuracy, dynamic range, autonomy, reliability and resilience.*

The major impact of the White Rabbit project comes from the collaborative and demand-driven nature of the goal to control a large-scale system. The research on such a highly complex system and the foreseen integration with probably the most complex machinery ever built will strengthen the competitiveness of the industrial partners by the aggregation of know-how in this area.

To the best knowledge of the consortium the state of the art of today’s large-scale control solutions does not provide the capability as described in this proposal. The advantages beyond the state of the art and commercially available products can be divided into four categories:

- **Functional efficiency.** As White Rabbit eases the possibilities for new services, the foreseen timing information of all nodes within the network can be used for efficiency optimisation of network scheduling and real-time planning. Currently no solutions exist, which place monitoring points in distributed processes exactly where they are needed. The efficiency of the processes themselves can be increased by dynamic adjustable process optimisation.

- **Flexible dynamic adaptivity.** As flexible wired technology is the enabler for large-scale networked control, the project will have an important impact on this issue. Currently, industrial networks are far from being fully deployed in terms of research and commercial products. White Rabbit concentrates exactly on that flexibility, easing the possibility for nodes which are dynamically attached to the network at run-time. The project will therefore have a major influence on upcoming research in this area and synergy effects on other research projects and the medium term evolution after the end of the project.

- **Robustness, reliability and resilience.** As fault tolerance via wired technologies is one of the goals of the White Rabbit project, these issues will be tackled in terms of decreased downtimes and simplified repair and installation procedures. With this and the foreseen improved fault tolerance, the intended system will increase productivity with a high reliability from the beginning. Moreover, maintenance is simplified in terms of novel user-friendly possibilities as no power-up or central re-engineering of a network configuration is mandatory. This simplified access to data and additional services, like the flexibility to control and monitor components throughout the whole factory or plant, increases productivity and reduces maintenance effort.

- **Dynamic industrial backbone networks.** As with the change from direct wiring to fieldbuses or the change from field busses to industrial Ethernet a trend towards wireless automation networks is noticeable. The ARC advisory group expects growth rates of 51.4% for this market segment. The development of industrial wireless networks is being investigated by many market participants. This trend however, will not end the requirement for wired industrial communication. All of these networks need a high performance backbone to which the access points are connected. The knowledge gained within the White Rabbit project will be a benefit for the competitiveness of the stakeholders involved in the preparation for any switch-over to wireless technologies.
• **New functionalities for tomorrow’s large-scale networks.** The trends point towards a new generation of networked embedded systems made up of thousands, or even millions, of tiny computing devices interacting with the environment and each other in a network-organised way. Hiding this complexity while enabling this interaction and offering an open interface to application developers is major goal. The need for an infrastructure offering robust, secure and real-time connection services to these devices is becoming crucial in many contexts; e.g. sensor networks, fast reconfigurable real-time networks or context aware computing.

European manufacturers of time-aware network devices and protocol stacks will benefit directly from the findings and results of White Rabbit, allowing them to build competitive network devices and IP-cores.

*Higher energy efficiency and reduction of waste and of resource use in manufacturing and processing plants; improved ease-of-use and simplified operation and maintenance of monitoring and control systems, also for non-experts; and more effective management systems for natural resources and the environment.*

• **Energy efficiency.** White Rabbit enables improved energy efficiency by facilitating the sharing of non-real-time and clock synchronization networks, reducing the power demands of the overall network infrastructure. Though small compared to the energy demands of an entire facility, in absolute terms the savings can be considerable as timing solutions typically involve thousands of nodes and hundreds of kilometres of cabling.

Unlike existing custom timing solutions, White Rabbit will impose fewer restrictions on the contents of the real-time messages. This will allow designers to pass additional real-time data, allowing for improved control of processes. Given the large power requirements of huge experimental physics facilities, even a small relative saving would be significant in absolute terms.

• **New capabilities for energy aware environmental management.** One of the most obvious problems in efficiency management is that it is mandatory to monitor natural resources in a spatially distributed manner. For example, exact monitoring of environmental parameters is limited by the distribution of proper sensors. The data collection network has also to fulfil the task of an easy to use and large-scale monitoring infrastructure. The approach chosen in White Rabbit will fulfil this requirement by the capability to dynamically extend such networks and the plug and play character for the addressed layer 2.

Also the possibility for real-time monitoring can improve certain use-cases such as water quality monitoring.

• Finally, having cheap sensing and actuating capabilities virtually everywhere within processing and manufacturing plants is the starting point for a more detailed energy optimisation than is currently technically and economically possible. This is especially true for the use of White Rabbit in conjunction with wireless technologies as the “last mile”.

*Reinforced European inter-disciplinary excellence in control and systems engineering and associated modelling and simulation tools as well as in real-time computing, communications, wireless sensor (and actuator) networks and cooperating objects.*

• The primary focus of the White Rabbit project is real-time communication. In this field, the project will bring together partners from industry and leading research institutes, providing a potential to consolidate and commercialise expertise in the field, as well as allowing the sharing and improving of modelling and simulation approaches. This can be also seen in the necessity for a European approach for White Rabbit due to the needed
critical mass to carry out such a large project and since one of the expected impact and dissemination plans is standardisation. This is needed as the European market for process automation has a large common base of technical and economical requirements that is reflected in legislation and standards. The partners are from a wide range of member states who can provide input from both a European and an international perspective.

- The industrial partners will be closely involved in the project so that they gain detailed knowledge and understanding of the White Rabbit platform in order to be able to exploit and commercialise the results. To this end, industrial partners participate in most work packages of the project (see section 1.3). Also, the White Rabbit platform will be adequately marketed to the target users (e.g., designers of control algorithms), as well as to staff at other experimental facilities.

Of the external influences on the impact, the biggest one is probably the long term use of the results. The industrial partners can re-use the knowledge gained in the project, but the current economic situation and cuts to research budgets could reduce the expected impact. This risk is however minimised by the guaranteed scientific dissemination of the results and know-how. Finally, in this period, the industrial partners are very motivated to strengthen their competitiveness with innovative products that will result out of this project.
3.2 Dissemination and/or exploitation of project results, and management of intellectual property

Dissemination strategy

Dissemination activities are planned throughout the duration of the project. The means of dissemination will be those already used by each member, plus others particular to the consortium; they are digital media and conventional media. By digital media we mean all actions that use the Internet as a communication medium. By conventional media we mean all actions that take place using traditional platforms like journals and fairs. The targets identified are the scientific community and technical industries, although, as the project evolves, the consortium will learn more about the applicability of White Rabbit to other target areas.

The project website will play a central role. The website will offer two well integrated, but distinct, facets with the aim of covering all the information needed in the technical domain. One facet will be focused on communication and the other is intended to host, organise, and showcase the technical material generated in the project; the so-called Open Hardware Repository (OHR). Technical material will be protected under an open license scheme and development specifications will be published, at the latest, by the end of the project. The project website will contain information for interested companies, research institutes and the general public and will supply information on the goals, progress, achievements, demonstrations, and promotional material. As a way of disseminating technical and commercial information related to the project, the website will provide, via subscription, a free e-seminar and a newsletter (available quarterly) to those interested in the project. The project undertakes to establish a dynamic, lively, up-to-date website supported by the project partners which will provide a united view of the project.

In order to announce the project and its website, it is planned to distribute press releases and articles via first-rate on-line publications such as “EE Times” and “EDN: Electronics Design, Strategy, News”. Conventional media activities will include raising public awareness of the project via traditional press releases (at least at the launch and at the end of the project) and will target magazines such as Elektronik I Norden (Sweden), Automatik (Denmark), Elektronikk (Norway), PROSESSORI (Finland), Automation Magazine (France/Belgium), Conectronic (Spain), and Elektronik (Germany). Individual partners will also participate in scientific fairs such as Elektronika, Embedded World, SPS-Messe, GSMA, Embedded System Conference and the Hannover Fair and will disseminate the project concepts and developments. For the detailed activities, the consortium plans to use the existing contacts of the respective PR departments.

Two workshops will be organised to coincide with the annual project meetings. These workshops will be the occasion to encourage the participation of other companies and institutes, to spread the awareness of White Rabbit and gather feedback. Participation in these workshops will be heavily promoted using the website and newsletters. The project will use an open license scheme, such as the Open Hardware License (OHL) [27], for any hardware produced. This can be a powerful tool for dissemination as the hardware designs will be freely available to a large community which would not be the case if the designs were proprietary.

Another opportunity for dissemination is the possibility of a future standardisation, the highest aspiration of a newborn technology since it spreads the technology more easily, triggers new refinements and improves costs effectiveness and integration. The standardisation process is out of the scope of this project, due to the time and resources needed to deal with such a task, but the consortium intends to establish the basis for a future standardisation process using standard protocols like IEEE 1588 and following abstract description schemes like the OSI model.

In addition to the general dissemination strategy described above, individual dissemination efforts will be carried out by the members of the consortium within their own sphere of influence.
Individual dissemination plans

All partners of the consortium will follow individual dissemination plans. This is important as the structure of the consortium needs also these complementary dissemination paths in order to maximise the result of White Rabbit.

NI. National Instruments is a recognised leader in applying timing technologies across multiple industries. As experts in using the PXI platform to time and synchronize systems using COTS modules, NI – who leads the Dissemination and Exploitation work package – is well positioned to present White Rabbit across multiple industries and events. NI’s proficiency in marketing technologies to diverse industries and its large worldwide sales, marketing and engineering presence will be central in disseminating White Rabbit and ensuring its adoption and success.

In addition to conferences and custom presentations on the applications of the technology, NI uses direct customer marketing material, customer visits and online materials.

CERN. CERN’s contribution to the dissemination effort will consist in presenting White Rabbit in the scientific community working in particle accelerator controls. In addition, CERN will use existing collaborations as a basis for dissemination:

- The MedAustron project for a Hadron Therapy accelerator to be built in Austria has requirements for a high-speed, fully deterministic network which could be completely fulfilled by White Rabbit. Therefore, it could become an essential part of one of the most modern Hadron Therapy facilities in Europe and may be used for other facilities of this type.

- The ITER project aims to build and operate the first large-scale fusion reactor. The ITER project is in the specifications stage and data networks needed to operate the facility have been described in abstract terms. Preliminary studies have shown that White Rabbit will be the only network technology to comply with the requirements of all data networks needed in the ITER control system, therefore enabling a complete networking solution based on only one technology.

CERN is also very active within the community of large physics facilities and White Rabbit would be a very good candidate for many facilities with which CERN has long-established contacts. Some examples include orbit feedback systems in Synchrotron Light Sources, timing systems for Free Electron Lasers, synchronization of distributed sensors in radio telescope arrays and gravitational waves experiments. To help in this dissemination effort, CERN will be able to use its in-house Knowledge and Technology Transfer service.

AAS. The Institute for Integrated Sensor Systems (IISS) of the Austrian Academy of Sciences is well established in the communities of sensor design, wireless networks and clock synchronization. Dissemination activities will not only include publishing of scientific results at conferences, but also spreading the ideas and the technology among cooperating industrial partners. The MedAustron project, mentioned above, is an obvious candidate since IISS is part of the same Technopol (local cooperation of companies and research institutions in Lower Austria). Furthermore, IISS is located in the same building as the MedAustron company, which is very close to the construction site. AAS can therefore very conveniently support the dissemination of the White Rabbit within MedAustron.

As one of the major goals of AAS is the engagement in basic research, IISS will aim for dissemination in the form of at least two PhD thesis. This will include the employment of young doctoral students. IISS is heavily involved in the promotion of science to young people, before they start their studies, by providing summer jobs and internships. Usually, around four internships are given per year to motivate young people to study technical sciences. Additionally,
IISS will publicise the project at large popular scientific events, like the “Austrian Long Night of Science”, where research institutions present their work to the public from sunset to midnight. This event is especially important for demonstrating high-quality technical research in a vivid way by simplified demonstrations. The visitors have the chance to talk directly to the people involved who are best placed to explain the details of their research goal and results.

**GSI.** GSI’s contribution to the dissemination effort will consist mainly in presenting White Rabbit in symposiums related to particle accelerator controls. A new international particle accelerator facility, FAIR (Facility for Antiproton and Ion Research), will be built at GSI. FAIR partners comes from 13 countries (Austria, Finland, France, Germany, India, Italy, Romania, Russia, Slovenia, Sweden, United Kingdom, Spain and Poland). White Rabbit will be made known to FAIR partners by technical meetings and reports, specifications, design documents, and interface descriptions. Public awareness of White Rabbit will happen through the strong dissemination and PR strategy that FAIR has already implemented. GSI, like CERN, is also very active in the community of large physics facilities.

White Rabbit is a promising candidate for timing systems in physics experiments at accelerators or other facilities with which GSI has long-established contacts and close relations. At GSI, NUSTAR (a collaboration of the international nuclear structure and astrophysics community) has already expressed interest in White Rabbit.

**UniBS.** UniBS will disseminate the results obtained from the White Rabbit project to the scientific communities of industrial automation, industrial communication, and network synchronization. Additionally, seminars on White Rabbit will be organised within their PhD courses. Participation in the national and international committees (CEI, IEC) concerned with industrial communication technology will give the possibility to enlarge the scope of the current standards with the new concepts coming from the White Rabbit project.

**ZHAW.** ZHAW’s contribution to the dissemination effort will consist of presenting White Rabbit at conferences and workshops related to real-time Ethernet for industrial applications such as automation, data acquisition, test and measurement, navigation, etc. The active role of ZHAW’s staff in standardisation bodies allows them to check the opportunities for standardisation of the White Rabbit technology or parts of it.

**Hirschmann.** Hirschmann plans to present White Rabbit on conferences, in trade publications in the area of industrial automation, and on trade fairs where Hirschmann typically demonstrates and showcases its products (e.g. SPS/IPC/Drives Fair, etc.). In addition, Hirschmann will include White Rabbit into its marketing activities for industrial automation markets.

**Cosylab.** Cosylab will present White Rabbit at conferences such as ICALEPCS (International Conference on Accelerator and Large Experimental Physics Control Systems), PCaPAC (International Workshop on Personal Computers and Particle Accelerator Controls) and IAEA Technical Meetings on Control, Data Acquisition and Remote Participation in Fusion Research. Cosylab will also inform its customers of the possible benefits of White Rabbit, as well as its potential to fit their specific requirements.

**Oregano Systems.** Oregano Systems will actively participate in the dissemination activities by means of conference and workshop proceedings. Additionally, the results will be implemented into existing evaluation platforms that will be presented at multi-vendor plug fests or at selected customers.
Exploitation strategy

The exploitation of White Rabbit has to be discussed separately for the industrial partners and university/research-centres. While the goal of the White Rabbit project fits the long-term research agenda of all the industrial partners, the main exploitation of the results is the positive influence of White Rabbit to the ongoing research of pre-product development, future trends and possibilities. This also includes exploitation using the insight gained in the state-of-the-art analysis and system design. Secondly and more directly, as the goal of the project is a pre-development of a future technology, the medium-term (3-5 years) exploitation goal is the development of actual products based on White Rabbit.

As the White Rabbit project is research-centred, the direct exploitation of the non-industrial partners can be conducted much earlier than for the product and business-oriented industrial partners. In accordance with the different research agendas of the universities, the exploitation is the research itself and spread of the results to the wider community. This includes the usual paths like doctoral and diploma theses, publication in journals, presentations at appropriate conferences such as shown in table S as well as the contribution to the open source community.

The exploitation of White Rabbit will, like the dissemination efforts, follow a two-pronged approach. In addition to the general exploitation plan, which involves both research and industrial partners, individual exploitation strategies will be identified to address each area covered by White Rabbit.

Individual exploitation plans

**CERN.** CERN will use the results of the White Rabbit project to renovate the timing system of the accelerators which act as the injectors for the Large Hadron Collider (LHC). These include a proton linac, a heavy-ion linac and several synchrotrons. In addition, White Rabbit will be an essential building block in the design of the control system for the Compact Linear Collider (CLIC), and its associated test facilities. Another key application at CERN concerns the distributed analogue acquisition system, where White Rabbit will be used to synchronize and time-tag trigger pulses.

**AAS.** The current expertise on the simulation of clock synchronized systems will be extended by experience gained with large-scale real-time systems. The investigations done as part of this project will open a new, related research topic for AAS, opening new possibilities for further projects in the area. In accordance with the general goals of publicly funded research institutions, exploitation will include the publication of results in conference proceedings, peer-reviewed journals, and PhD and master theses. AAS will also increase cooperation with other scientific partners in order to benefit from existing expertise. As a first step this will enable AAS to start a collaboration with the MedAustron project. The exploitation, in terms of contribution of knowledge, will be carried out by influencing the education of students, since the key researchers also act as lecturers at universities.

**GSI.** GSI intends to use the outcome from the White Rabbit project to provide the timing system services for the complete set of FAIR accelerators. In addition, GSI will use White Rabbit to interface the current timing system of the existing GSI accelerators to the new system. It is also expected that NUSTAR will adopt this technology for their future experiments and will obtain all necessary accelerator and beam information using White Rabbit. White Rabbit will be a cornerstone for other systems within the FAIR project such as the RF Bunchphase Timing System and all beam diagnostic systems.

**UniBS.** The University of Brescia will benefit from the increased knowledge on clock synchronization in at least three fields: research, didactics and contacts with Italian companies.
### Table 8: Conferences and working groups for dissemination

<table>
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<tr>
<th>Short Name</th>
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<tr>
<td>IAEA</td>
<td>Technical Meetings on Control, Data Acquisition and Remote Participation in Fusion Research</td>
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<tr>
<td>ICALEPCS</td>
<td>Int. Conference in Accelerator and Large Experimental Physics Control Systems</td>
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<tr>
<td>IPac</td>
<td>Int. Particle Accelerator Conference</td>
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<tr>
<td>PCaPAC</td>
<td>Int. Workshop on Personal Computers and Particle Accelerator Controls</td>
</tr>
<tr>
<td>TWEPP</td>
<td>Topical Workshop on Electronics for Particle Physics</td>
</tr>
<tr>
<td>ETFA</td>
<td>Int. IEEE Conference on Emerging Technologies and Factory Automation</td>
</tr>
<tr>
<td>ISPCS</td>
<td>Int. IEEE Symposium on Precision Clock Synchronization for Measurement, Control and Communication</td>
</tr>
<tr>
<td>I2MTC</td>
<td>Int. IEEE Instrumentation and Measurement Technology Conference</td>
</tr>
<tr>
<td>ISIE</td>
<td>Int. IEEE Symposium on Industrial Electronics</td>
</tr>
<tr>
<td>Real Time Conf.</td>
<td>Int. IEEE-NPSS Technical Committee on Computer Applications in Nuclear and Plasma Sciences</td>
</tr>
<tr>
<td>SENSORS</td>
<td>Int. IEEE Conference on Sensors</td>
</tr>
<tr>
<td>WFCS</td>
<td>Int. IEEE Workshop on Factory Communication Systems</td>
</tr>
<tr>
<td>IECON</td>
<td>Annual Conference of the IEEE Industrial Electronics Society</td>
</tr>
<tr>
<td>PTTI</td>
<td>Precise Time &amp; Time Interval Meeting</td>
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<tr>
<td>FeT</td>
<td>IFAC Int. Conference on Fieldbuses and Networks in Industrial and Embedded Systems.</td>
</tr>
<tr>
<td>IEC SC65C</td>
<td>Sub-committee MT9 and WG16 of Industrial Networks</td>
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<tr>
<td>WirelessHART</td>
<td>WirelessHART consortium</td>
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<tr>
<td>Autotestcon</td>
<td>The Support Systems Technology Conference</td>
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<tr>
<td>ESC</td>
<td>Embedded Systems Conference</td>
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<tr>
<td>IMAC</td>
<td>Conference and Exposition on Structural Dynamics</td>
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<tr>
<td>NI week</td>
<td>Worldwide Conference on Measurement and Automation</td>
</tr>
<tr>
<td>CTIA</td>
<td>Conference of the Cellular Telecommunications Industry Association</td>
</tr>
<tr>
<td>CASES</td>
<td>Int. Conference on Compilers, Architecture, and Synthesis for Embedded Systems</td>
</tr>
<tr>
<td>CODESISSS</td>
<td>Int. Conference on Hardware - Software Codesign and System Synthesis</td>
</tr>
<tr>
<td>IST Event</td>
<td>The Biennial ICT Event, European Union forum for discussing research and public policy in information and communication technologies</td>
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</table>
The investigations done as part of the project will open up new topics for its research group, whose goal is to become a national competence centre for real-time industrial communications and distributed measurement systems. The new knowledge acquired from the White Rabbit project will attract more students (undergraduate, graduate and PhD students) to the University. In addition, since UniBS can boast an active role in supporting local companies in the development of new products for industrial automation, White Rabbit can be an enabling technology for a great variety of state-of-the-art devices.

ZHAW. Swiss Universities of Applied Sciences have technology transfer as part of their mission. ZHAW will help interested industries to bring the White Rabbit technology, or parts of it, into their products or solutions. The knowledge acquired as part of the consortium will be used to further strengthen the institute’s position in the area of real-time Ethernet and to evolve the portfolio of supported technologies.

NI. National Instruments will use the results of the White Rabbit project to enable improved timing and synchronization for modular instrumentation in multiple industries. NI’s current timing technologies enable advanced applications in aerospace, defence, power monitoring, control systems, etc. by sharing electrical timing signals or through timing protocols including IEEE 1588, GPS and IRIG. It is anticipated that White Rabbit will become a complementary high performance option to synchronize systems. To complement the efforts of the EU-funded White Rabbit research, NI will fund the development of White Rabbit for PXI, the highest performance timing platform for these modular instrument applications.

Hirschmann. Hirschmann is interested in the industrialisation of the White Rabbit switch implementation into a commercial product. Hirschmann believes there is a need for this technology in applications in the scientific, industrial automation and instrumentation area. Such a product will complement Hirschmann’s Ethernet product offering with a very high-performance solution for the most demanding applications.

Cosylab. Cooperating on the White Rabbit project will further advance Cosylab’s understanding of timing systems, and will put the company in a very good position to offer its clients consulting and development services in this field. Considering that White Rabbit will likely meet requirements of a wider range of Cosylab’s existing and potential customers, Cosylab will also have an incentive to develop a White Rabbit product suite. Cosylab’s speciality would be highly-customisable products manufactured in quantities of several hundred units.

Oregano. As an SME, Oregano Systems’ exploitation has to focus on the identification of niche markets and the gain of knowledge for pre-product development. The results of the project will allow Oregano Systems to implement high-resolution timestamping technology into its hardware products and will trigger the design of a new family of clock synchronization hardware devices suited for niche markets like Test & Measurement requiring accuracies and timestamp resolution in the sub-nanosecond range.

Intellectual property rights

The consortium considers the management and the public access to knowledge as an important task. The project’s handling of IPRs will be detailed in the Consortium Agreement and will be in line with the Model Contract of the EC, particularly Annex I.33, “Protection of knowledge”. The Consortium Agreement will distinguish between pre-existing knowledge of the partners (background), publicly available knowledge and protected knowledge generated by the project (foreground). Within the scope and duration of this project, knowledge generated will be publicly available and protected under open license for both hardware and software,
offering practical accessibility to the all technical designs and documents in the Open Hardware Repository.

Open licenses permit knowledge and learning to be widely shared and readily adapted, improved or built upon and allow those later improvements to be readily distributed [28]. The terms and conditions of general public licenses are available to anybody receiving a copy of the work that has a General Public License applied to it. Any licensee who adheres to the terms and conditions is given permission to modify the work, as well as to copy and redistribute the work or any derivative version.

For software, firmware, and HDL code, “copyleft licenses” seem the most appropriate. These licenses use the privileges granted to authors via the copyright mechanism to ensure that the intellectual property is adequately protected and disseminated. In our case, the policy will be to make the results as widely available as possible in order to benefit from peer review and to ease dissemination. Concerning hardware designs, copyright is not an effective means of protection, and an alternative method has to be found to achieve the same goals of peer review and wide adoption. Open hardware licensing is a relatively new legal field, and the consortium will be attentive to evolutions in order to provide a solid overall licensing scheme in the Consortium Agreement.
4 Ethical Issues

The consortium confirms that no ethical issues apply to this proposal.

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- Does the proposal involve children?
- Does the proposal involve patients or persons not able to give consent?
- Does the proposal involve adult healthy volunteers?
- Does the proposal involve Human Genetic Material?
- Does the proposal involve Human biological samples?
- Does the proposal involve Human data collection?

**Research on Human embryo/foetus**

- Does the proposal involve Human Embryos?
- Does the proposal involve Human Foetal Tissue / Cells?
- Does the proposal involve Human Embryonic Stem Cells?

**Privacy**

- Does the proposal involve processing of genetic information or personal data (e.g. health, sexual lifestyle, ethnicity, political opinion, religious or philosophical conviction)
- Does the proposal involve tracking the location or observation of people?

**Research on Animals**

- Does the proposal involve research on animals?
- Are those animals transgenic small laboratory animals?
- Are those animals transgenic farm animals?
- Are those animals cloned farm animals?
- Are those animals non-human primates?

**Research Involving Developing Countries**

- Use of local resources (genetic, animal, plant etc.)
- Benefit to local community (capacity building i.e. access to healthcare, education etc.)

**Dual Use**

- Research having direct military application
- Research having the potential for terrorist abuse

**ICT Implants**

- Does the proposal involve clinical trials of ICT implants?

I CONFIRM THAT NONE OF THE ABOVE ISSUES APPLY TO MY PROPOSAL

YES
References


