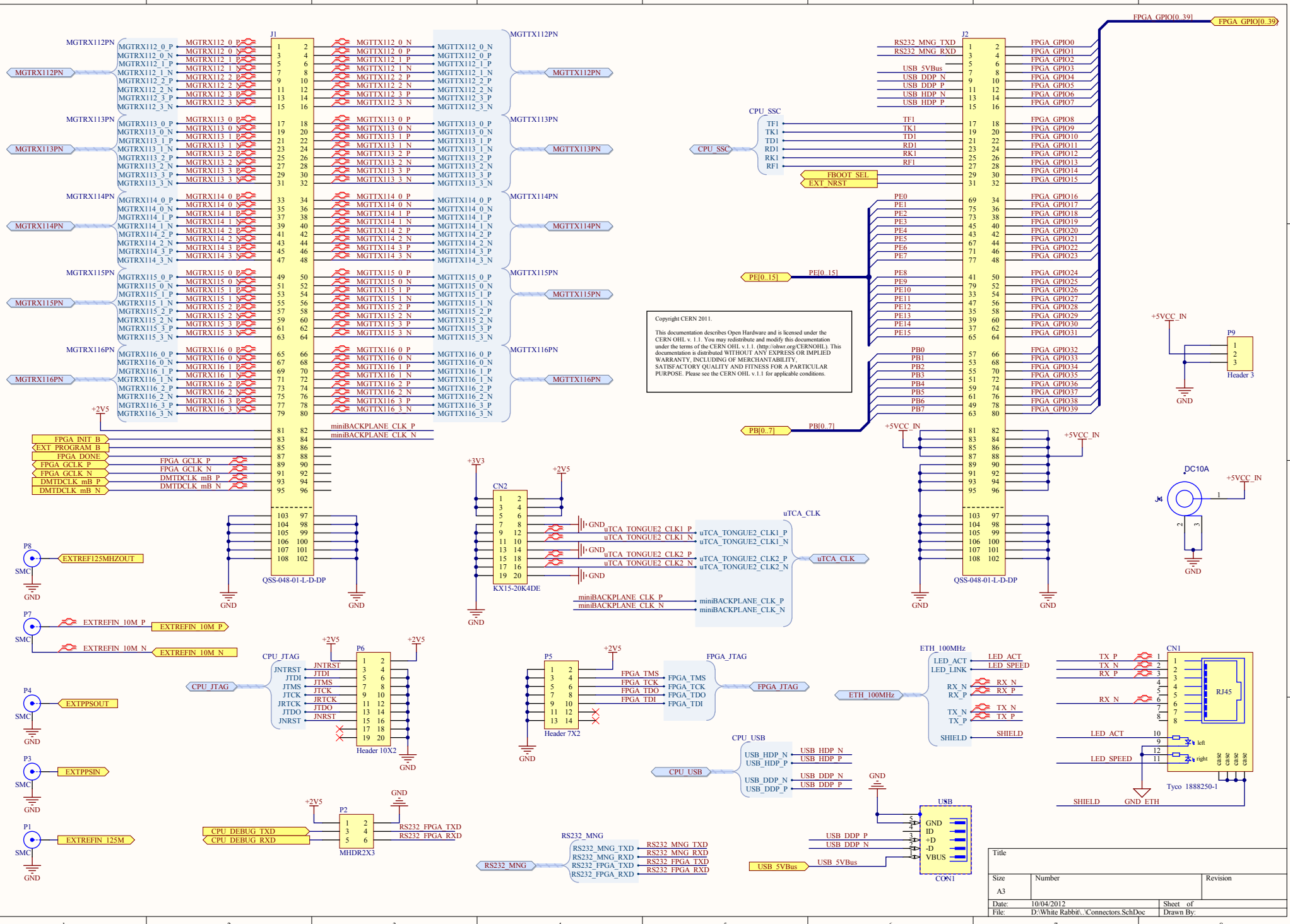
J1
J2
MGTRX112PN
MGTRX113PN
MGTRX114PN
MGTRX115PN
MGTRX116PN
MGTTX112PN
MGTTX113PN
MGTTX114PN
MGTTX115PN
MGTTX116PN
QSS-048-01-L-D-DP
FPGA_GPIO[0..39]
CPU_SSC
FBOOT_SEL
EXT_NRST
PE[0..15]
PB[0..7]
+5VCC_IN
Header 3
DC10A
FPGA_INIT_B
EXT_PROGRAM_B
FPGA_DONE
FPGA_GCLK_P
FPGA_GCLK_N
DMTDCLK_mB_P
DMTDCLK_mB_N
miniBACKPLANE_CLK_P
miniBACKPLANE_CLK_N
CN2
KX15-20K4DE
uTCA_CLK
P8
EXTREF125MHZOUT
SMC
GND
P7
EXTREFIN_10M_P
EXTREFIN_10M_N
P4
EXTPPSOUT
P3
EXTPPSIN
P1
EXTREFIN_125M
CPU_JTAG
P6
Header 10X2
P5
Header 7X2
FPGA_JTAG
ETH_100MHz
CN1
RJ45
Tyco 1888250-1
CPU_USB
USB
CON1
CPU_DEBUG_TXD
CPU_DEBUG_RXD
P2
MHDR2X3
RS232_MNG
RS232_MNG_TXD
RS232_MNG_RXD
RS232_FPGA_TXD
RS232_FPGA_RXD
USB_5VBus
USB_DDP_P
USB_DDP_N
USB_HDP_P
USB_HDP_N
LED_ACT
LED_SPEED
SHIELD
GND_ETH
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Date:
10/04/2012
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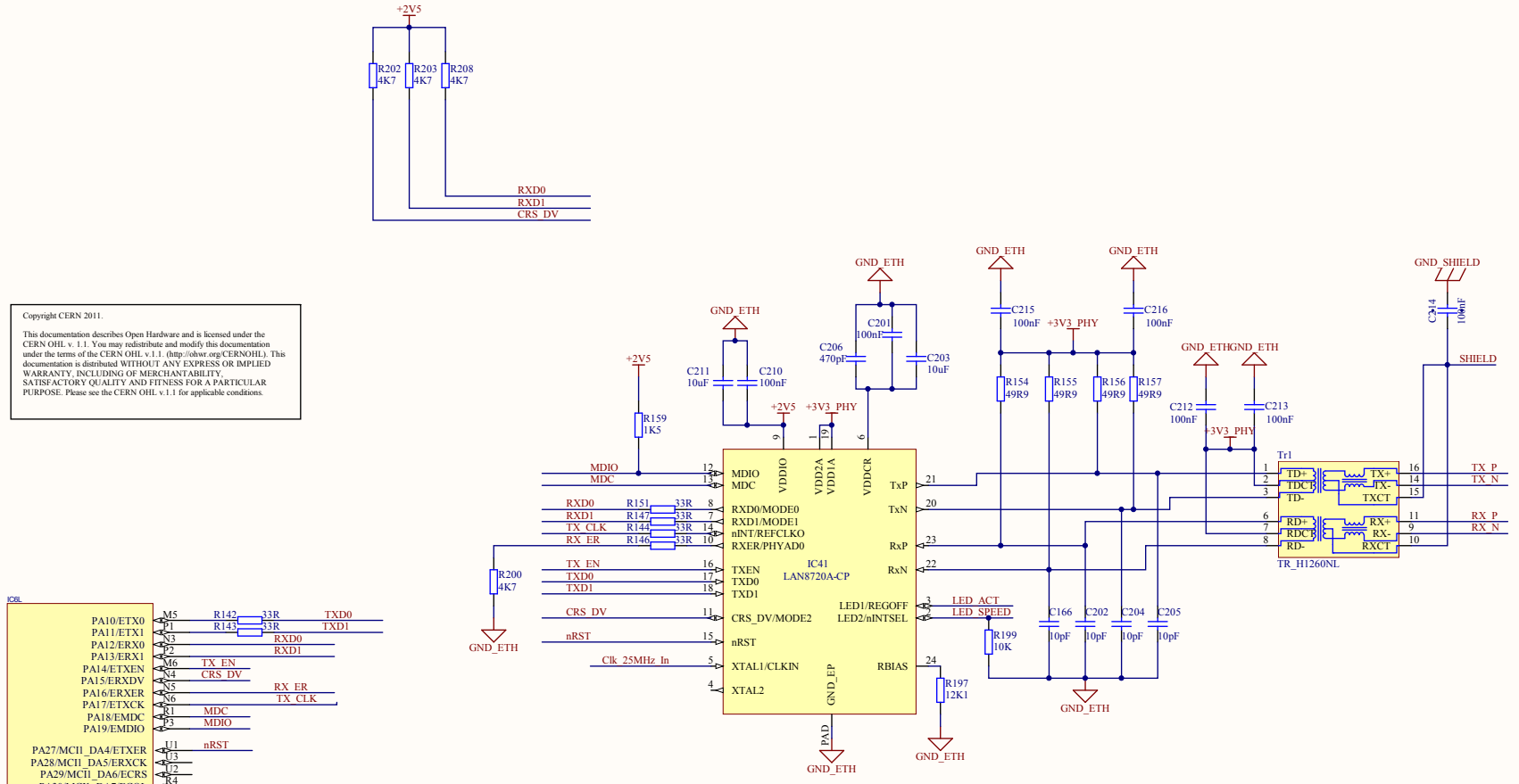

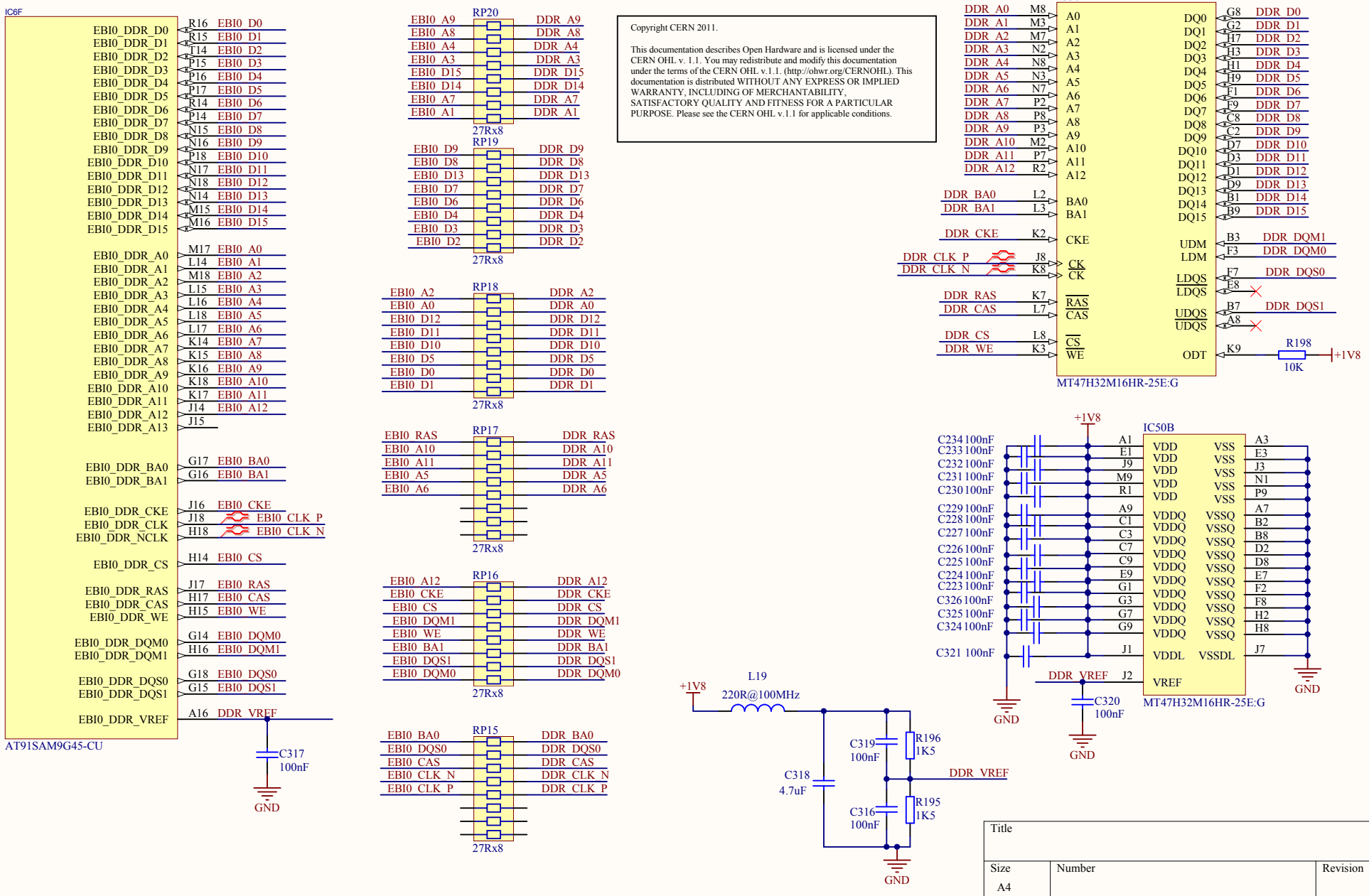
IC6F
EBI0_DDR_D0
EBI0_DDR_D1
EBI0_DDR_D2
EBI0_DDR_D3
EBI0_DDR_D4
EBI0_DDR_D5
EBI0_DDR_D6
EBI0_DDR_D7
EBI0_DDR_D8
EBI0_DDR_D9
EBI0_DDR_D10
EBI0_DDR_D11
EBI0_DDR_D12
EBI0_DDR_D13
EBI0_DDR_D14
EBI0_DDR_D15
EBI0_DDR_A0
EBI0_DDR_A1
EBI0_DDR_A2
EBI0_DDR_A3
EBI0_DDR_A4
EBI0_DDR_A5
EBI0_DDR_A6
EBI0_DDR_A7
EBI0_DDR_A8
EBI0_DDR_A9
EBI0_DDR_A10
EBI0_DDR_A11
EBI0_DDR_A12
EBI0_DDR_A13
EBI0_DDR_BA0
EBI0_DDR_BA1
EBI0_DDR_CKE
EBI0_DDR_CLK
EBI0_DDR_NCLK
EBI0_DDR_CS
EBI0_DDR_RAS
EBI0_DDR_CAS
EBI0_DDR_WE
EBI0_DDR_DQM0
EBI0_DDR_DQM1
EBI0_DDR_DQS0
EBI0_DDR_DQS1
EBI0_DDR_VREF
AT91SAM9G45-CU
C317
100nF
GND
RP20
RP19
RP18
RP17
RP16
RP15
27Rx8
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IC50A
DDR_A0
DDR_A1
DDR_A2
DDR_A3
DDR_A4
DDR_A5
DDR_A6
DDR_A7
DDR_A8
DDR_A9
DDR_A10
DDR_A11
DDR_A12
DDR_BA0
DDR_BA1
DDR_CKE
DDR_CLK_P
DDR_CLK_N
DDR_RAS
DDR_CAS
DDR_CS
DDR_WE
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
UDM
LDM
LDQS
UDQS
ODT
R198
10K
+1V8
MT47H32M16HR-25E:G
IC50B
VDD
VSS
VDDQ
VSSQ
VDDL
VSSDL
VREF
C234 100nF
C233 100nF
C232 100nF
C231 100nF
C230 100nF
C229 100nF
C228 100nF
C227 100nF
C226 100nF
C225 100nF
C224 100nF
C223 100nF
C326 100nF
C325 100nF
C324 100nF
C321 100nF
C320
100nF
L19
220R@100MHz
C319
100nF
C318
4.7uF
C316
100nF
R196
1K5
R195
1K5
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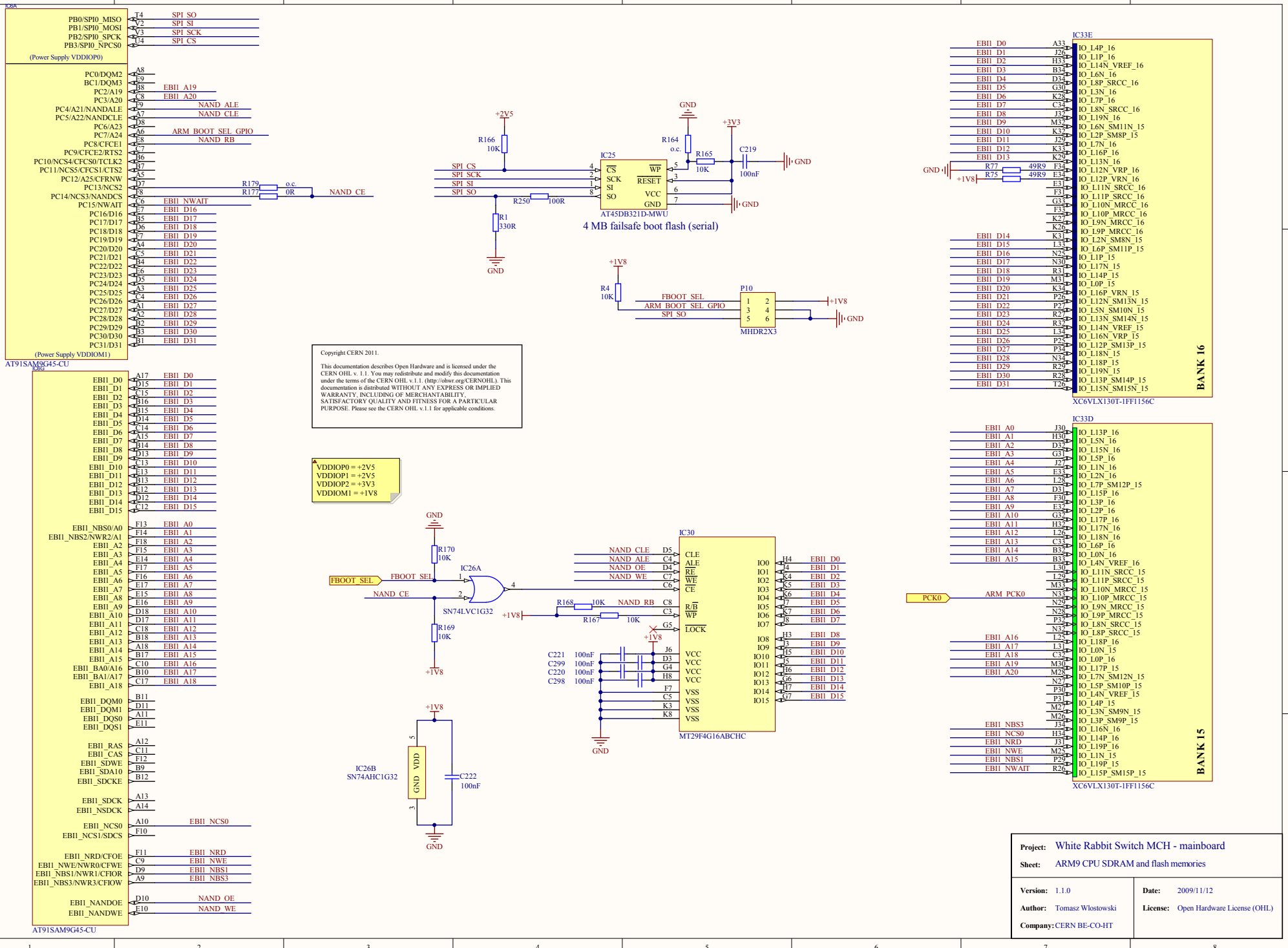
PB0/SPI0_MISO
PB1/SPI0_MOSI
PB2/SPI0_SPCK
PB3/SPI0_NPCS0
(Power Supply VDDIOP0)
PC0/DQM2
PC1/DQM3
PC2/A19
PC3/A20
PC4/A21/NANDALE
PC5/A22/NANDCLE
PC6/A23
PC7/A24
PC8/CFCE1
PC9/CFCE2/RTS2
PC10/NCS4/CFCS0/TCLK2
PC11/NCS5/CFCS1/CTS2
PC12/A25/CFRNW
PC13/NCS2
PC14/NCS3/NANDCS
PC15/NWAIT
PC16/D16
PC17/D17
PC18/D18
PC19/D19
PC20/D20
PC21/D21
PC22/D22
PC23/D23
PC24/D24
PC25/D25
PC26/D26
PC27/D27
PC28/D28
PC29/D29
PC30/D30
PC31/D31
(Power Supply VDDIOM1)
AT91SAM9G45-CU
SPI_SO
SPI_SI
SPI_SCK
SPI_CS
EBI1_A19
EBI1_A20
NAND_ALE
NAND_CLE
ARM_BOOT_SEL_GPIO
NAND_RB
R179
R177
o.c.
0R
NAND_CE
EBI1_NWAIT
EBI1_D16
EBI1_D17
EBI1_D18
EBI1_D19
EBI1_D20
EBI1_D21
EBI1_D22
EBI1_D23
EBI1_D24
EBI1_D25
EBI1_D26
EBI1_D27
EBI1_D28
EBI1_D29
EBI1_D30
EBI1_D31
EBI1_D0
EBI1_D1
EBI1_D2
EBI1_D3
EBI1_D4
EBI1_D5
EBI1_D6
EBI1_D7
EBI1_D8
EBI1_D9
EBI1_D10
EBI1_D11
EBI1_D12
EBI1_D13
EBI1_D14
EBI1_D15
EBI1_NBS0/A0
EBI1_NBS2/NWR2/A1
EBI1_A2
EBI1_A3
EBI1_A4
EBI1_A5
EBI1_A6
EBI1_A7
EBI1_A8
EBI1_A9
EBI1_A10
EBI1_A11
EBI1_A12
EBI1_A13
EBI1_A14
EBI1_A15
EBI1_BA0/A16
EBI1_BA1/A17
EBI1_A18
EBI1_DQM0
EBI1_DQM1
EBI1_DQS0
EBI1_DQS1
EBI1_RAS
EBI1_CAS
EBI1_SDWE
EBI1_SDA10
EBI1_SDCKE
EBI1_SDCK
EBI1_NSDCK
EBI1_NCS0
EBI1_NCS1/SDCS
EBI1_NRD/CFOE
EBI1_NWE/NWR0/CFWE
EBI1_NBS1/NWR1/CFIOR
EBI1_NBS3/NWR3/CFIOW
EBI1_NANDOE
EBI1_NANDWE
NAND_OE
NAND_WE
AT91SAM9G45-CU
+2V5
R166
10K
SPI_CS
SPI_SCK
SPI_SI
SPI_SO
R250
100R
R1
330R
GND
IC25
CS
SCK
SI
SO
WP
RESET
VCC
GND
AT45DB321D-MWU
4 MB failsafe boot flash (serial)
R164
o.c.
R165
10K
+3V3
C219
100nF
+1V8
R4
10K
FBOOT_SEL
ARM_BOOT_SEL_GPIO
SPI_SO
P10
MHDR2X3
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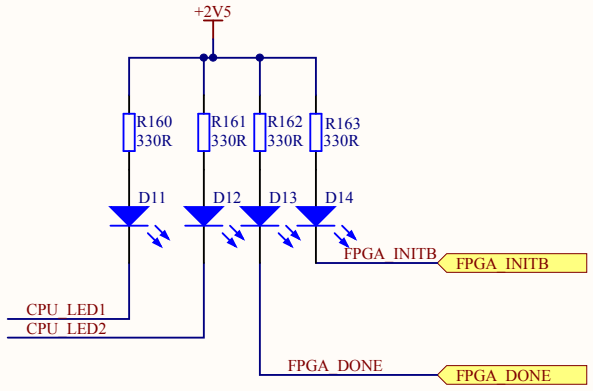
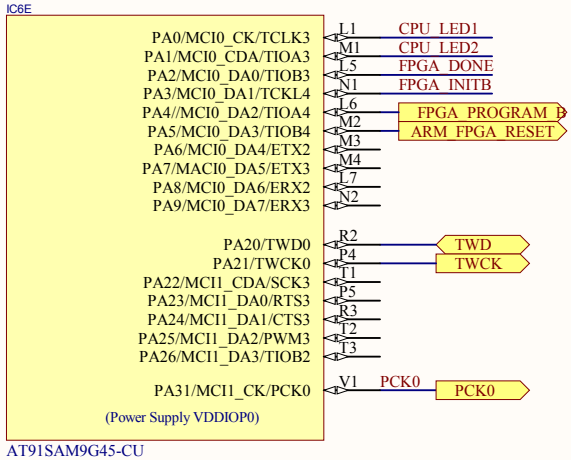
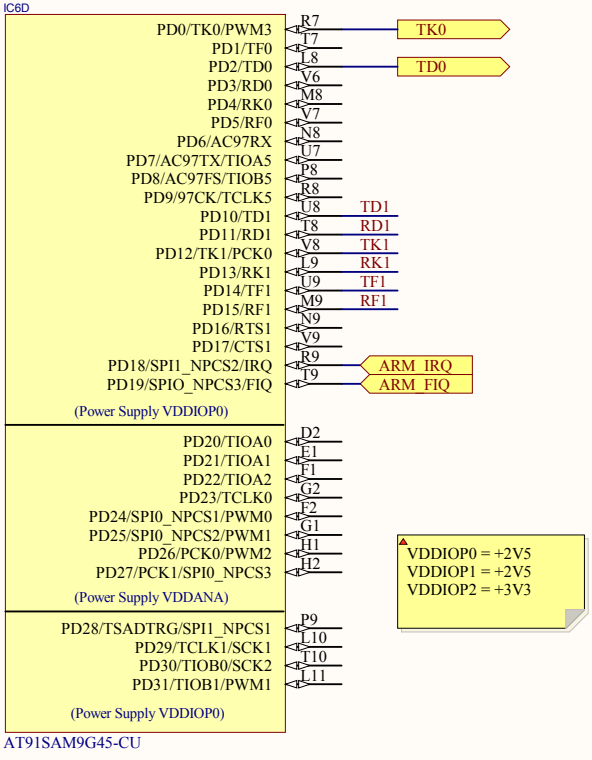
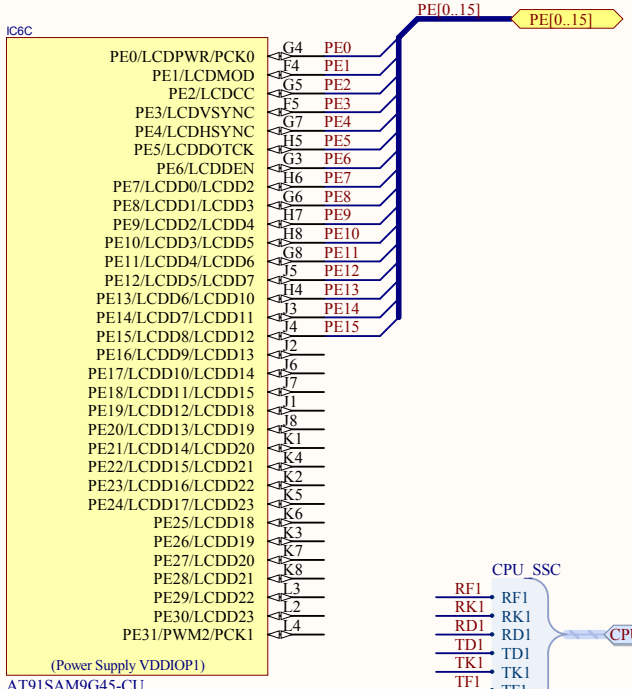
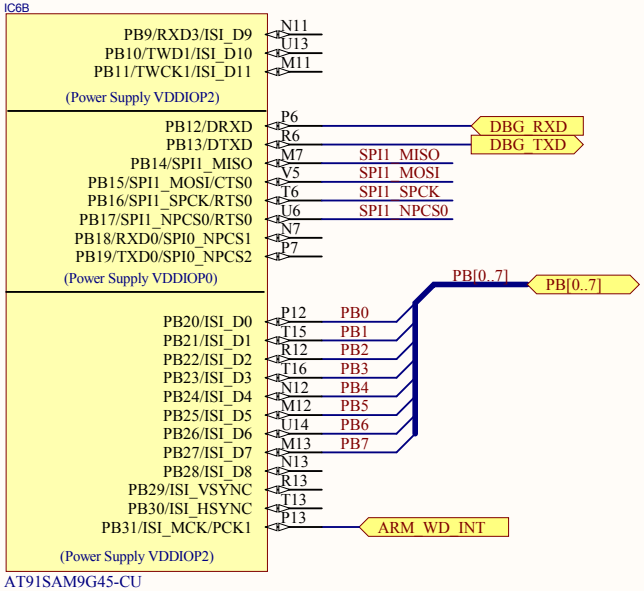
VDDIOP0 = +2V5
VDDIOP1 = +2V5
VDDIOP2 = +3V3
VDDIOM1 = +1V8
R170
10K
R169
10K
IC26A
SN74LVC1G32
NAND_CE
R168
10K
R167
10K
NAND_RB
IC30
CLE
ALE
RE
WE
CE
R/B
WP
LOCK
VCC
VSS
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
IO10
IO11
IO12
IO13
IO14
IO15
MT29F4G16ABCHC
C221
C299
C220
C298
100nF
IC26B
SN74AHC1G32
C222
100nF
IC33E
IC33D
BANK 16
BANK 15
XC6VLX130T-1FF1156C
PCK0
ARM_PCK0
Project: White Rabbit Switch MCH - mainboard
Sheet: ARM9 CPU SDRAM and flash memories
Version: 1.1.0
Date: 2009/11/12
Author: Tomasz Wlostowski
License: Open Hardware License (OHL)
Company: CERN BE-CO-HT











White Rabbit Switch MCH - mainboard

ARM9 CPU I/O ports, busses and power

Project:

Sheet:

Date: 2009/11/12

Tomasz Wlostowski

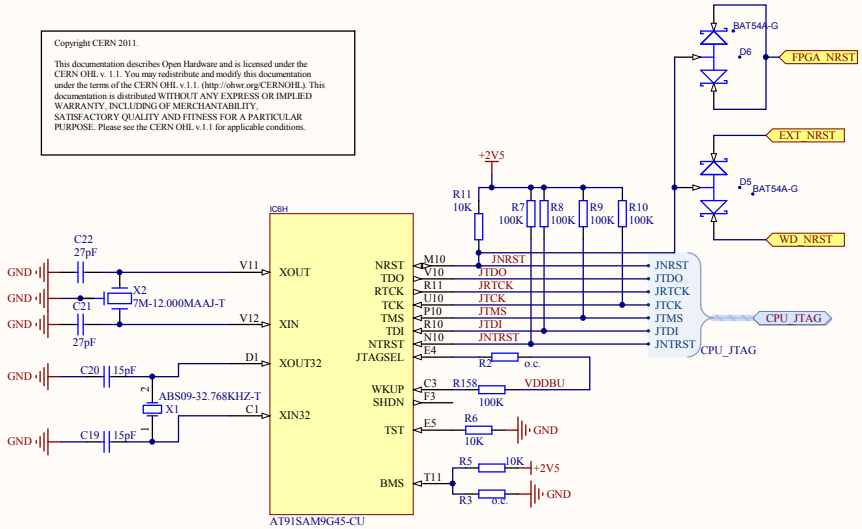
License: Open Hardware License (OHL)

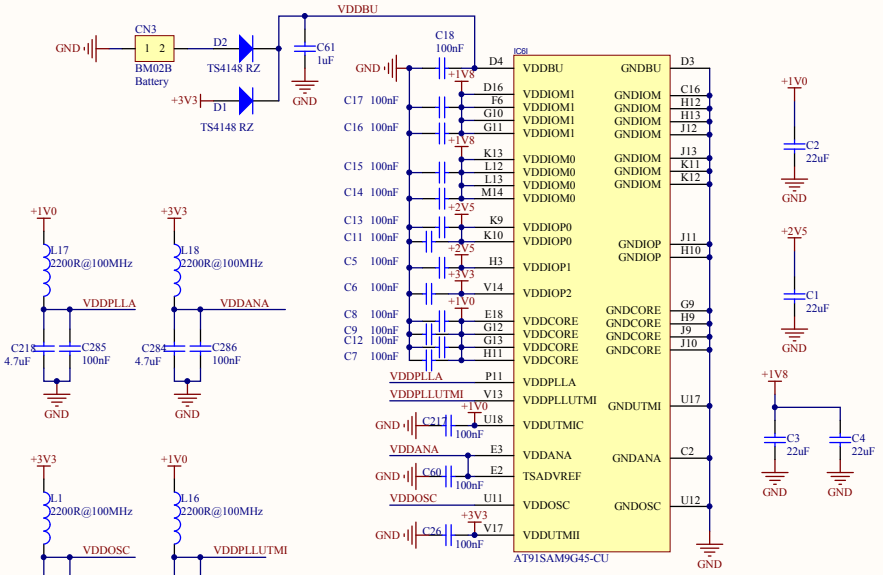
Version:

CERN BE-CO-HT

Company:

Author:





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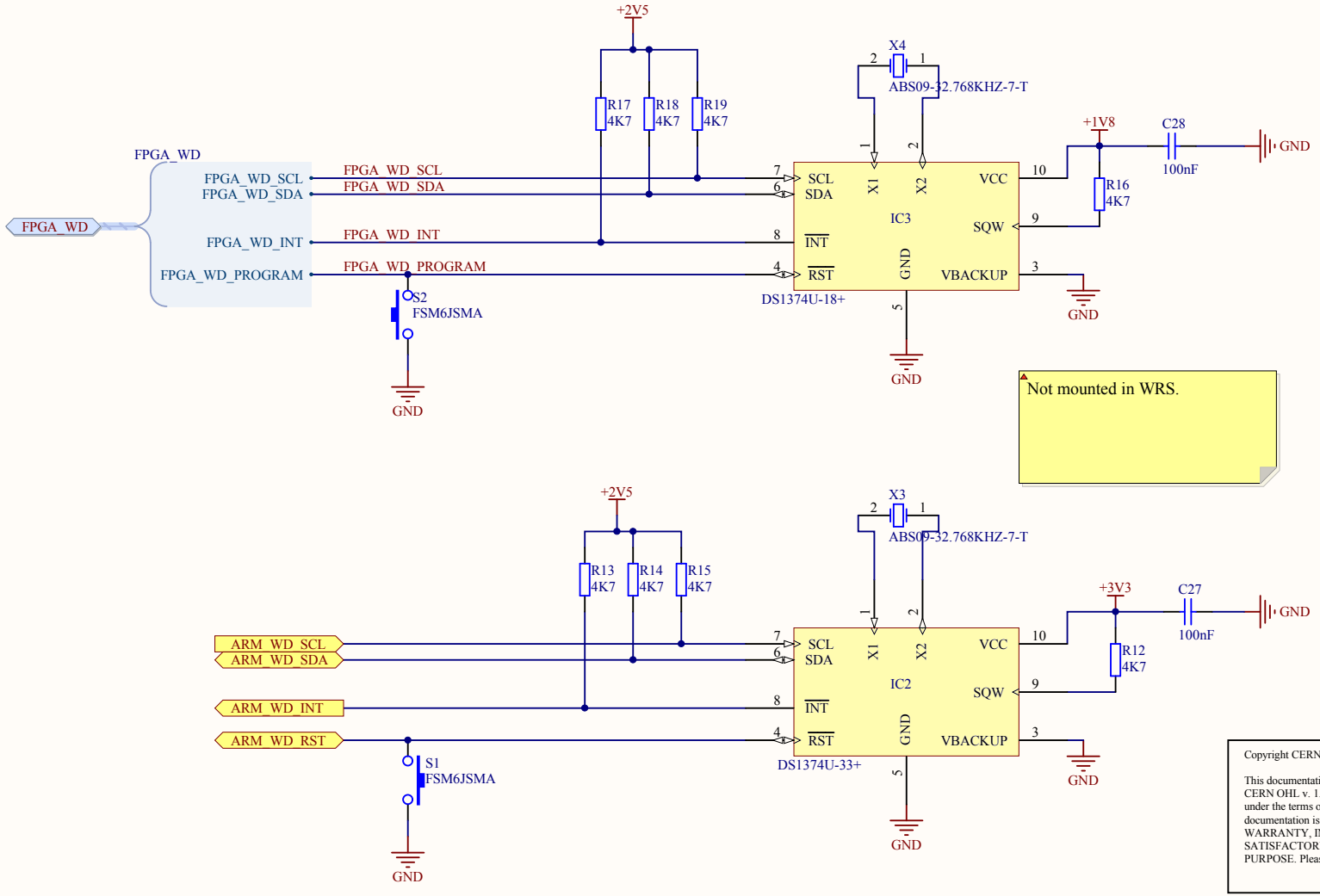

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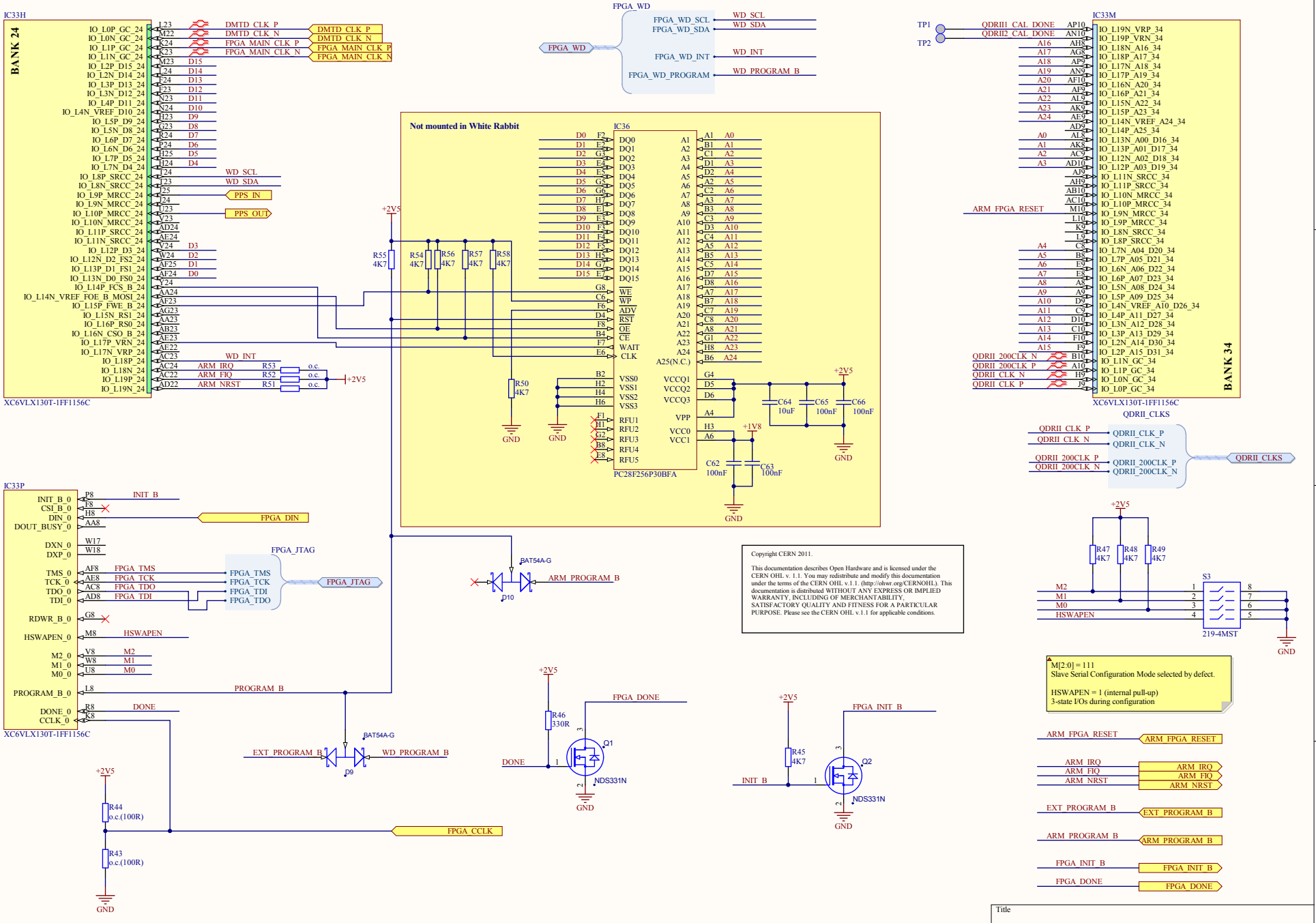
IC33H
BANK 24
XC6VLX130T-1FF1156C
DMTD_CLK_P
DMTD_CLK_N
FPGA_MAIN_CLK_P
FPGA_MAIN_CLK_N
WD_SCL
WD_SDA
PPS_IN
PPS_OUT
WD_INT
ARM_IRQ
ARM_FIQ
ARM_NRST
R53
R52
R51
o.c.
+2V5
FPGA_WD
FPGA_WD_SCL
FPGA_WD_SDA
FPGA_WD_INT
FPGA_WD_PROGRAM
WD_PROGRAM_B
Not mounted in White Rabbit
IC36
PC28F256P30BFA
R55 4K7
R54 4K7
R56 4K7
R57 4K7
R58 4K7
R50 4K7
GND
C64 10uF
C65 100nF
C66 100nF
C62 100nF
C63 100nF
+1V8
IC33M
BANK 34
XC6VLX130T-1FF1156C
TP1
TP2
QDRII1_CAL_DONE
QDRII2_CAL_DONE
ARM_FPGA_RESET
QDRII_200CLK_N
QDRII_200CLK_P
QDRII_CLK_N
QDRII_CLK_P
QDRII_CLKS
IC33P
INIT_B_0
CSI_B_0
DIN_0
DOUT_BUSY_0
DXN_0
DXP_0
TMS_0
TCK_0
TDO_0
TDI_0
RDWR_B_0
HSWAPEN_0
M2_0
M1_0
M0_0
PROGRAM_B_0
DONE_0
CCLK_0
INIT_B
FPGA_DIN
FPGA_JTAG
FPGA_TMS
FPGA_TCK
FPGA_TDO
FPGA_TDI
HSWAPEN
M2
M1
M0
PROGRAM_B
DONE
FPGA_CCLK
BAT54A-G
D10
ARM_PROGRAM_B
D9
EXT_PROGRAM_B
R44 o.c.(100R)
R43 o.c.(100R)
R46 330R
R45 4K7
Q1
Q2
NDS331N
FPGA_DONE
FPGA_INIT_B
R47 4K7
R48 4K7
R49 4K7
S3
219-4MST
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M[2:0] = 111
Slave Serial Configuration Mode selected by defect.
HSWAPEN = 1 (internal pull-up)
3-state I/Os during configuration
Title
Size
A3
Number
Revision
Date: 10/04/2012
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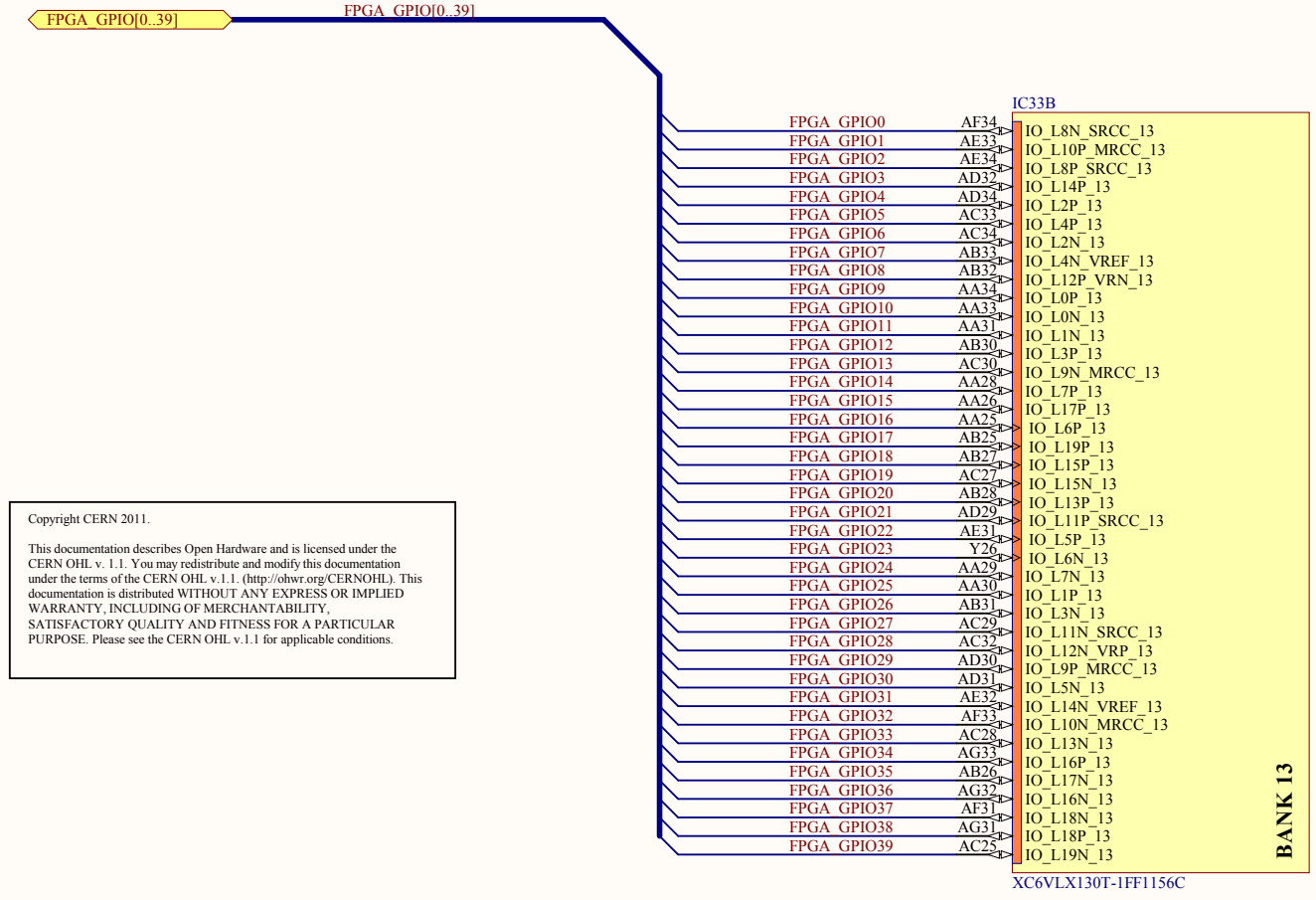

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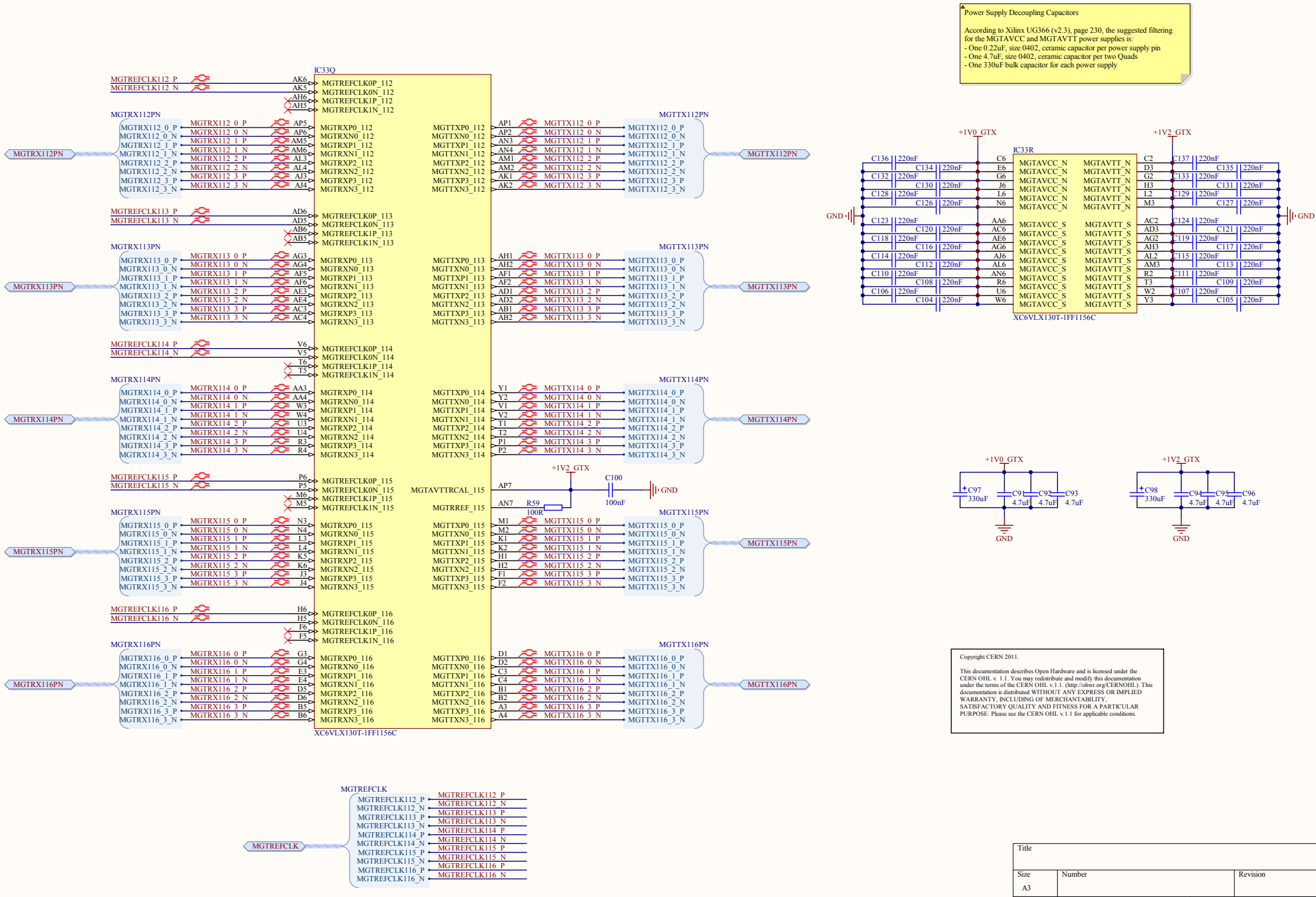
IC33Q
XC6VLX130T-1FF1156C
MGTREFCLK112_P
MGTREFCLK112_N
MGTREFCLK113_P
MGTREFCLK113_N
MGTREFCLK114_P
MGTREFCLK114_N
MGTREFCLK115_P
MGTREFCLK115_N
MGTREFCLK116_P
MGTREFCLK116_N
MGTREFCLK0P_112
MGTREFCLK0N_112
MGTREFCLK1P_112
MGTREFCLK1N_112
MGTREFCLK0P_113
MGTREFCLK0N_113
MGTREFCLK1P_113
MGTREFCLK1N_113
MGTREFCLK0P_114
MGTREFCLK0N_114
MGTREFCLK1P_114
MGTREFCLK1N_114
MGTREFCLK0P_115
MGTREFCLK0N_115
MGTREFCLK1P_115
MGTREFCLK1N_115
MGTREFCLK0P_116
MGTREFCLK0N_116
MGTREFCLK1P_116
MGTREFCLK1N_116
MGTAVTTRCAL_115
MGTRREF_115
MGTRX112PN
MGTRX113PN
MGTRX114PN
MGTRX115PN
MGTRX116PN
MGTTX112PN
MGTTX113PN
MGTTX114PN
MGTTX115PN
MGTTX116PN
MGTREFCLK
+1V2_GTX
C100
100nF
GND
R59
100R
AP7
AN7
Power Supply Decoupling Capacitors
According to Xilinx UG366 (v2.3), page 230, the suggested filtering for the MGTAVCC and MGTAVTT power supplies is:
- One 0.22uF, size 0402, ceramic capacitor per power supply pin
- One 4.7uF, size 0402, ceramic capacitor per two Quads
- One 330uF bulk capacitor for each power supply
IC33R
XC6VLX130T-1FF1156C
+1V0_GTX
+1V2_GTX
C97 330uF
C91 4.7uF
C92 4.7uF
C93 4.7uF
C98 330uF
C94 4.7uF
C95 4.7uF
C96 4.7uF
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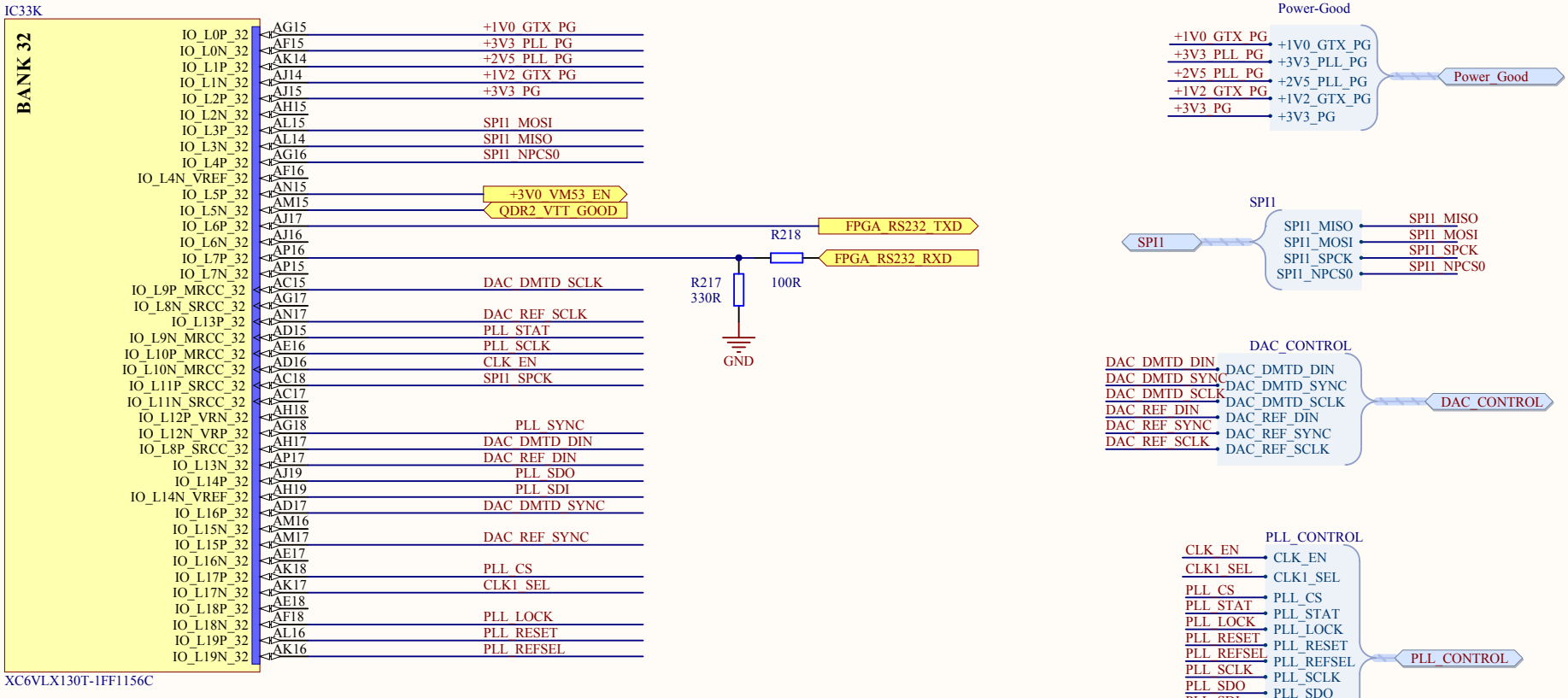

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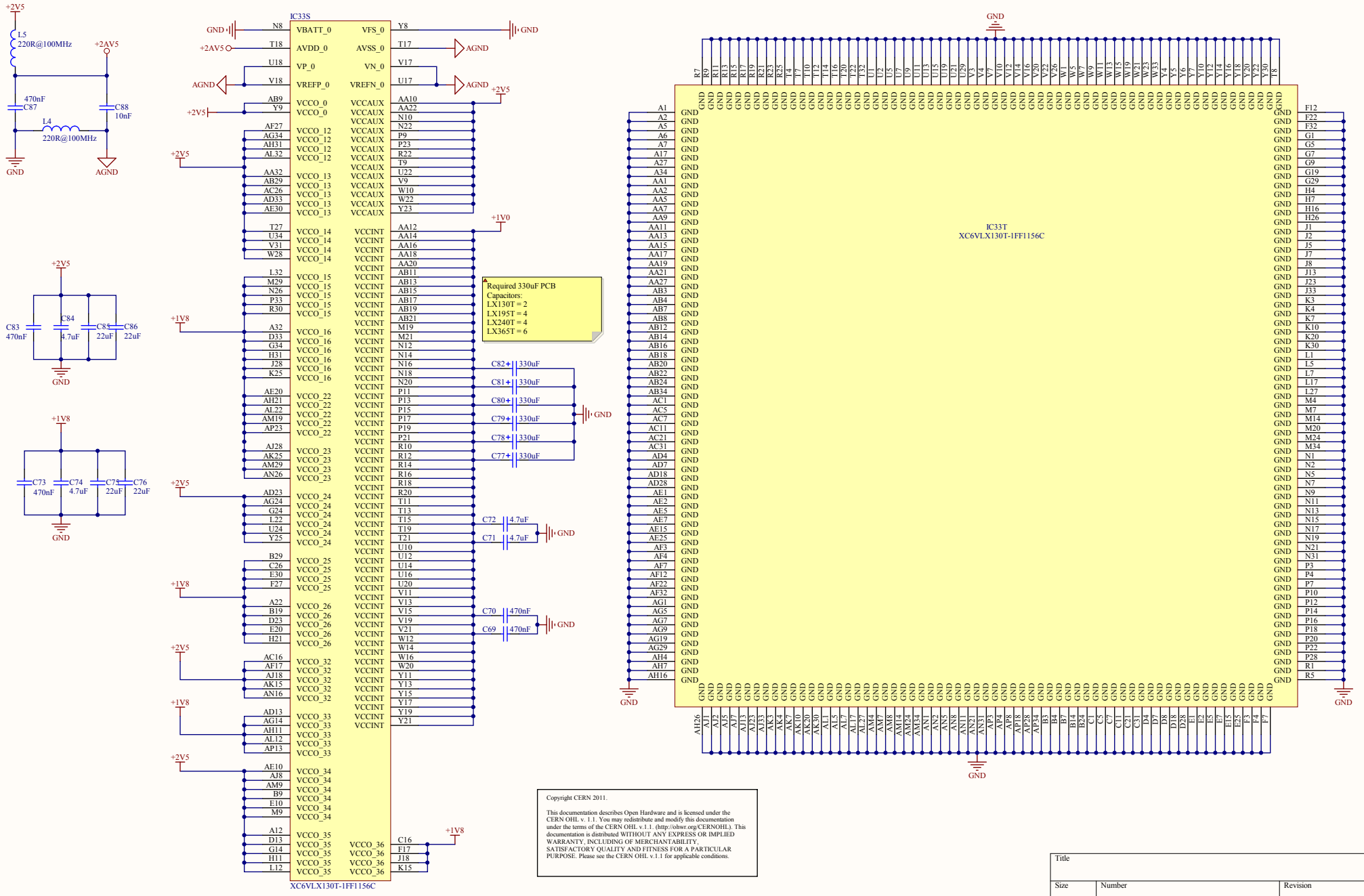
IC33S
XC6VLX130T-1FF1156C
IC33T
XC6VLX130T-1FF1156C
Required 330uF PCB Capacitors:
LX130T = 2
LX195T = 4
LX240T = 4
LX365T = 6
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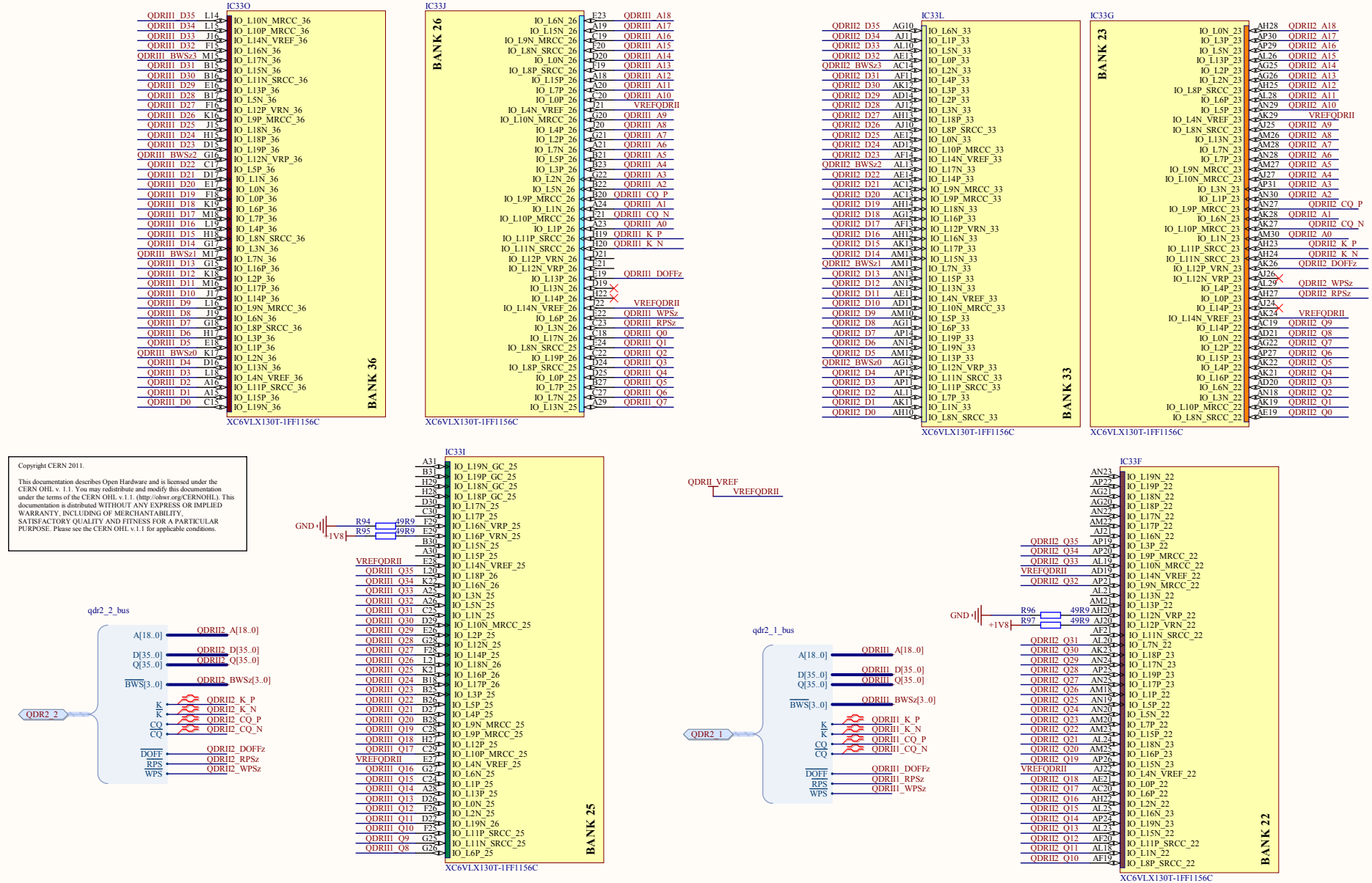
IC33O
BANK 36
XC6VLX130T-1FF1156C
IC33J
BANK 26
XC6VLX130T-1FF1156C
IC33L
BANK 33
XC6VLX130T-1FF1156C
IC33G
BANK 23
XC6VLX130T-1FF1156C
IC33I
BANK 25
XC6VLX130T-1FF1156C
IC33F
BANK 22
XC6VLX130T-1FF1156C
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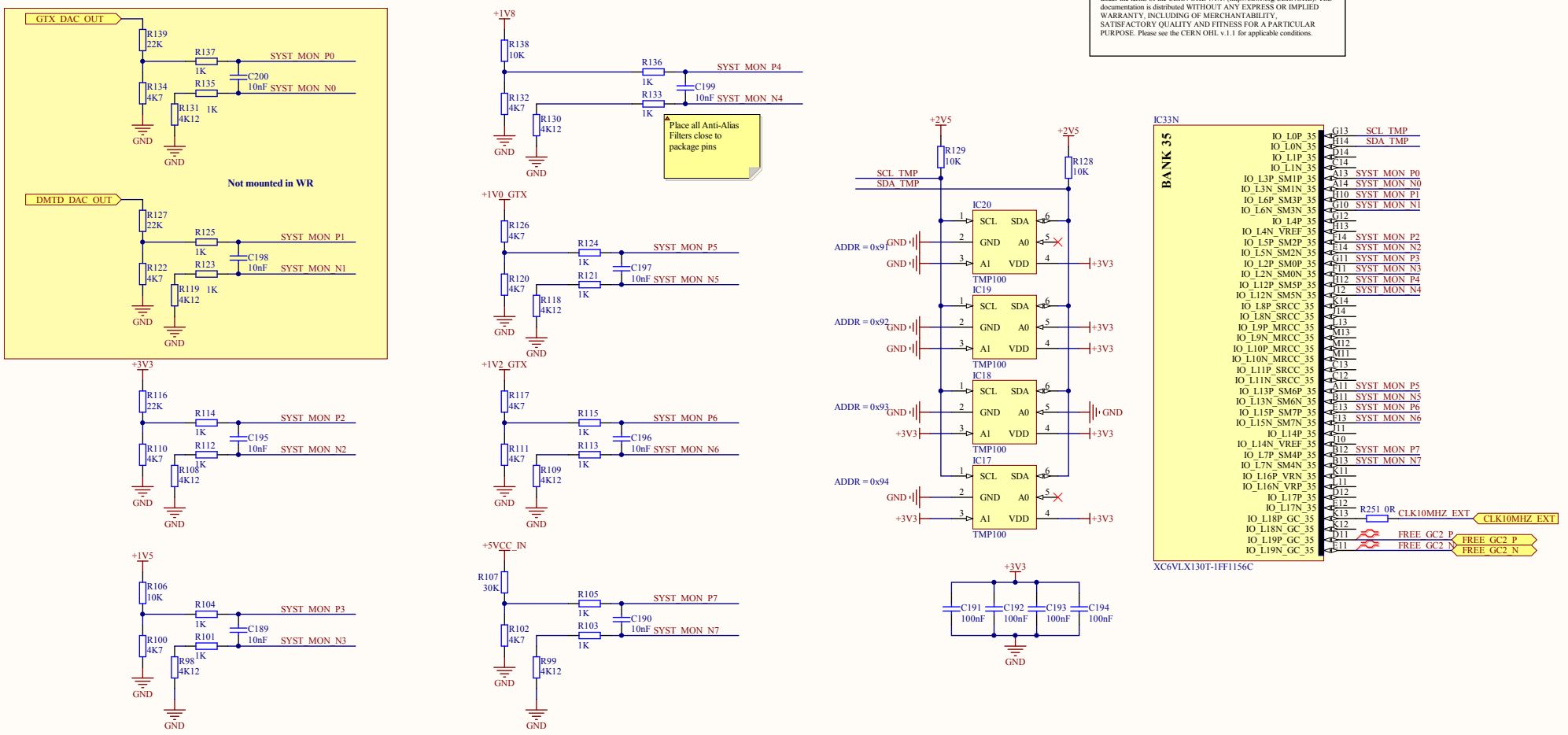
qdr2_2_bus
QDR2_2
qdr2_1_bus
QDR2_1
QDRII_VREF
VREFQDRII
GND
+1V8
R94
R95
R96
R97
49R9
Title
Size
A3
Number
Revision
Date:
10/04/2012
Sheet of
File:
D:\White Rabbit\..\FPGA_QDRII.SchDoc
Drawn By:



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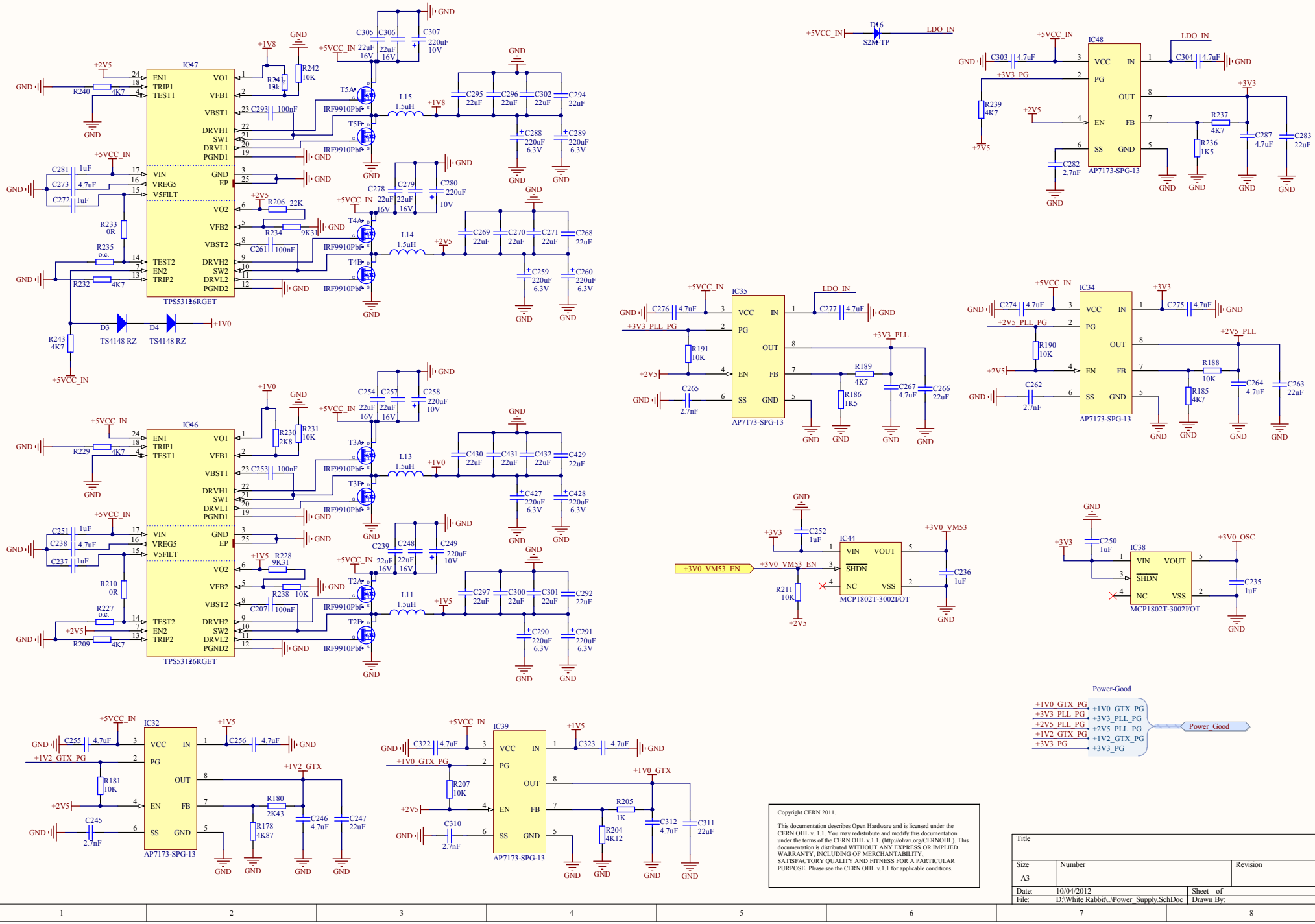
Size: A3	Number	Revision
Date: 10/04/2012		Sheet of
File: D:\White Rabbit\...\FPGA_System_Monitor.SchDoc		Drawn By:


IC47
TPS53126RGET
IC46
TPS53126RGET
D16
S2M-TP
IC48
AP7173-SPG-13
IC35
AP7173-SPG-13
IC34
AP7173-SPG-13
IC44
MCP1802T-3002I/OT
IC38
MCP1802T-3002I/OT
IC32
AP7173-SPG-13
IC39
AP7173-SPG-13
D3
TS4148 RZ
D4
TS4148 RZ
Power-Good
Power_Good
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Title
Size
A3
Number
Revision
Date:
10/04/2012
Sheet of
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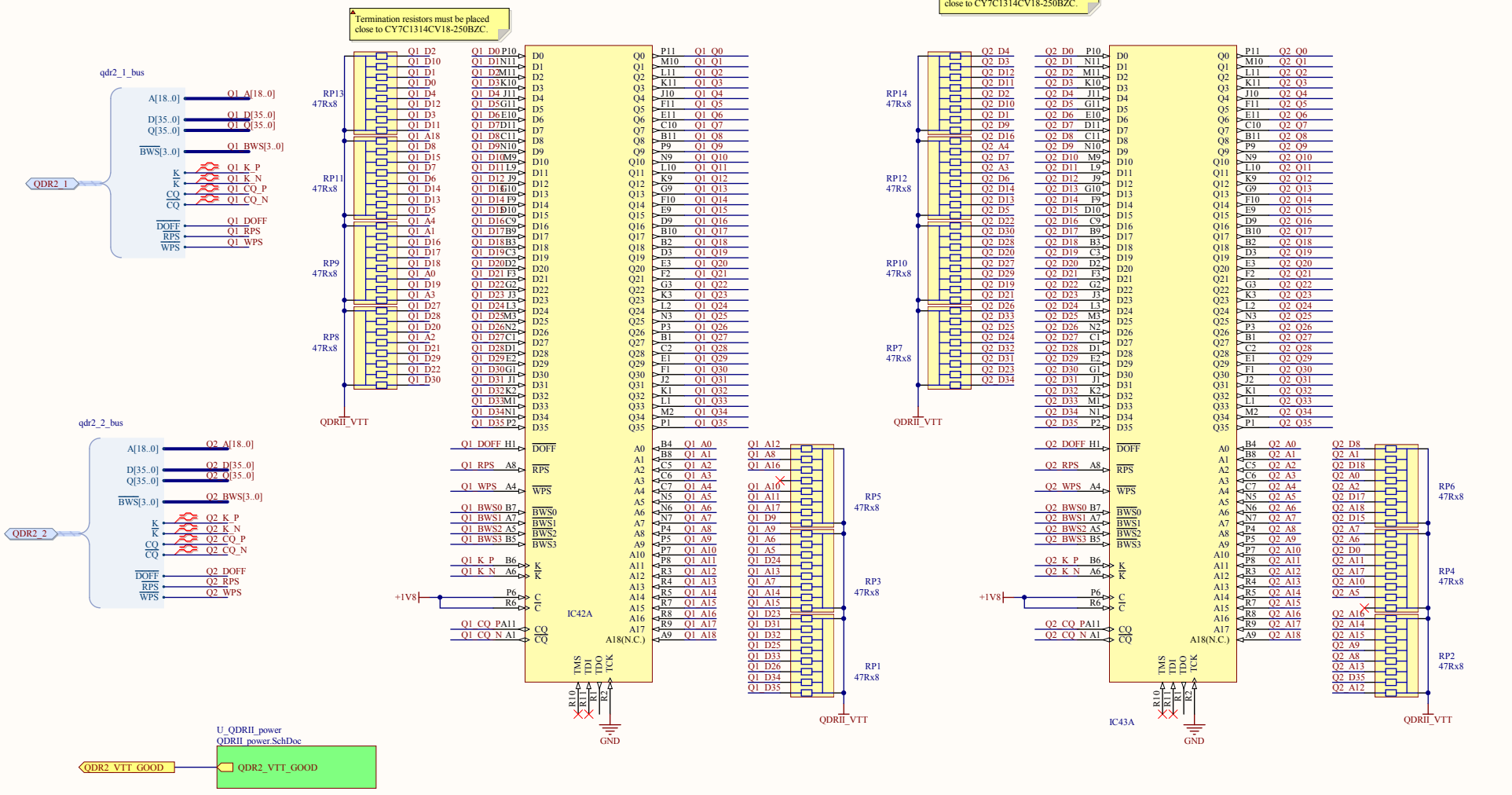
D:\White Rabbit\..\Power_Supply.SchDoc
Drawn By:



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Size: A3	Number	Revision
Date: 10/04/2012		Sheet of
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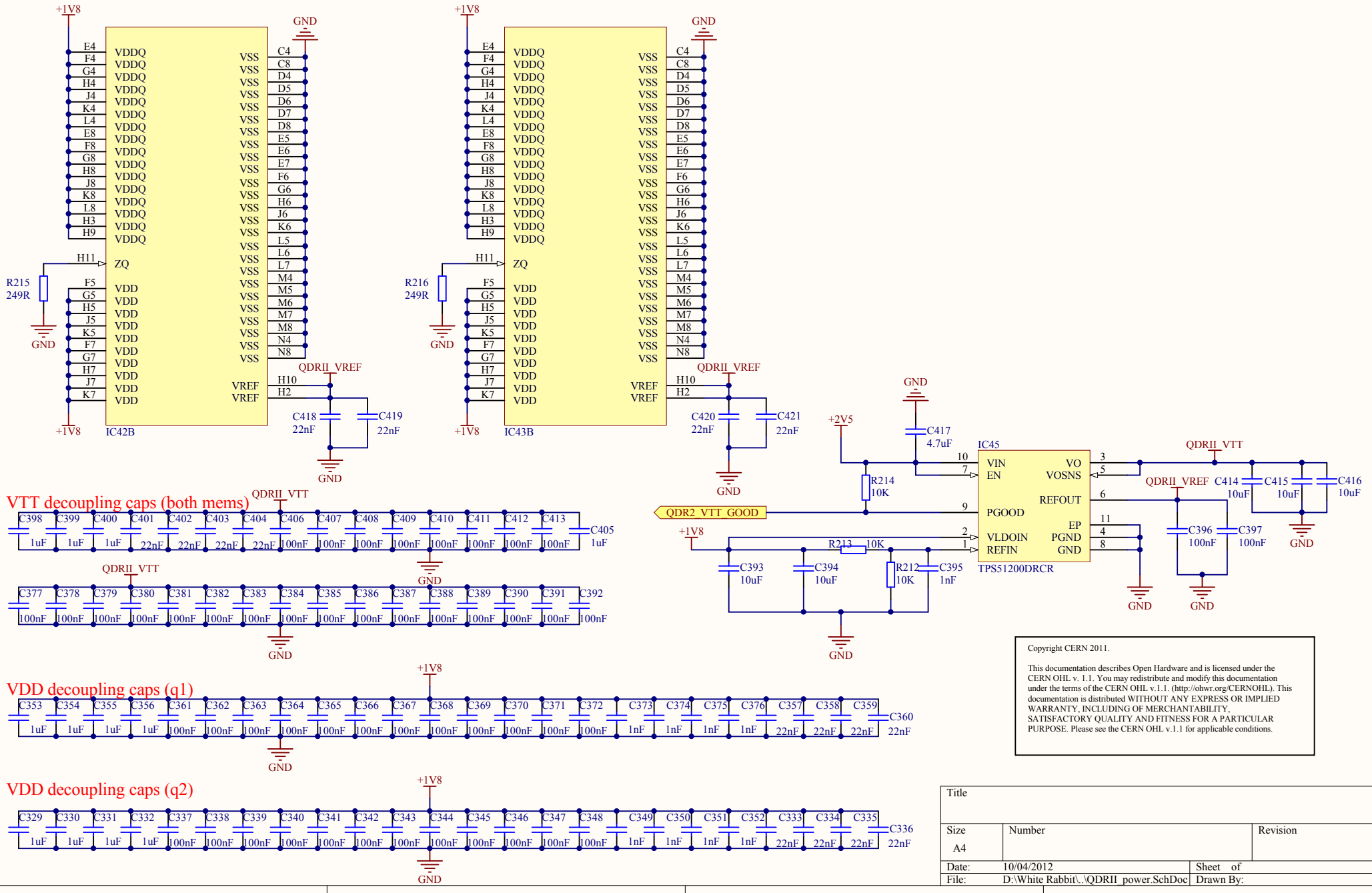

Title		
Size A4	Number	Revision
Date: 10/04/2012		Sheet of
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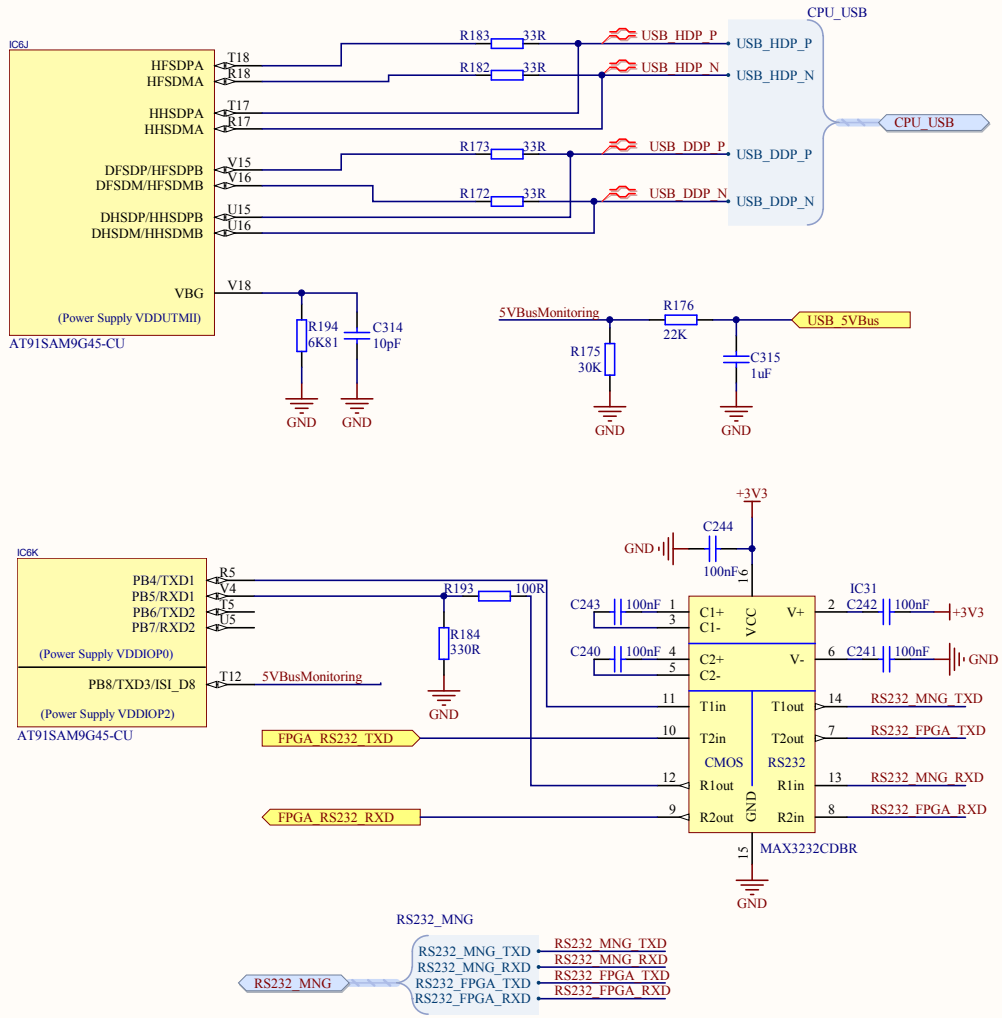
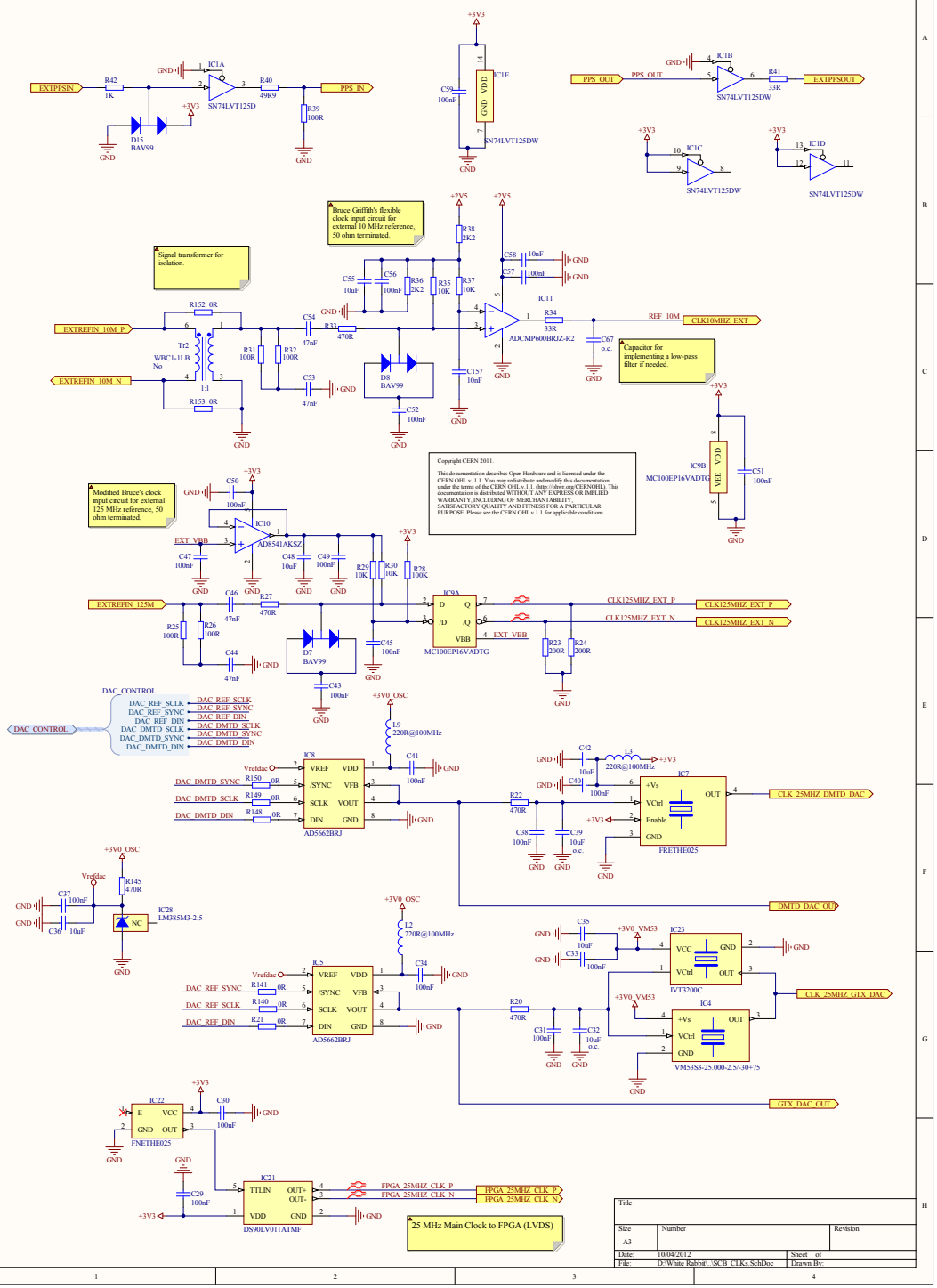


Title	White Rabbit Switch MCH - clocking mezzanine RS232 port	
Size: A	Number:	Revision:
Date: 10/04/2012	Sheet of	
File: D:\White Rabbit\..\RS232_and_USB_ports.SchDoc	Drawn By:	


EXTPPSIN
PPS_IN
SN74LVT125D
SN74LVT125DW
PPS_OUT
EXTPPSOUT
Bruce Griffith's flexible clock input circuit for external 10 MHz reference, 50 ohm terminated.
Signal transformer for isolation.
EXTREFIN_10M_P
EXTREFIN_10M_N
REF_10M
CLK10MHZ_EXT
ADCMP600BRJZ-R2
Capacitor for implementing a low-pass filter if needed.
MC100EP16VADTG
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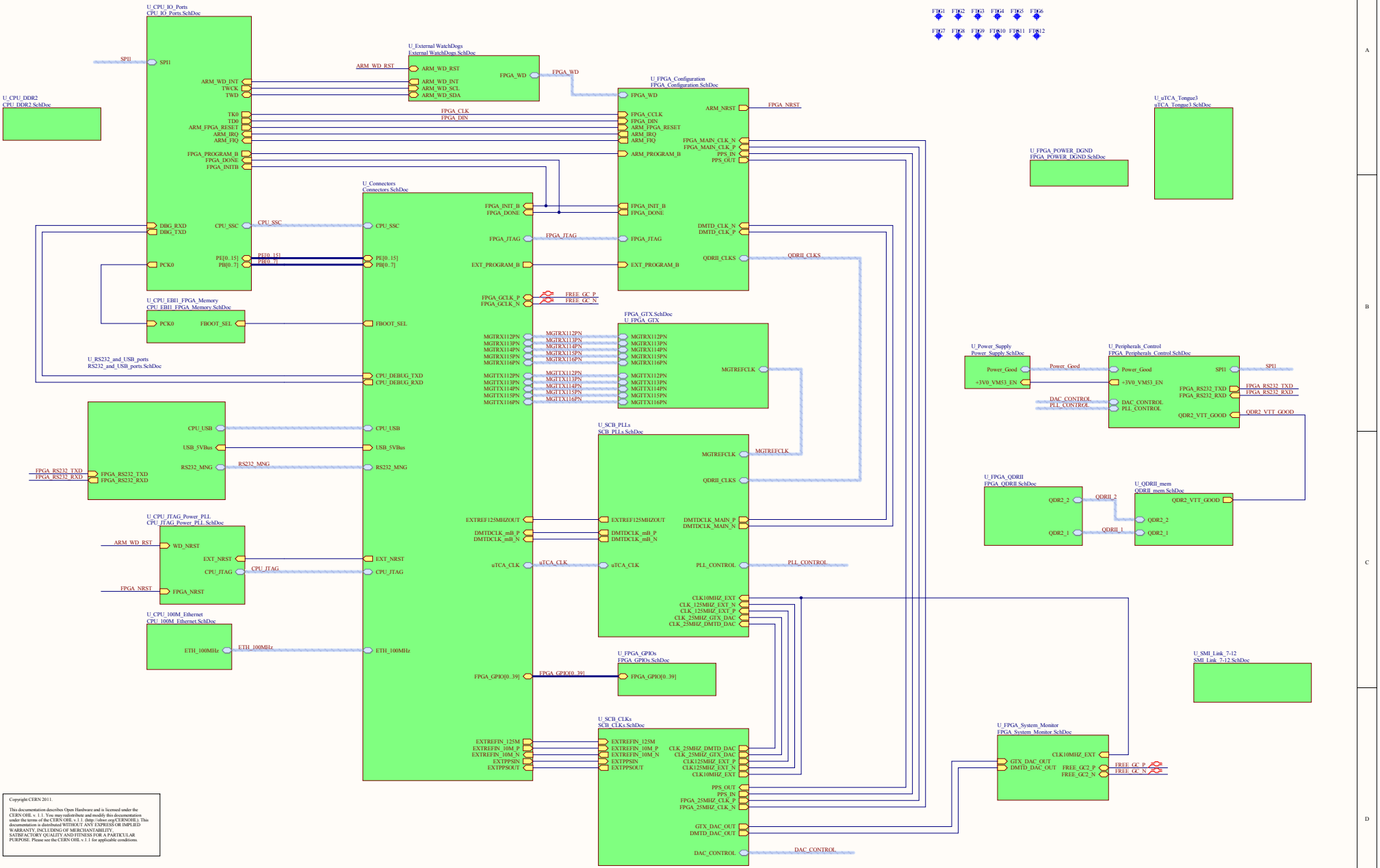
Modified Bruce's clock input circuit for external 125 MHz reference, 50 ohm terminated.
EXTREFIN_125M
CLK125MHZ_EXT_P
CLK125MHZ_EXT_N
DAC_CONTROL
DAC_REF_SCLK
DAC_REF_SYNC
DAC_REF_DIN
DAC_DMTD_SCLK
DAC_DMTD_SYNC
DAC_DMTD_DIN
AD5662BRJ
FRETHE025
CLK_25MHZ_DMTD_DAC
DMTD_DAC_OUT
IVT3200C
CLK_25MHZ_GTX_DAC
VM53S3-25.000-2.5/-30+75
GTX_DAC_OUT
FNETHE025
DS90LV011ATMF
FPGA_25MHZ_CLK_P
FPGA_25MHZ_CLK_N
25 MHz Main Clock to FPGA (LVDS)
Title
Size
A3
Number
Revision
Date:
10/04/2012
Sheet of
File:
D:\White Rabbit\..\SCB_CLKs.SchDoc
Drawn By:


U_CPU_IO_Ports
CPU_IO_Ports.SchDoc
SPI1
ARM_WD_INT
TWCK
TWD
TDI
ARM_FPGA_RESET
ARM_IRQ
ARM_FIQ
FPGA_PROGRAM_B
FPGA_DONE
FPGA_INITB
DBG_RXD
DBG_TXD
CPU_SSC
PE[0..15]
PB[0..7]
PCK0
U_CPU_DDR2
CPU_DDR2.SchDoc
U_CPU_EBI1_FPGA_Memory
CPU_EBI1_FPGA_Memory.SchDoc
FBOOT_SEL
U_RS232_and_USB_ports
RS232_and_USB_ports.SchDoc
CPU_USB
USB_5VBus
RS232_MNG
FPGA_RS232_TXD
FPGA_RS232_RXD
U_CPU_JTAG_Power_PLL
CPU_JTAG_Power_PLL.SchDoc
ARM_WD_RST
WD_NRST
EXT_NRST
CPU_JTAG
FPGA_NRST
U_CPU_100M_Ethernet
CPU_100M_Ethernet.SchDoc
ETH_100MHz
U_External WatchDogs
External_WatchDogs.SchDoc
FPGA_WD
ARM_WD_SCL
ARM_WD_SDA
FPGA_CLK
FPGA_DIN
U_Connectors
Connectors.SchDoc
FPGA_INIT_B
FPGA_JTAG
EXT_PROGRAM_B
FPGA_GCLK_P
FPGA_GCLK_N
FREE_GC_P
FREE_GC_N
MGTRX112PN
MGTRX113PN
MGTRX114PN
MGTRX115PN
MGTRX116PN
MGTTX112PN
MGTTX113PN
MGTTX114PN
MGTTX115PN
MGTTX116PN
FPGA_GPIO[0..39]
EXTREFIN_125M
EXTREFIN_10M_P
EXTREFIN_10M_N
EXTPPSIN
EXTPPSOUT
U_FPGA_Configuration
FPGA_Configuration.SchDoc
FPGA_CCLK
ARM_FPGA_RESET
ARM_PROGRAM_B
FPGA_NRST
FPGA_MAIN_CLK_N
FPGA_MAIN_CLK_P
PPS_IN
PPS_OUT
DMTD_CLK_N
DMTD_CLK_P
QDRII_CLKS
FPGA_GTX.SchDoc
U_FPGA_GTX
MGTREFCLK
U_SCB_PLLs
SCB_PLLs.SchDoc
EXTREF125MHZOUT
DMTDCLK_mB_P
DMTDCLK_mB_N
DMTDCLK_MAIN_P
DMTDCLK_MAIN_N
uTCA_CLK
PLL_CONTROL
CLK10MHZ_EXT
CLK_125MHZ_EXT_N
CLK_125MHZ_EXT_P
CLK_25MHZ_GTX_DAC
CLK_25MHZ_DMTD_DAC
U_FPGA_GPIOs
FPGA_GPIOs.SchDoc
U_SCB_CLKs
SCB_CLKs.SchDoc
PPS_OUT
PPS_IN
FPGA_25MHZ_CLK_P
FPGA_25MHZ_CLK_N
GTX_DAC_OUT
DMTD_DAC_OUT
DAC_CONTROL
U_FPGA_POWER_DGND
FPGA_POWER_DGND.SchDoc
U_uTCA_Tongue3
uTCA_Tongue3.SchDoc
U_Power_Supply
Power_Supply.SchDoc
Power_Good
+3V0_VM53_EN
U_Peripherals_Control
FPGA_Peripherals_Control.SchDoc
SPI1
FPGA_RS232_TXD
FPGA_RS232_RXD
DAC_CONTROL
PLL_CONTROL
QDR2_VTT_GOOD
U_FPGA_QDRII
FPGA_QDRII.SchDoc
QDR2_2
QDR2_1
QDRII_2
QDRII_1
U_QDRII_mem
QDRII_mem.SchDoc
U_FPGA_System_Monitor
FPGA_System_Monitor.SchDoc
U_SMI_Link_7-12
SMI_Link_7-12.SchDoc
FTR1
FTR2
FTR3
FTR4
FTR5
FTR6
FTR7
FTR8
FTR9
FTR10
FTR11
FTR12
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A2
Number
Revision
Date: 10/04/2012
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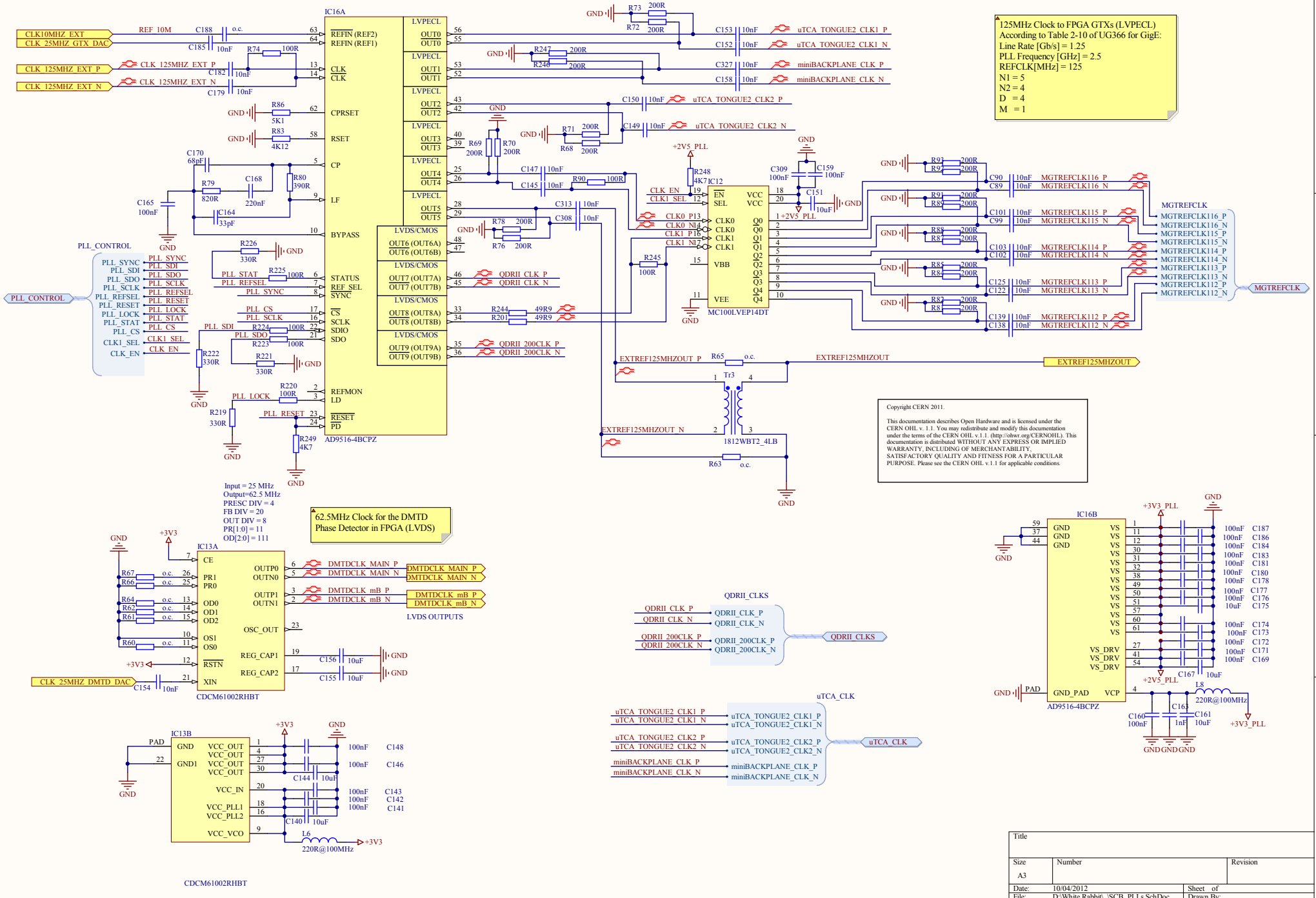
125MHz Clock to FPGA GTXs (LVPECL)
According to Table 2-10 of UG366 for GigE:
Line Rate [Gb/s] = 1.25
PLL Frequency [GHz] = 2.5
REFCLK[MHz] = 125
N1 = 5
N2 = 4
D = 4
M = 1
IC16A
AD9516-4BCPZ
PLL_CONTROL
Input = 25 MHz
Output=62.5 MHz
PRESC DIV = 4
FB DIV = 20
OUT DIV = 8
PR[1:0] = 11
OD[2:0] = 111
62.5MHz Clock for the DMTD Phase Detector in FPGA (LVDS)
IC13A
CDCM61002RHBT
LVDS OUTPUTS
IC13B
CDCM61002RHBT
IC12
MC100LVEP14DT
1812WBT2_4LB
IC16B
AD9516-4BCPZ
QDRII_CLKS
uTCA_CLK
MGTREFCLK
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Revision
Date: 10/04/2012
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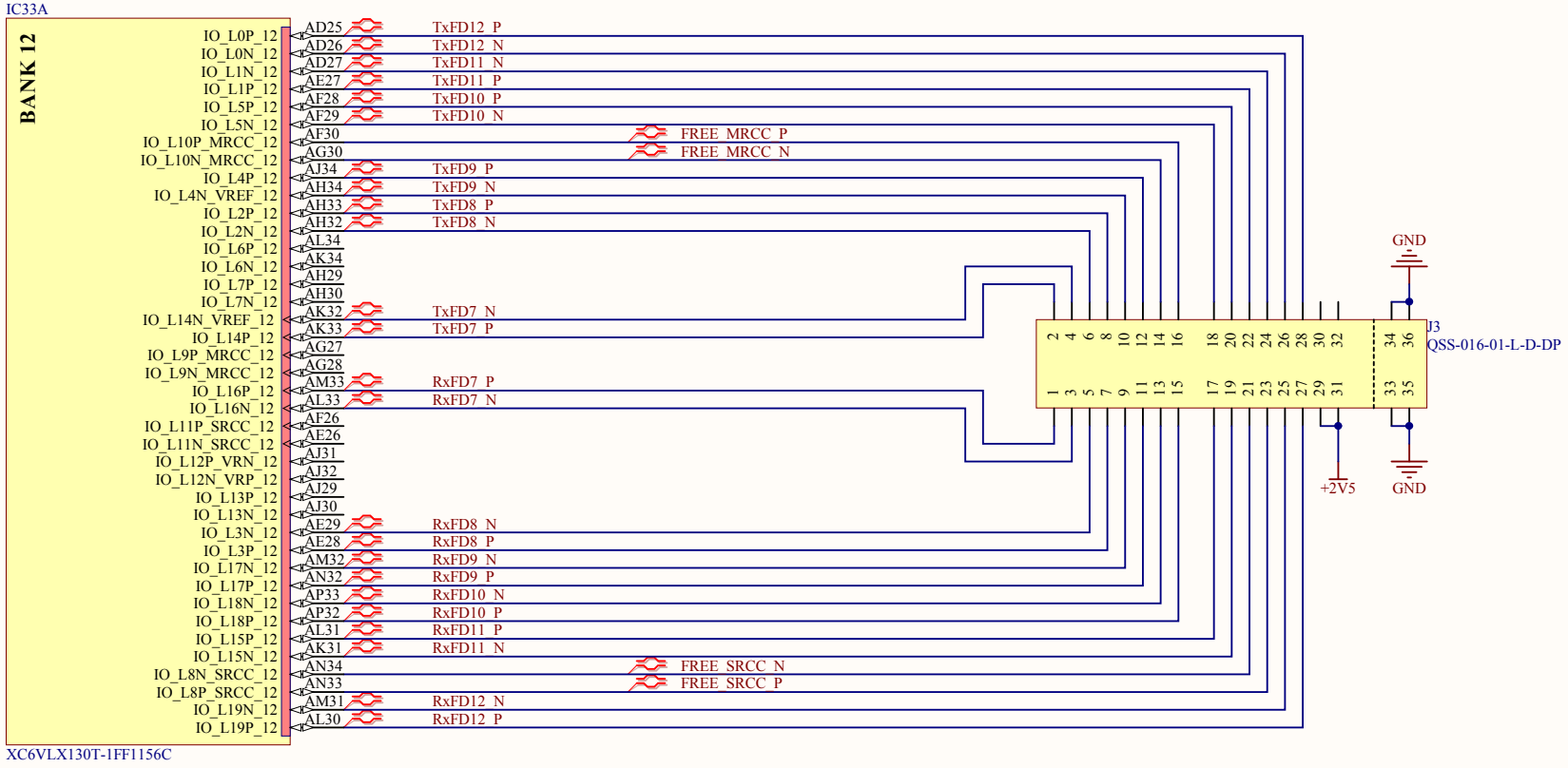

Title		
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File: D:\White Rabbit\..\SMI_Link_7-12.SchDoc	Drawn By:	

SMI links 1-6 -> fabric E

CN4C

77	TxFE-6+	RxFE-6+	94
78	TxFE-6-	RxFE-6-	93
65	TxFE-5+	RxFE-5+	106
66	TxFE-5-	RxFE-5-	105
53	TxFE-4+	RxFE-4+	118
54	TxFE-4-	RxFE-4-	117
41	TxFE-3+	RxFE-3+	130
42	TxFE-3-	RxFE-3-	129
29	TxFE-2+	RxFE-2+	142
30	TxFE-2-	RxFE-2-	141
17	TxFE-1+	RxFE-1+	154
18	TxFE-1-	RxFE-1-	153

UTCA_MCH_TONGUE3

SMI links 1-6 -> fabric D

CN4A

TxFD6_P	74	TxFD-6+	RxFD-6+	97	RxFD6_P
TxFD6_N	75	TxFD-6-	RxFD-6-	96	RxFD6_N
TxFD5_P	62	TxFD-5+	RxFD-5+	109	RxFD5_P
TxFD5_N	63	TxFD-5-	RxFD-5-	108	RxFD5_N
TxFD4_P	50	TxFD-4+	RxFD-4+	121	RxFD4_P
TxFD4_N	51	TxFD-4-	RxFD-4-	120	RxFD4_N
TxFD3_P	38	TxFD-3+	RxFD-3+	133	RxFD3_P
TxFD3_N	39	TxFD-3-	RxFD-3-	132	RxFD3_N
TxFD2_P	26	TxFD-2+	RxFD-2+	145	RxFD2_P
TxFD2_N	27	TxFD-2-	RxFD-2-	144	RxFD2_N
TxFD1_P	14	TxFD-1+	RxFD-1+	157	RxFD1_P
TxFD1_N	15	TxFD-1-	RxFD-1-	156	RxFD1_N

UTCA_MCH_TONGUE3

IC33C

BANK 14

IO_L18P_14	W25		TxFD6_P
IO_L18N_14	Y25		TxFD6_N
IO_L19P_14	W27		TxFD5_P
IO_L19N_14	W26		TxFD5_N
IO_L15P_14	Y29		TxFD4_P
IO_L15N_14	Y29		TxFD4_N
IO_L5P_14	T26		TxFD3_P
IO_L5N_14	T27		TxFD3_N
IO_L1P_14	T28		TxFD2_P
IO_L1N_14	T29		TxFD2_N
IO_L4P_14	U33		TxFD1_P
IO_L4N_VREF_14	U34		TxFD1_N
IO_L6P_14	U33		
IO_L6N_14	U32		
IO_L7P_14	U28		
IO_L7N_14	V29		
IO_L8P_SRCC_14	U31		
IO_L8N_SRCC_14	U30		
IO_L9P_MRCC_14	T30		
IO_L9N_MRCC_14	W30		
IO_L10P_MRCC_14	V34		
IO_L10N_MRCC_14	W34		
IO_L11P_SRCC_14	V28		
IO_L11N_SRCC_14	V27		
IO_L12P_VRN_14	V32		
IO_L12N_VRP_14	V33		
IO_L13P_14	T32		
IO_L13N_14	T31		
IO_L0P_14	Y25		RxFD6_P
IO_L0N_14	Y25		RxFD6_N
IO_L17P_14	V28		RxFD5_P
IO_L17N_14	V27		RxFD5_N
IO_L14P_14	T33		RxFD4_P
IO_L14N_VREF_14	T34		RxFD4_N
IO_L16P_14	W31		RxFD3_P
IO_L16N_14	W32		RxFD3_N
IO_L3P_14	T30		RxFD2_P
IO_L3N_14	T31		RxFD2_N
IO_L2P_14	R33		RxFD1_P
IO_L2N_14	R34		RxFD1_N

XC6VLX130T-1FF1156C

CN4B

2	RSVD	GND	86
3	RSVD	GND	89
5	RSVD	GND	92
6	RSVD	GND	95
169	RSVD	GND	98
168	RSVD	GND	101
166	RSVD	GND	104
165	RSVD	GND	107
		GND	110
1	GND	GND	113
4	GND	GND	116
7	GND	GND	119
10	GND	GND	122
13	GND	GND	125
16	GND	GND	128
19	GND	GND	131
22	GND	GND	134
25	GND	GND	137
28	GND	GND	140
31	GND	GND	143
34	GND	GND	146
37	GND	GND	149
40	GND	GND	152
43	GND	GND	155
46	GND	GND	158
49	GND	GND	161
52	GND	GND	164
55	GND	GND	167
58	GND	GND	170
61	GND	GND	85
64	GND	GND	82
67	GND	GND	79
70	GND	GND	76
73	GND		

UTCA_MCH_TONGUE3

GND

Title		
Size: A4	Number	Revision
Date: 10/04/2012		Sheet of
File: D:\White Rabbit\..\uTCA_Tongue3.SchDoc		Drawn By: