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Last note: Resistors must be placed close to the PLL. If not possible, we should resort to single 300R and 36R resistors.

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Place on a thermal-insulated PCB area, with vibration damper and screening box.
Banks 15 and 16 powered with VCCO=3.3V.

Banks 12, 13 and 14 powered with VCCO=3.3V.

Bank 0 powered with VCCO=3.3V.
Layout note: make sure MGT_R_REF is also used to set the direction of the external (100ohm) parallel resistor.

All inputs are NOT externally terminated (DIFF_TERM=FALSE).

All single-ended signals are LVCMOS.

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- FPGA: Configuration -

WR2RF VME Module

Project/Equipment: WR2RF VME Module

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Some 7 series devices require local PCB capacitors because high-frequency ceramic
 capacitors are already present inside the device package (see Table 18 and Table 20 for the package
 subtypes). Table 18 and Table 20 list the package subtypes for 7series and
 Virtex-7 devices. Spartan-6 and Spartan-6 device do not have package
 capacitors.

https://www.xilinx.com/support/documentation/user_guides/ug483_7Series_PCB.pdf
SN74VMEH22501DGGR is able to source 66mA and sink up to 48mA. Supplied from 3.3V delivers still above 3V at 60mA, it means that is able to easily drive 50Ohm load.

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Regulator for AXIOM45ULN-24 OCXO

Default voltage: 11.5V
Startup current: 350 mA
Steady-state current: 150 mA
Voltage setting: 1.4V (internal) + 6.4 V + 3.2V + 0.4 + 0.1 V = 11.5V

OCXO_CURR_SENSE (Volts) = 40*R*(ocxo_current(A))
Startup voltage sense = 0.7V
Steady-state voltage sense = 0.3V
One 100nf for PIN3V3_TRIG_A pin
One 100nf for power current loop
Connect the AGND and PGND pins to thermal pad directly on the same layer

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According to ANSI/VITA 580@100MHz, each power pin should be capable of providing at least 1A of current at 80°C.

Therefore:
- P12V_VME: 1A
- M12V_VME: 1A
- P5V_VME: 3A

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