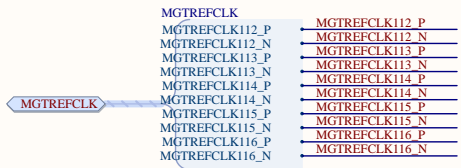


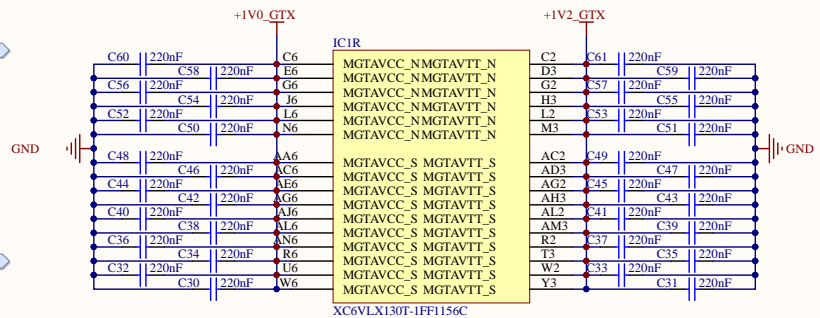
XC6VLX130T-1FF1156C



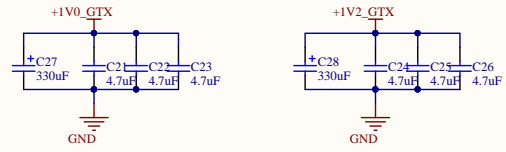
**Power Supply Decoupling Capacitors**

According to Xilinx UG366 (v2.3), page 230, the suggested filtering for the MGTAVCC and MGTAVTT power supplies is:

- One 0.22uF, size 0402, ceramic capacitor per power supply pin
- One 4.7uF, size 0402, ceramic capacitor per two Quads
- One 330uF bulk capacitor for each power supply



XC6VLX130T-1FF1156C



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File name	FPGA_GTX.SchDoc		
Revision	1.1	Organization	Tsinghua University
Project	WRS-FL-HW	Date	2018-3-15

IC1H

BANK 24

IO\_L0P\_GC\_24  
IO\_L0N\_GC\_24  
IO\_L1P\_GC\_24  
IO\_L1N\_GC\_24  
IO\_L2P\_D15\_24  
IO\_L2N\_D14\_24  
IO\_L3P\_D13\_24  
IO\_L3N\_D12\_24  
IO\_L4P\_D11\_24  
IO\_L4N\_VREF\_D10\_24  
IO\_L5P\_D9\_24  
IO\_L5N\_D8\_24  
IO\_L6P\_D7\_24  
IO\_L6N\_D6\_24  
IO\_L7P\_D5\_24  
IO\_L7N\_D4\_24  
IO\_L8P\_SRCC\_24  
IO\_L8N\_SRCC\_24  
IO\_L9P\_MRCC\_24  
IO\_L9N\_MRCC\_24  
IO\_L10P\_MRCC\_24  
IO\_L10N\_MRCC\_24  
IO\_L11P\_SRCC\_24  
IO\_L11N\_SRCC\_24  
IO\_L12P\_D3\_24  
IO\_L12N\_D2\_FS2\_24  
IO\_L13P\_D1\_FS1\_24  
IO\_L13N\_D0\_FS0\_24  
IO\_L14P\_FCS\_B\_24  
IO\_L14N\_VREF\_FOE\_B\_MOSI\_24  
IO\_L15P\_FWE\_B\_24  
IO\_L15N\_RS1\_24  
IO\_L16P\_RS0\_24  
IO\_L16N\_CSO\_B\_24  
IO\_L17P\_VRN\_24  
IO\_L17N\_VRP\_24  
IO\_L18N\_24  
IO\_L19P\_24  
IO\_L19N\_24

XC6VLX130T-1FF1156C

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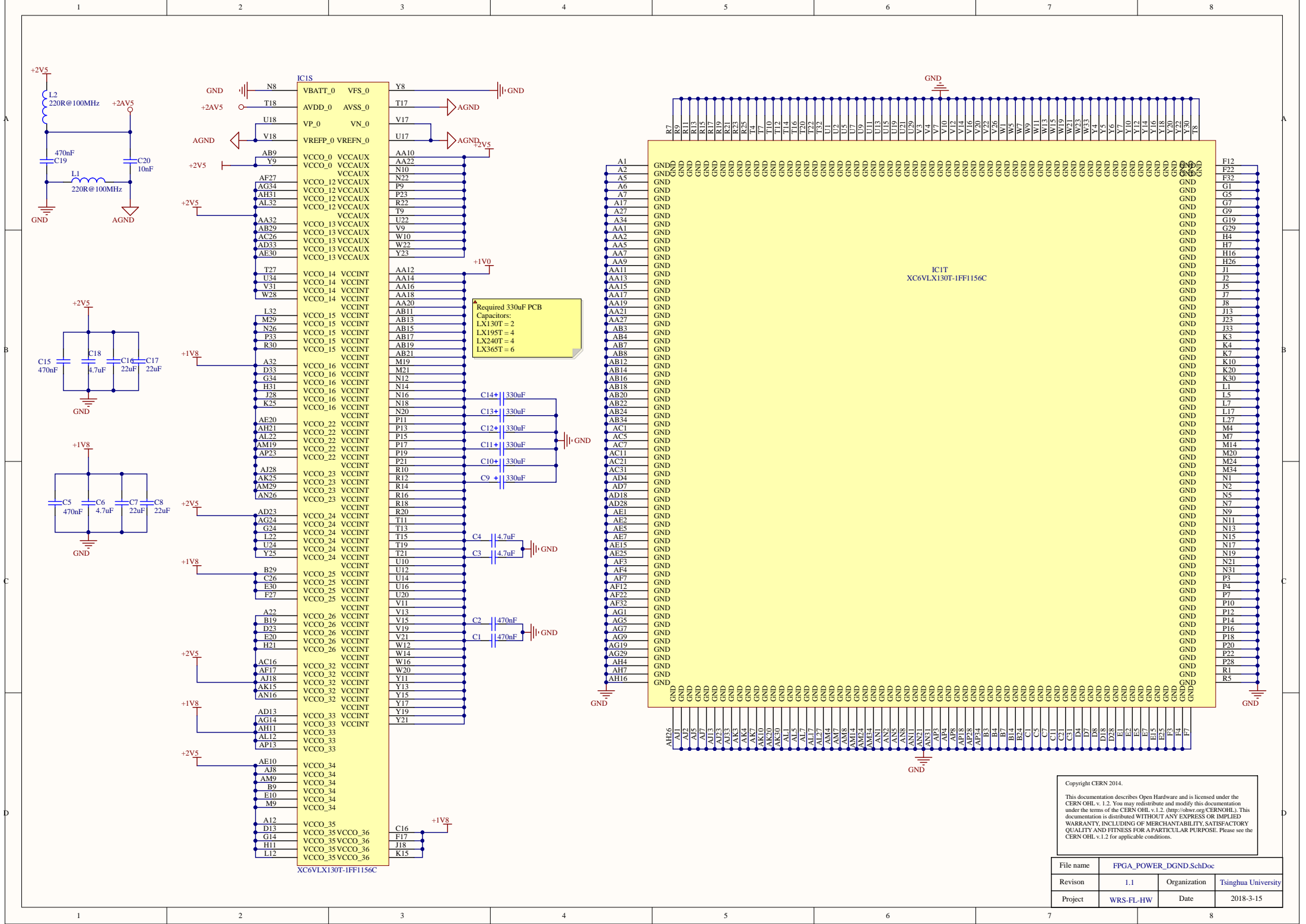
M24

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File name	FPGA_POWER_DGND.SchDoc		
Revision	1.1	Organization	Tsinghua University
Project	WRS-FL-HW	Date	2018-3-15

FPGA\_GPIO[0..39]

FPGA\_GPIO[0..39]

IC1B

FPGA_GPIO0	AF34	IO_L8N_SRCC_13
FPGA_GPIO1	AE33	IO_L10P_MRCC_13
FPGA_GPIO2	AE34	IO_L8P_SRCC_13
FPGA_GPIO3	AD32	IO_L14P_13
FPGA_GPIO4	AD34	IO_L2P_13
FPGA_GPIO5	AC33	IO_L4P_13
FPGA_GPIO6	AC34	IO_L2N_13
FPGA_GPIO7	AB33	IO_L4N_VREF_13
FPGA_GPIO8	AB32	IO_L12P_VRN_13
FPGA_GPIO9	AA34	IO_L0P_13
FPGA_GPIO10	AA33	IO_L0N_13
FPGA_GPIO11	AA31	IO_L1N_13
FPGA_GPIO12	AB30	IO_L3P_13
FPGA_GPIO13	AC30	IO_L9N_MRCC_13
FPGA_GPIO14	AA28	IO_L7P_13
FPGA_GPIO15	AA26	IO_L17P_13
FPGA_GPIO16	AA25	IO_L6P_13
FPGA_GPIO17	AB25	IO_L19P_13
FPGA_GPIO18	AB27	IO_L15P_13
FPGA_GPIO19	AC27	IO_L15N_13
FPGA_GPIO20	AB28	IO_L13P_13
FPGA_GPIO21	AD29	IO_L11P_SRCC_13
FPGA_GPIO22	AE31	IO_L5P_13
FPGA_GPIO23	Y26	IO_L6N_13
FPGA_GPIO24	AA29	IO_L7N_13
FPGA_GPIO25	AA30	IO_L1P_13
FPGA_GPIO26	AB31	IO_L3N_13
FPGA_GPIO27	AC29	IO_L11N_SRCC_13
FPGA_GPIO28	AC32	IO_L12N_VRP_13
FPGA_GPIO29	AD30	IO_L9P_MRCC_13
FPGA_GPIO30	AD31	IO_L5N_13
FPGA_GPIO31	AE32	IO_L14N_VREF_13
FPGA_GPIO32	AF33	IO_L10N_MRCC_13
FPGA_GPIO33	AC28	IO_L13N_13
FPGA_GPIO34	AG33	IO_L16P_13
FPGA_GPIO35	AB26	IO_L17N_13
FPGA_GPIO36	AG32	IO_L16N_13
FPGA_GPIO37	AF31	IO_L18N_13
FPGA_GPIO38	AG31	IO_L18P_13
FPGA_GPIO39	AC25	IO_L19N_13

XC6VLX130T-1FF1156C

BANK 13

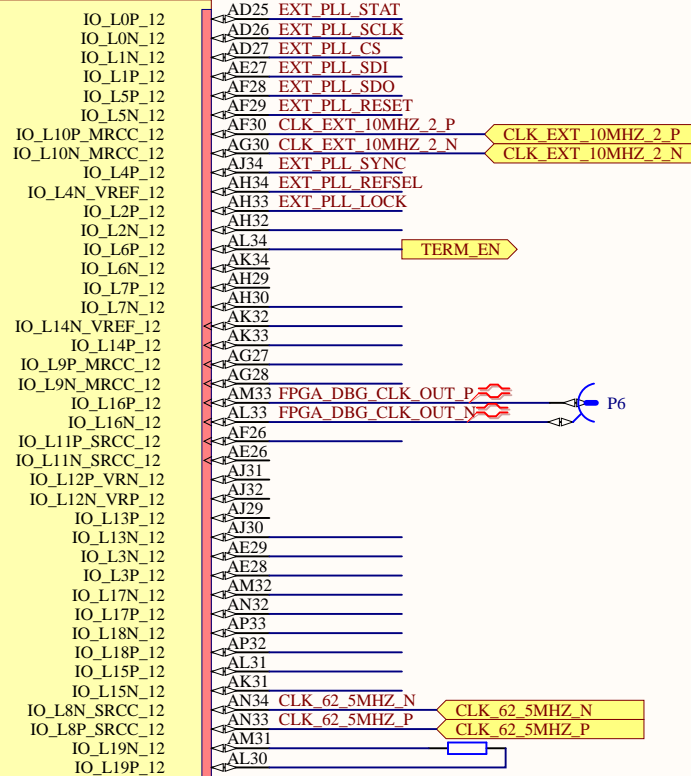
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File name	FPGA_GPIOs.SchDoc		
Revision	1.1	Organization	Tsinghua University
Project	WRS-FL-HW	Date	2018-3-15

IC1A

BANK 12



XC6VLX130T-1FF1156C

R36 100R

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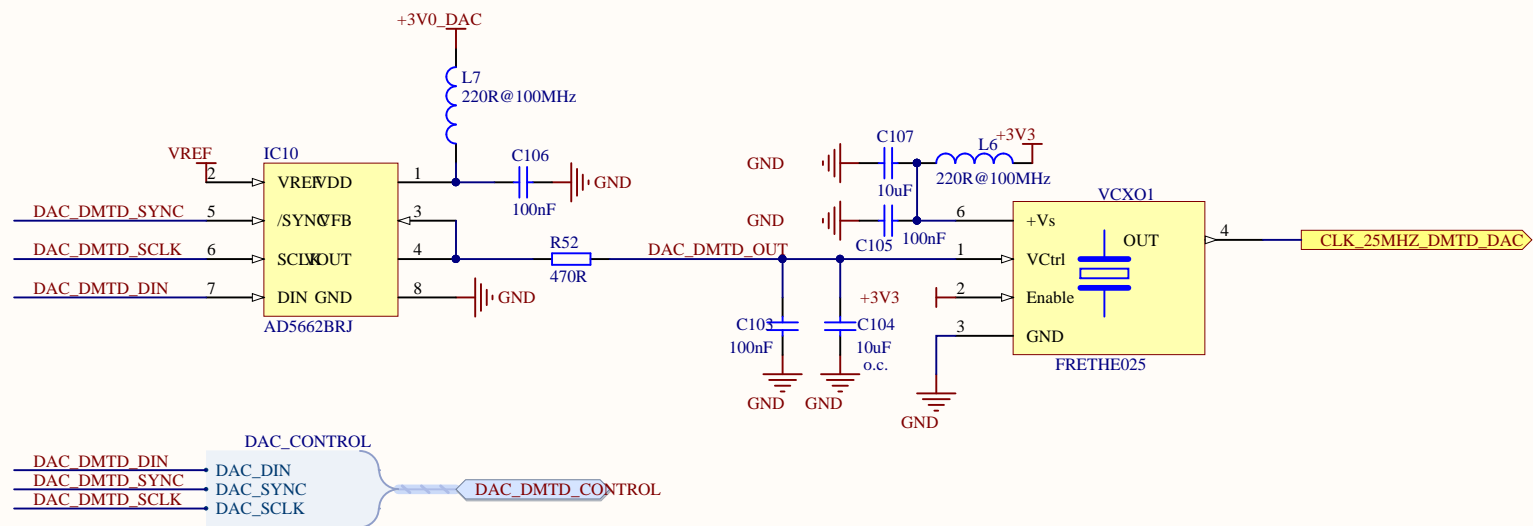
File name	FPGA_EXT_PLL.SchDoc		
Revision	1.1	Organization	Tsinghua University
Project	WRS-FL-HW	Date	2018-3-15







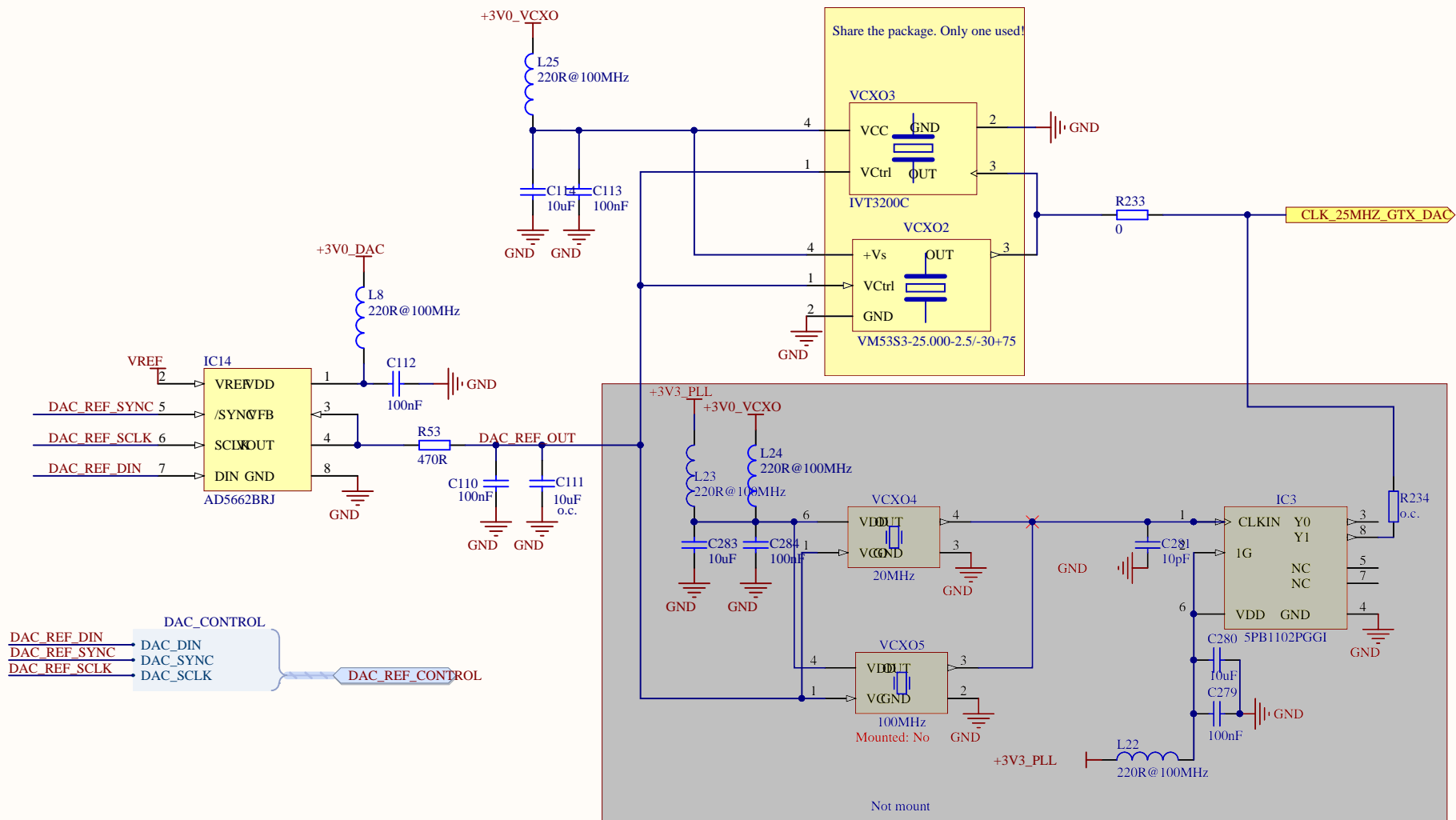




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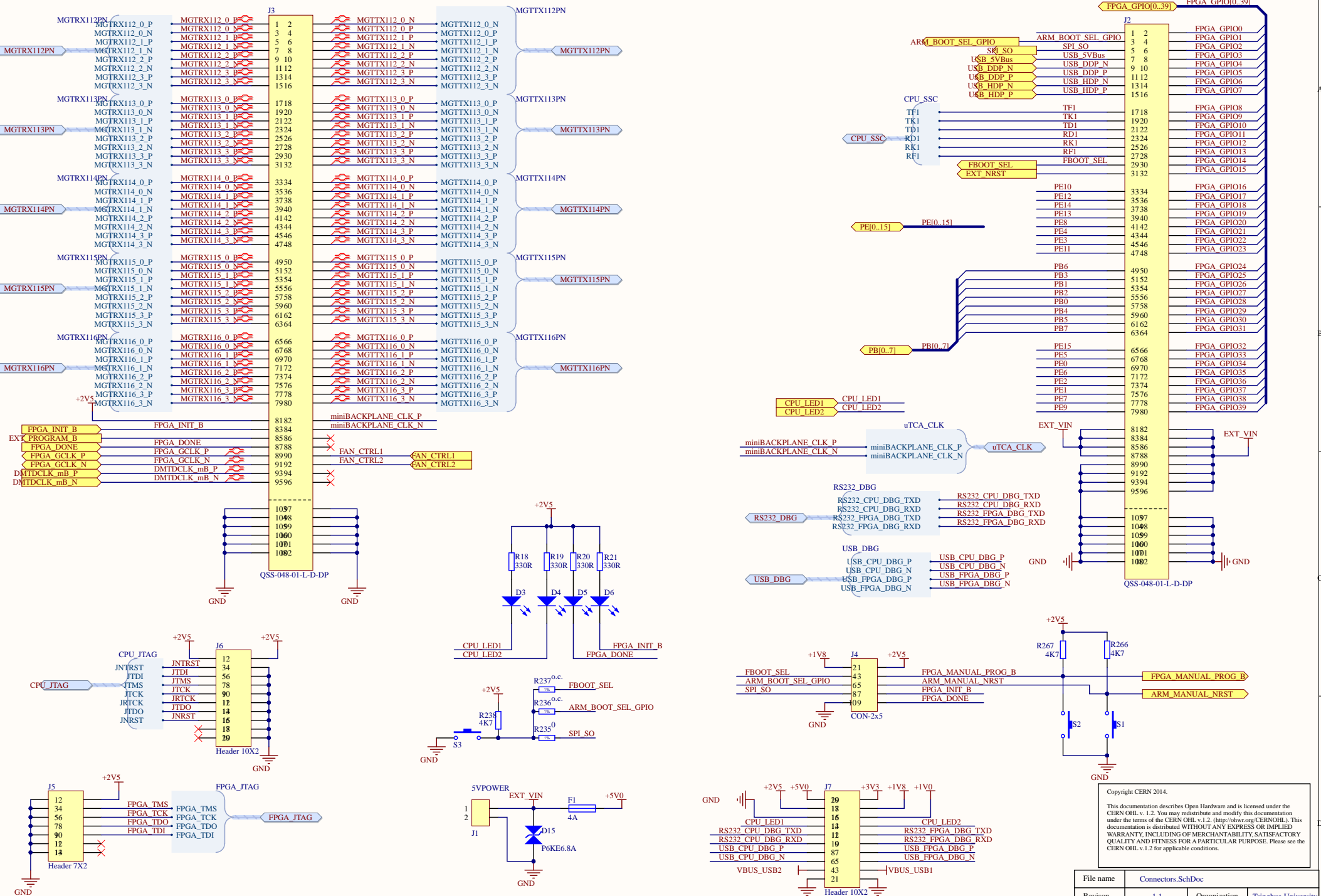
File name	CLK_25M_DMTD.SchDoc		
Revision	1.1	Organization	Tsinghua University
Project	WRS-FL-HW	Date	2018-3-15



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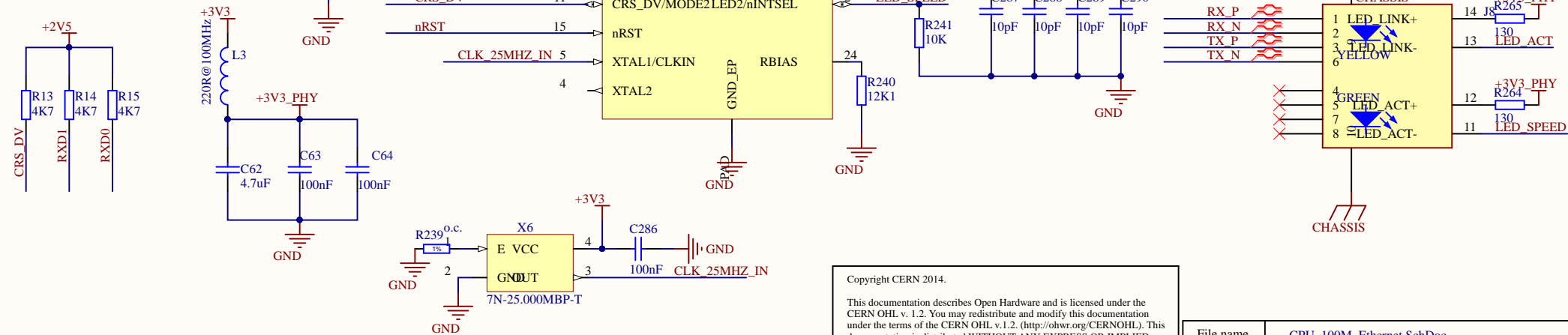
File name	CLK_25M_GTX.SchDoc		
Revision	1.1	Organization	Tsinghua University
Project	WRS-FL-HW	Date	2018-3-15



IC2L

PA10/ETX0  
PA11/ETX1  
PA12/ERX0  
PA13/ERX1  
PA14/ETXEN  
PA15/ERXDV  
PA16/ERXER  
PA17/ETXCK  
PA18/EMDC  
PA19/EMDIO  
  
PA27/MCI1\_DA4/ETXER  
PA28/MCI1\_DA5/ERXCK  
PA29/MCI1\_DA6/ECRS  
PA30/MCI1\_DA7/ECOL  
(Power Supply VDDIOPO)

AT91SAM9G45-CU

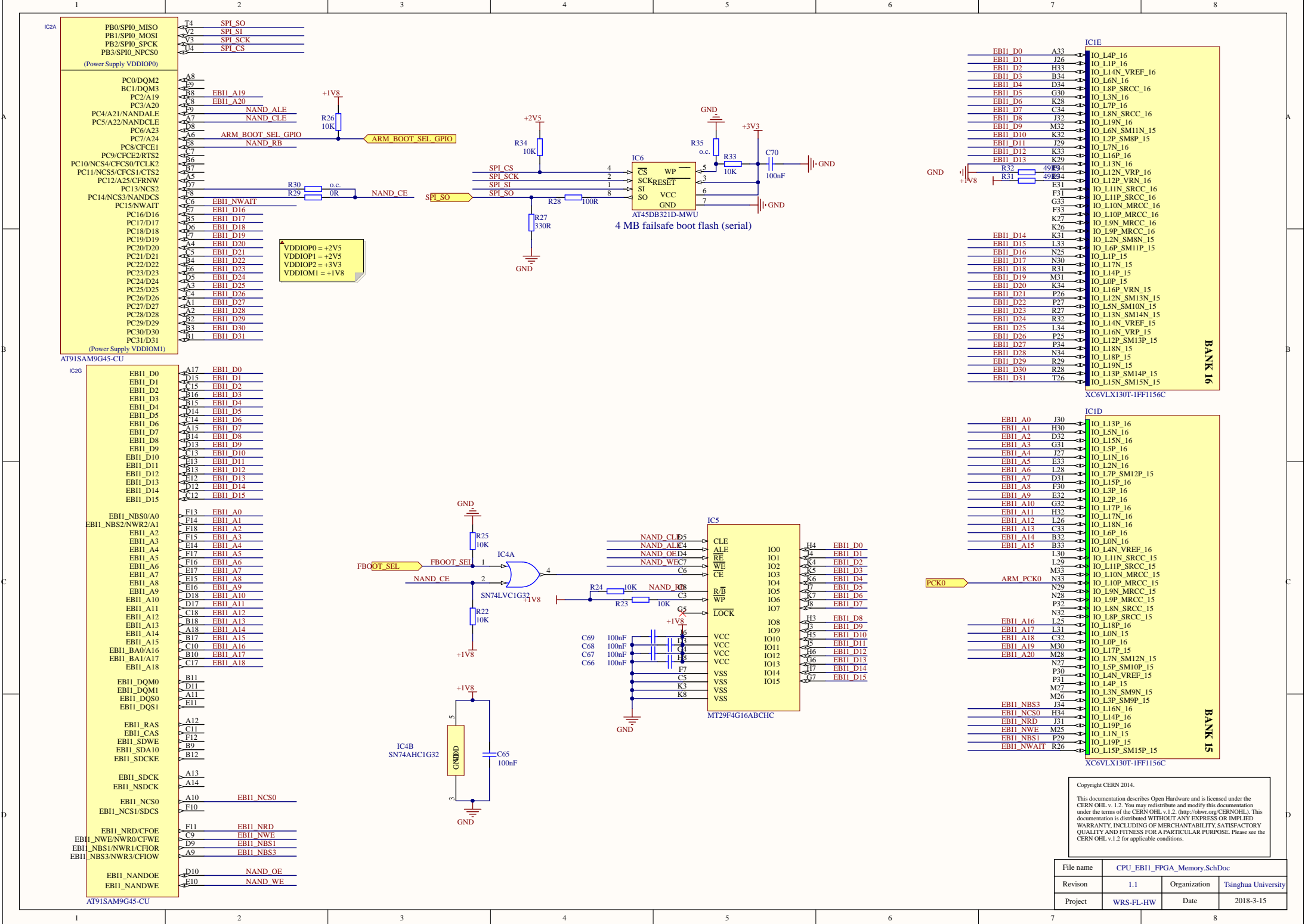


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File name	CPU_100M_Ethernet.SchDoc		
Revision	1.1	Organization	Tsinghua University
Project	WRS-FL-HW	Date	2018-3-15

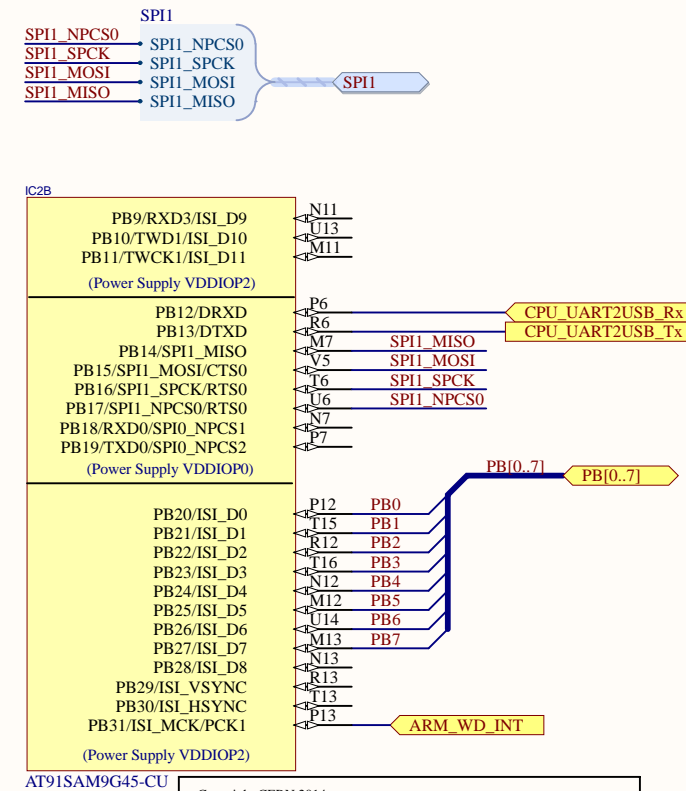
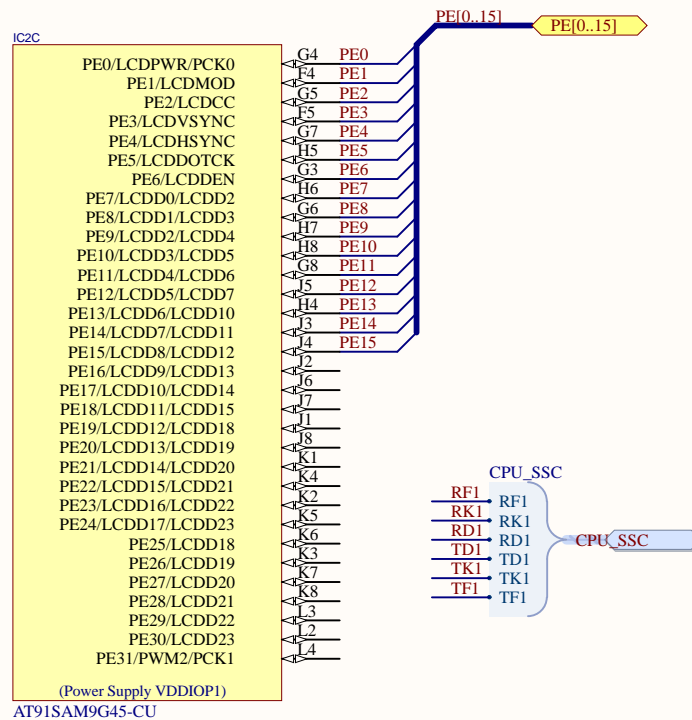
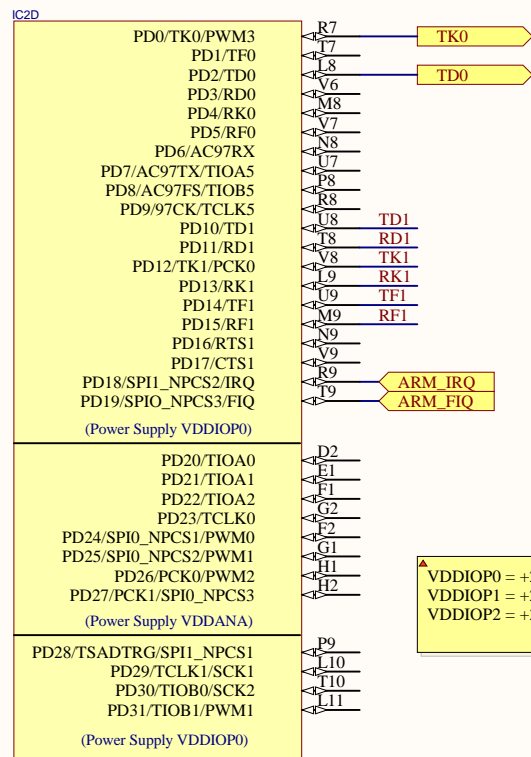
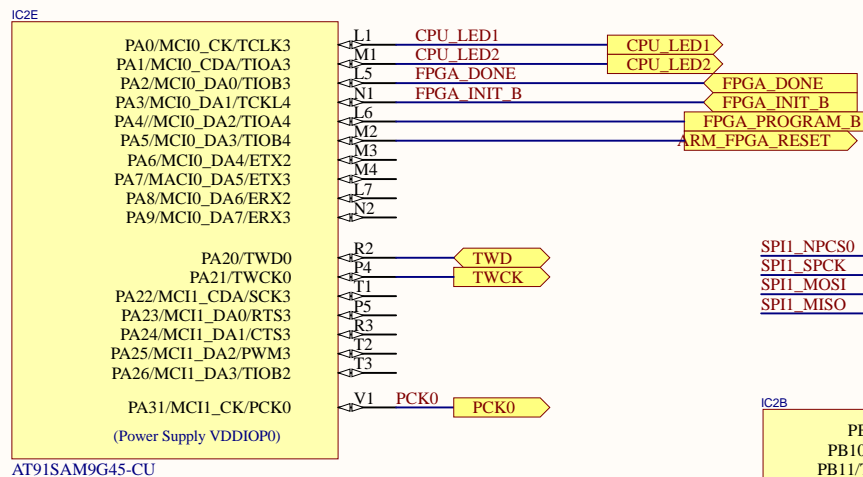
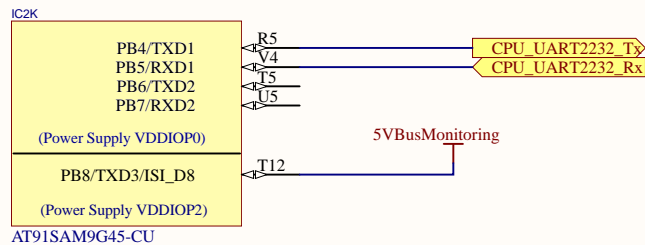




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File name	CPU_EBI1_FPGA_Memory.SchDoc		
Revision	1.1	Organization	Tsinghua University
Project	WRS-FL-HW	Date	2018-3-15

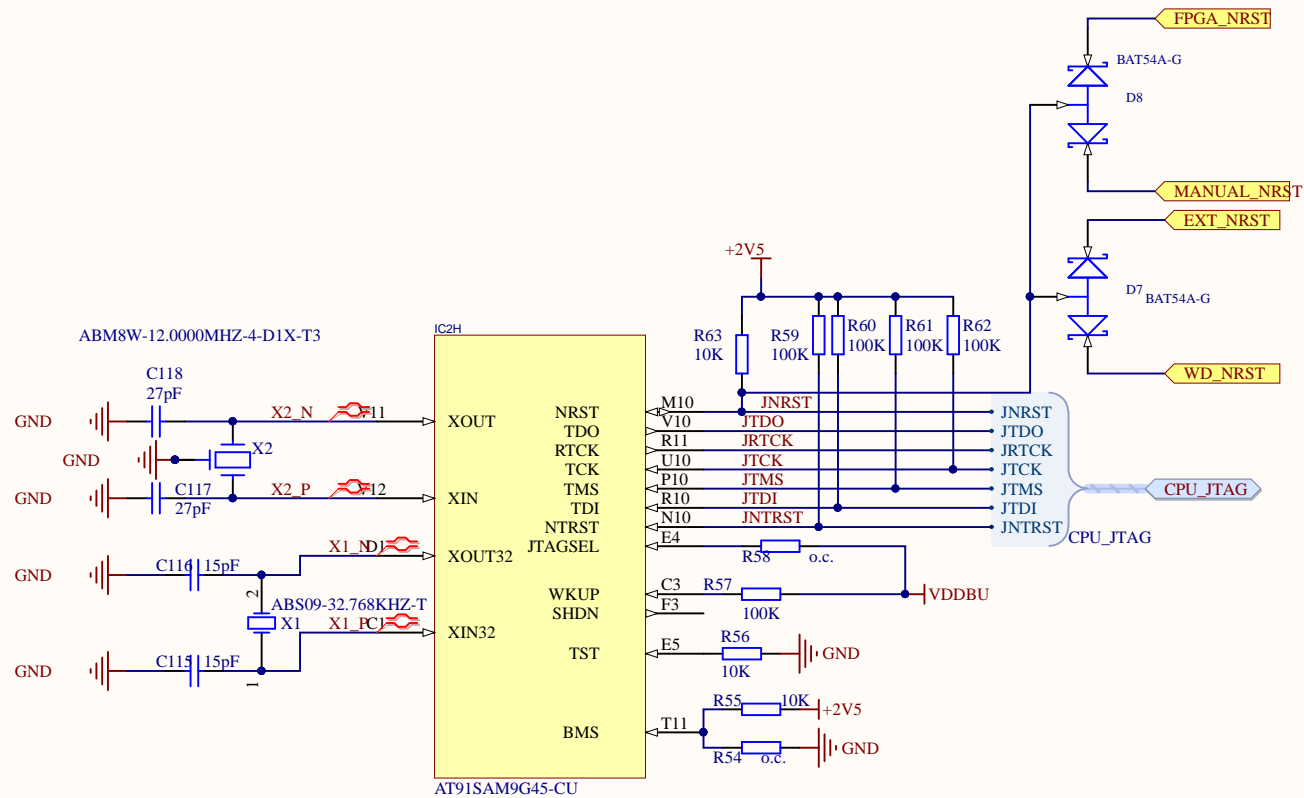


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File name	CPU_IO_Ports.SchDoc		
Revision	1.1	Organization	Tsinghua University
Project	WRS-FL-HW	Date	2018-3-15

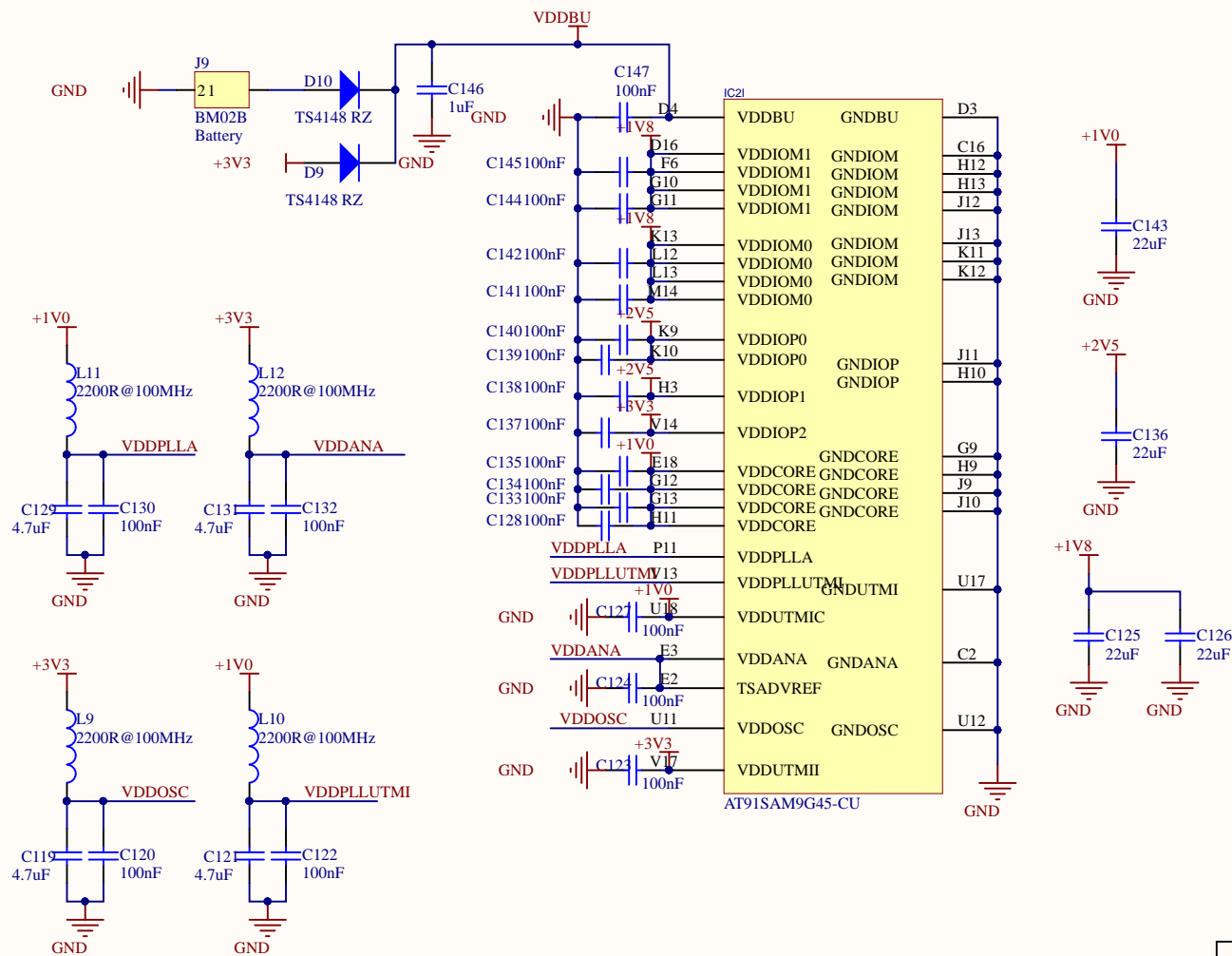




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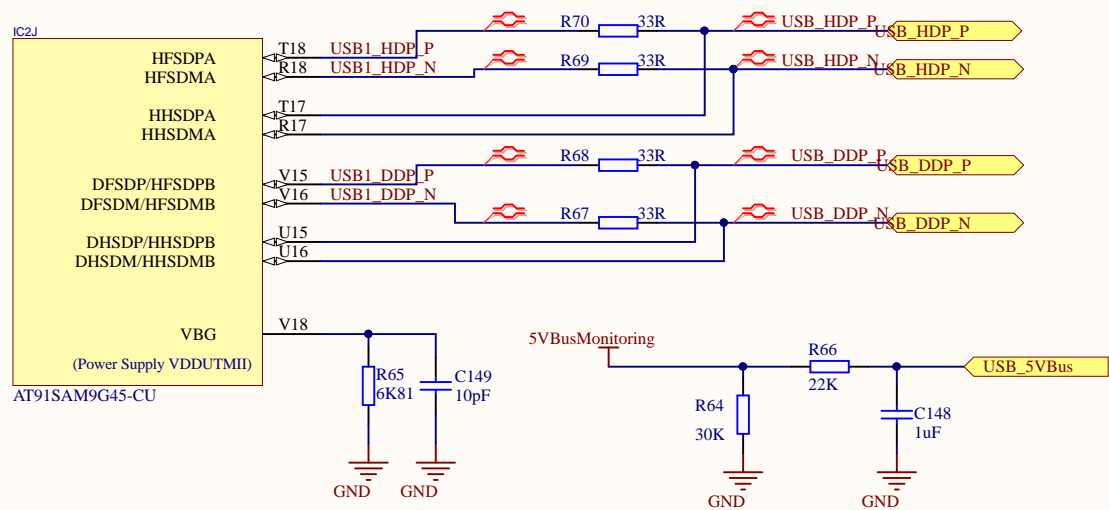
File name	CPU_JTAG.SchDoc		
Revision	1.1	Organization	Tsinghua University
Project	White Rabbit	Date	2018-3-15



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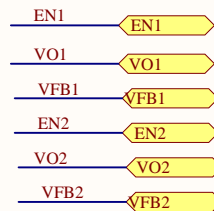
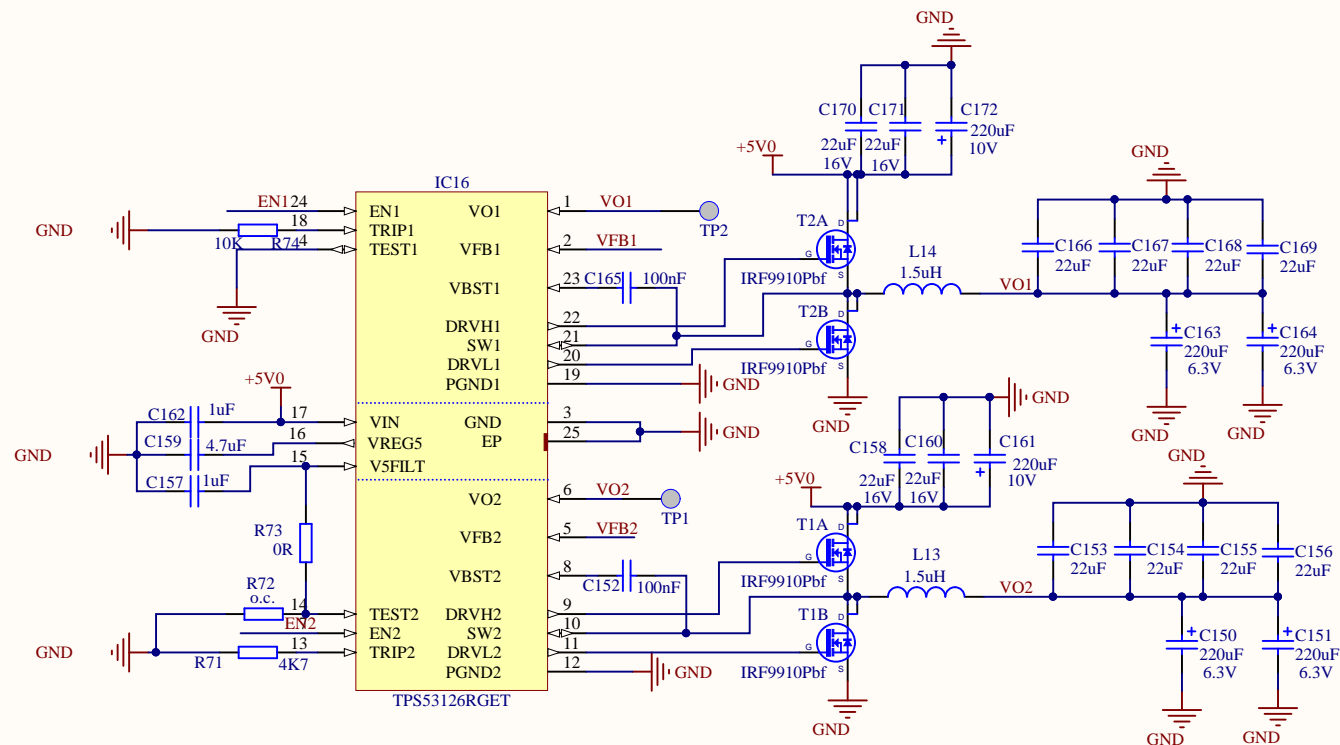
File name	CPU_POWER.SchDoc		
Revision	1.1	Organization	Tsinghua University
Project	White Rabbit	Date	2018-3-15



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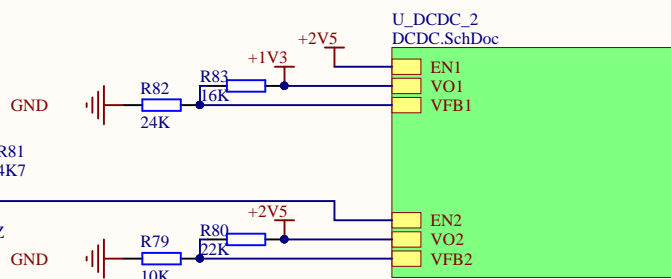
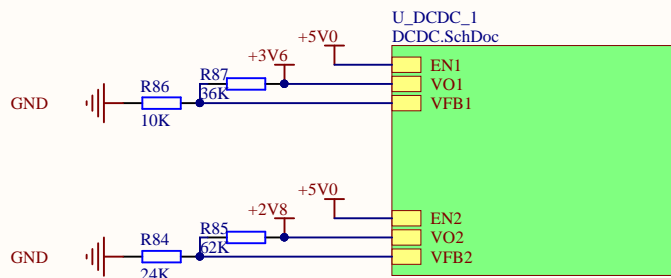
File name	CPU_USB.SchDoc		
Revision	1.1	Organization	Tsinghua University
Project	White Rabbit	Date	2018-3-15



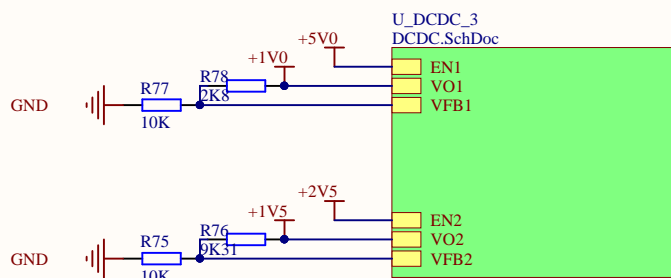
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File name	DCDC.SchDoc		
Revision	1.1	Organization	Tsinghua University
Project	WRS-FL-HW	Date	2018-3-15



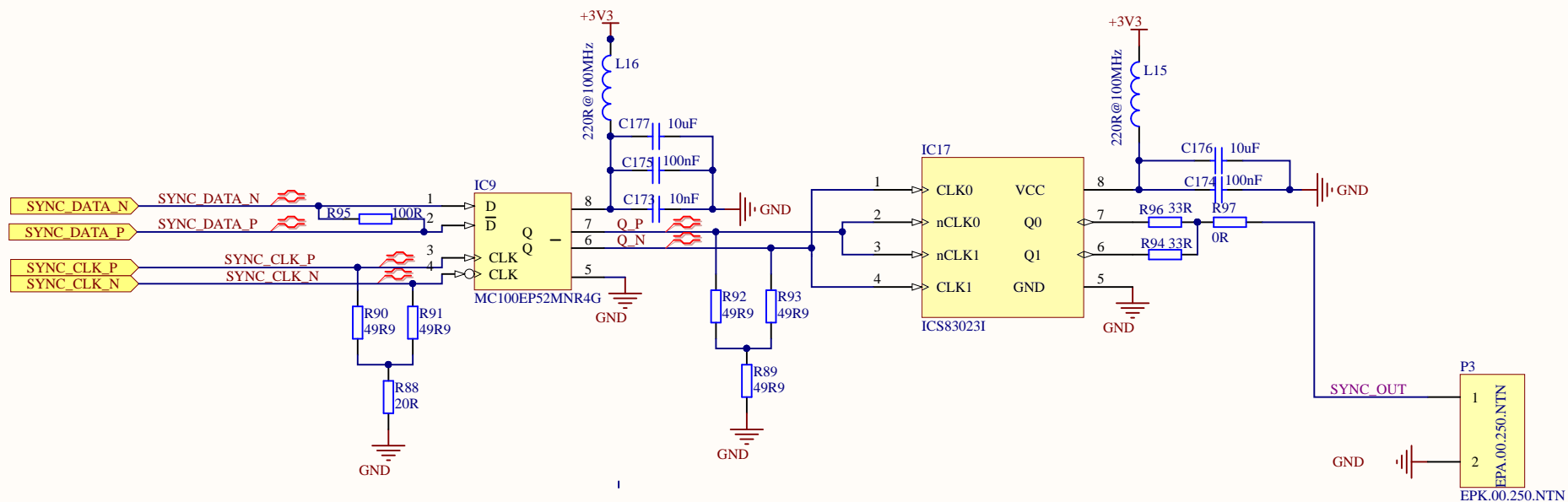
The voltage threshold of EN is 2.0V, the Vf-max of D4148 is 1V. Very critical, measurement shows that the 2.5V and 1.0V ramps the same speed.



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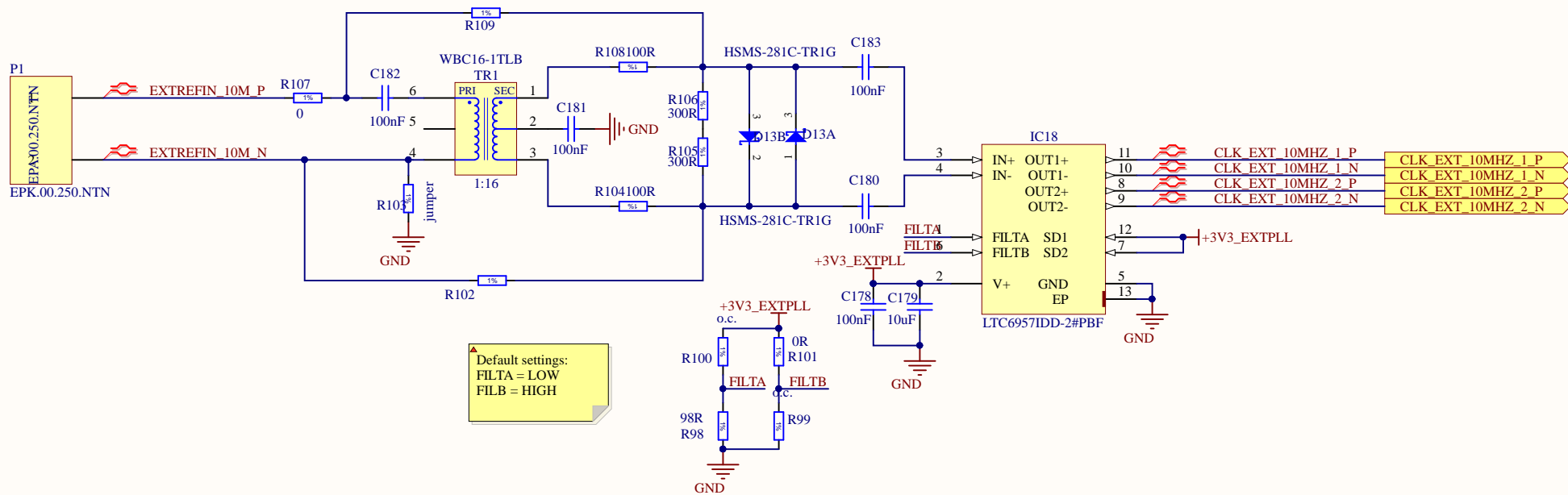
File name	DCDC_ALL.SchDoc		
Revision	1.1	Organization	Tsinghua University
Project	WRS-FL-HW	Date	2018-3-15



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File name	DFF_SYNC.SchDoc		
Revision	1.1	Organization	Tsinghua University
Project	WRS-FL-HW	Date	2018-3-15



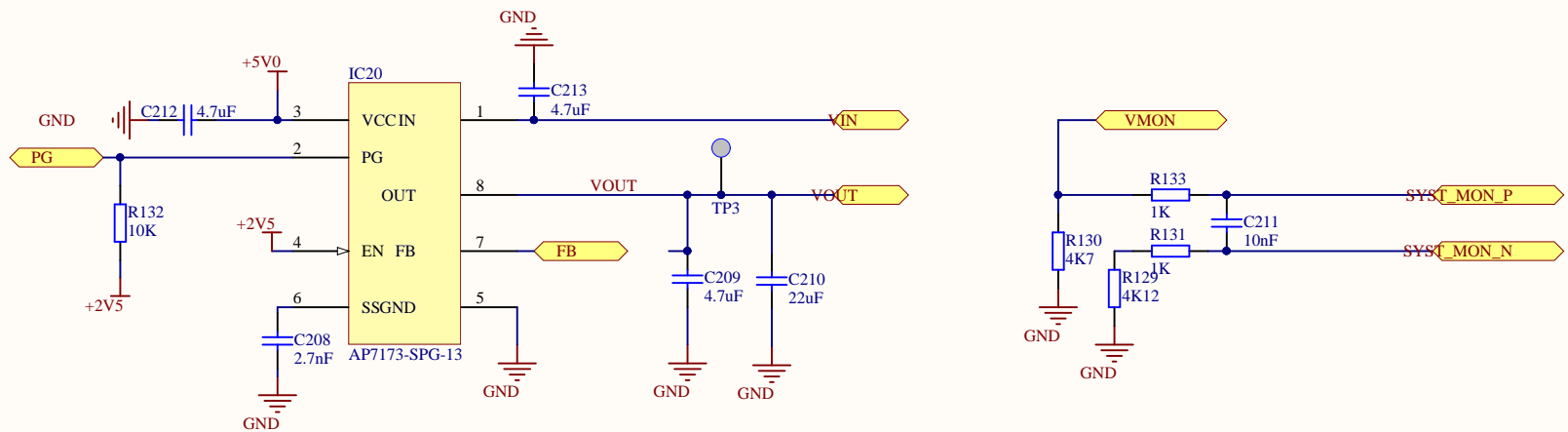
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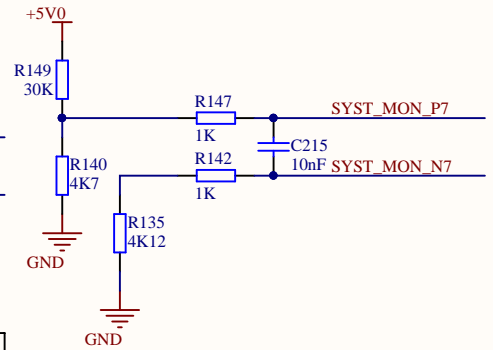
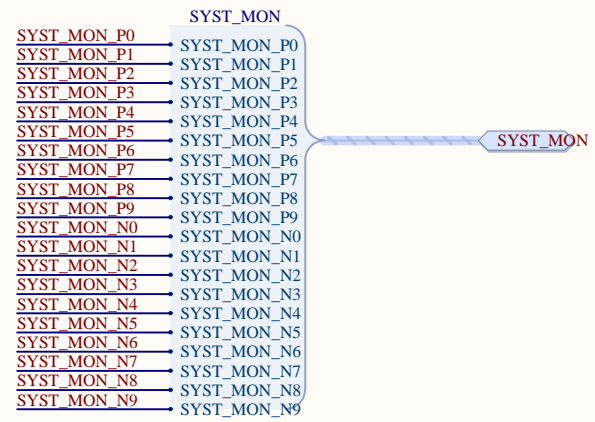
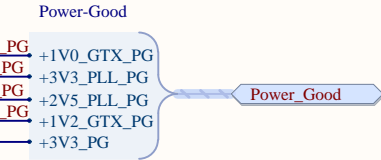
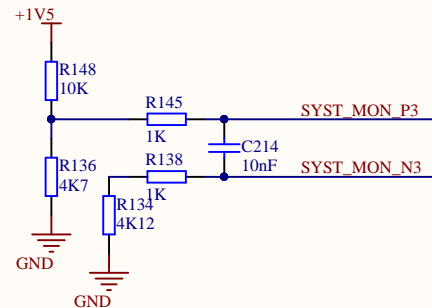
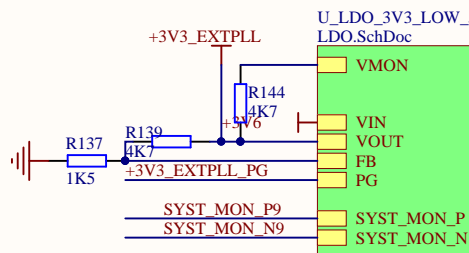
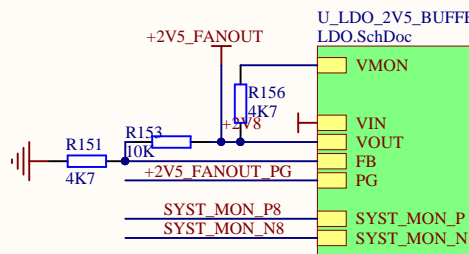
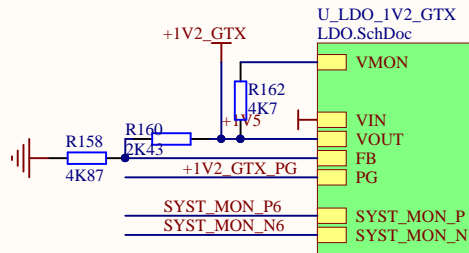
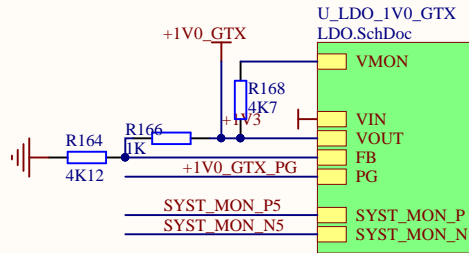
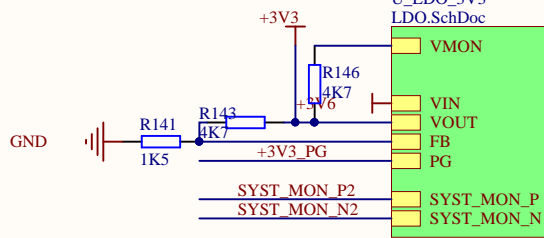
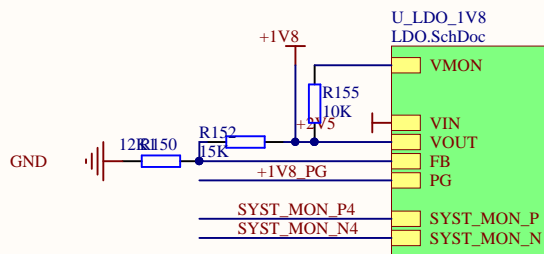
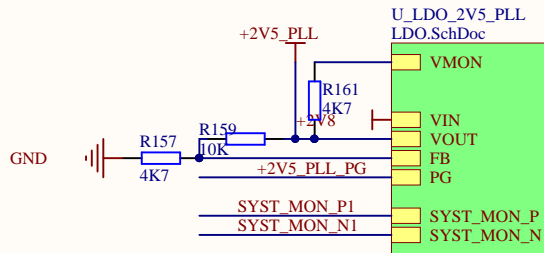
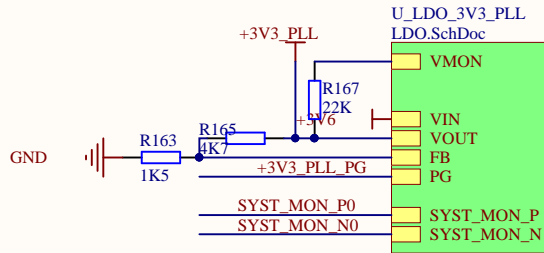
File name	EXT_10M_IN.SchDoc		
Revision	1.1	Organization	Tsinghua University
Project	WRS-FL-HW	Date	2018-3-15







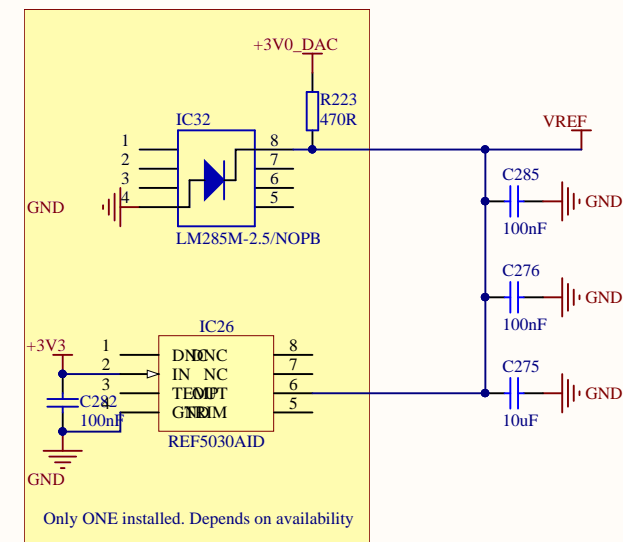
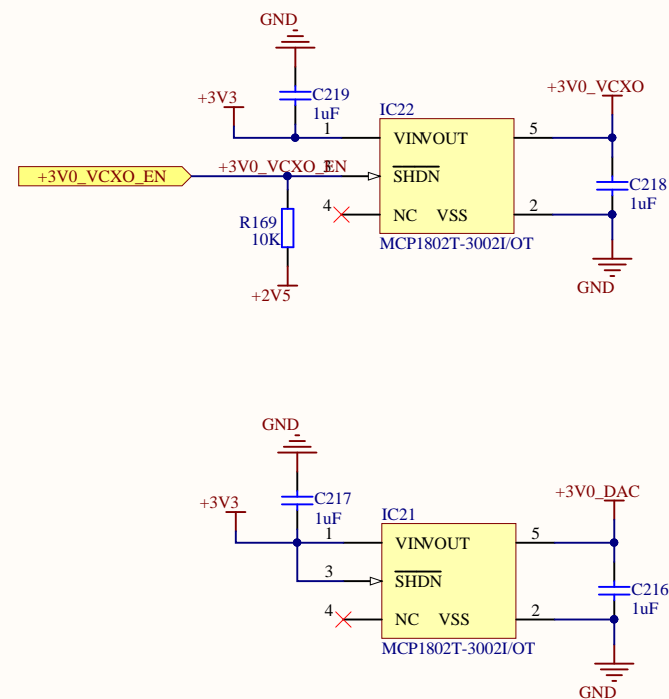
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Date:	2018-3-15	Sheet of
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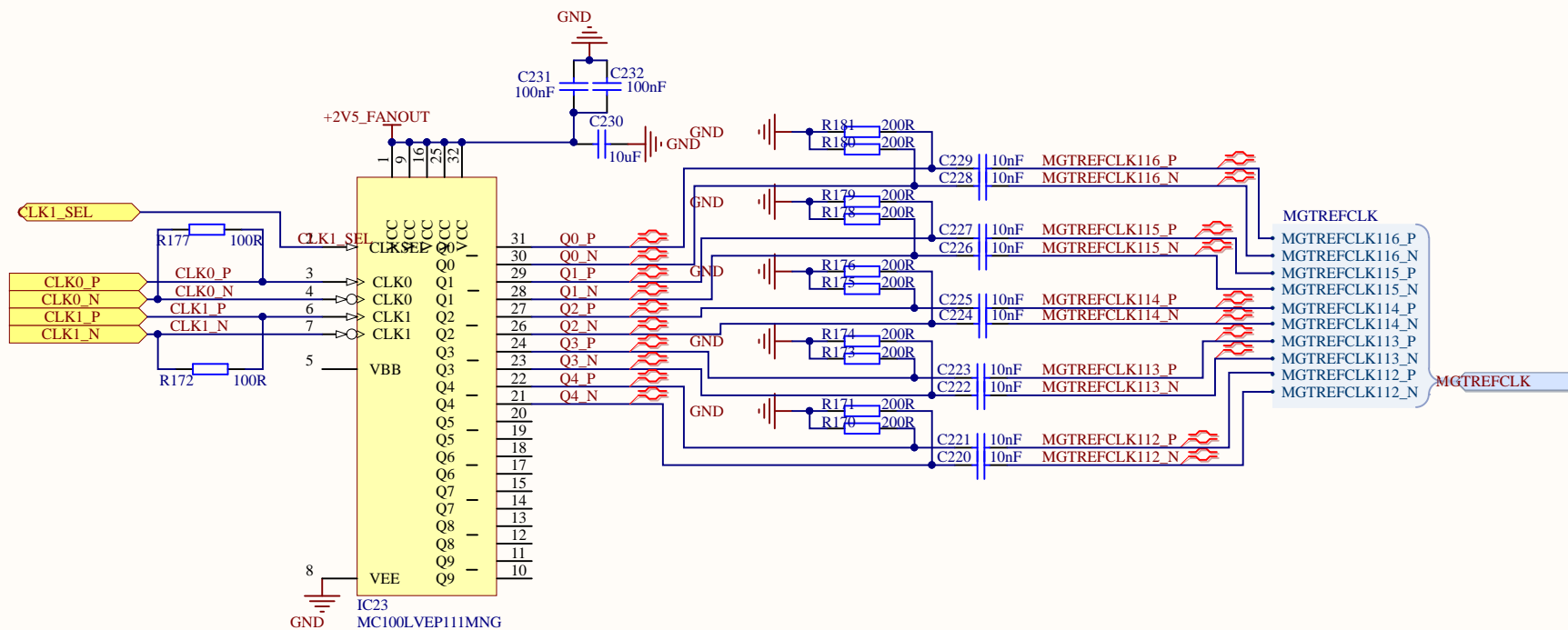
File name	LDO_ALL.SchDoc		
Revision	1.1	Organization	Tsinghua University
Project	WRS-FL-HW	Date	2018-3-15



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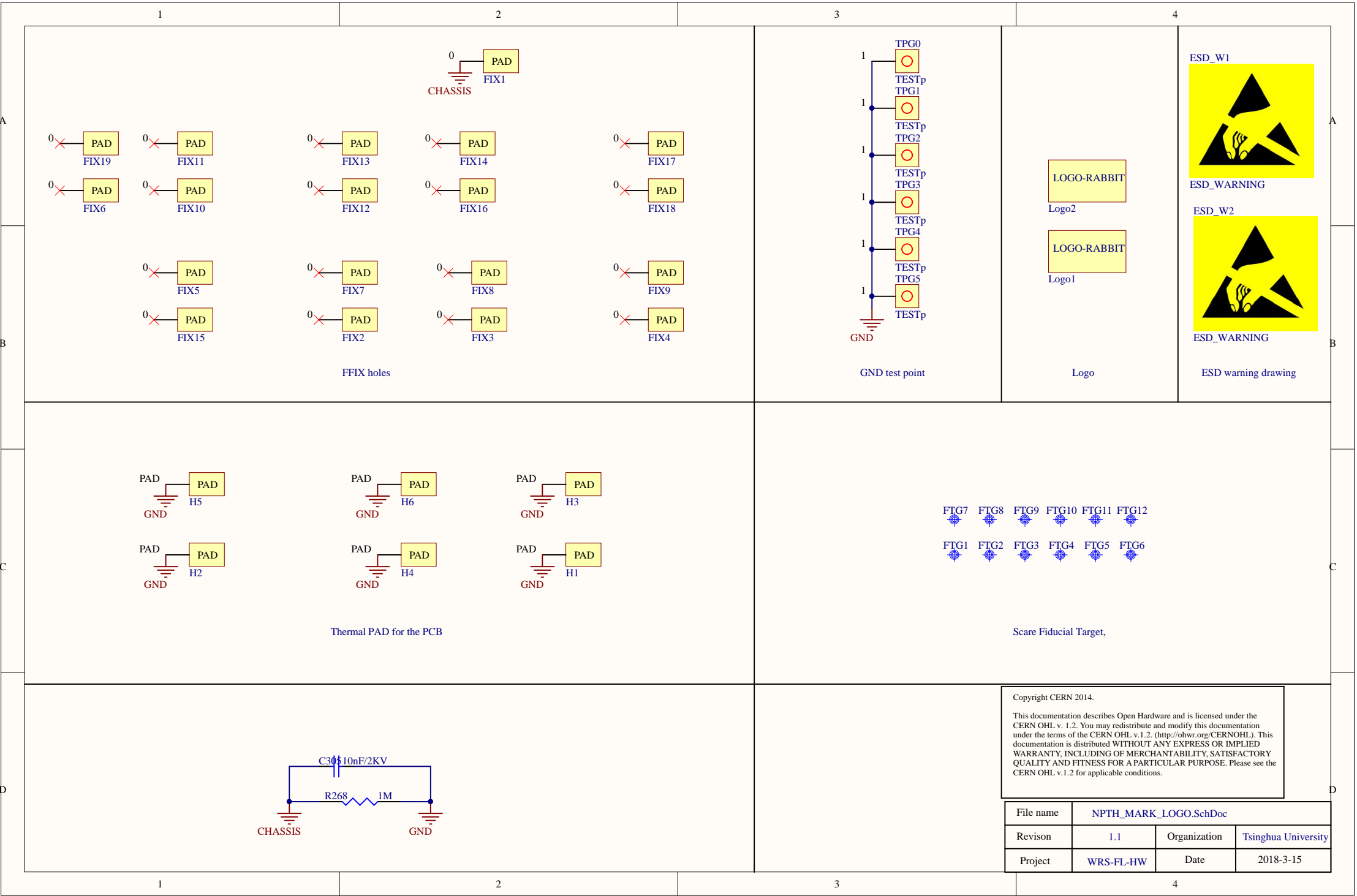
File name	LDO_XO.SchDoc		
Revision	1.1	Organization	Tsinghua University
Project	WRS-FL-HW	Date	2018-3-15

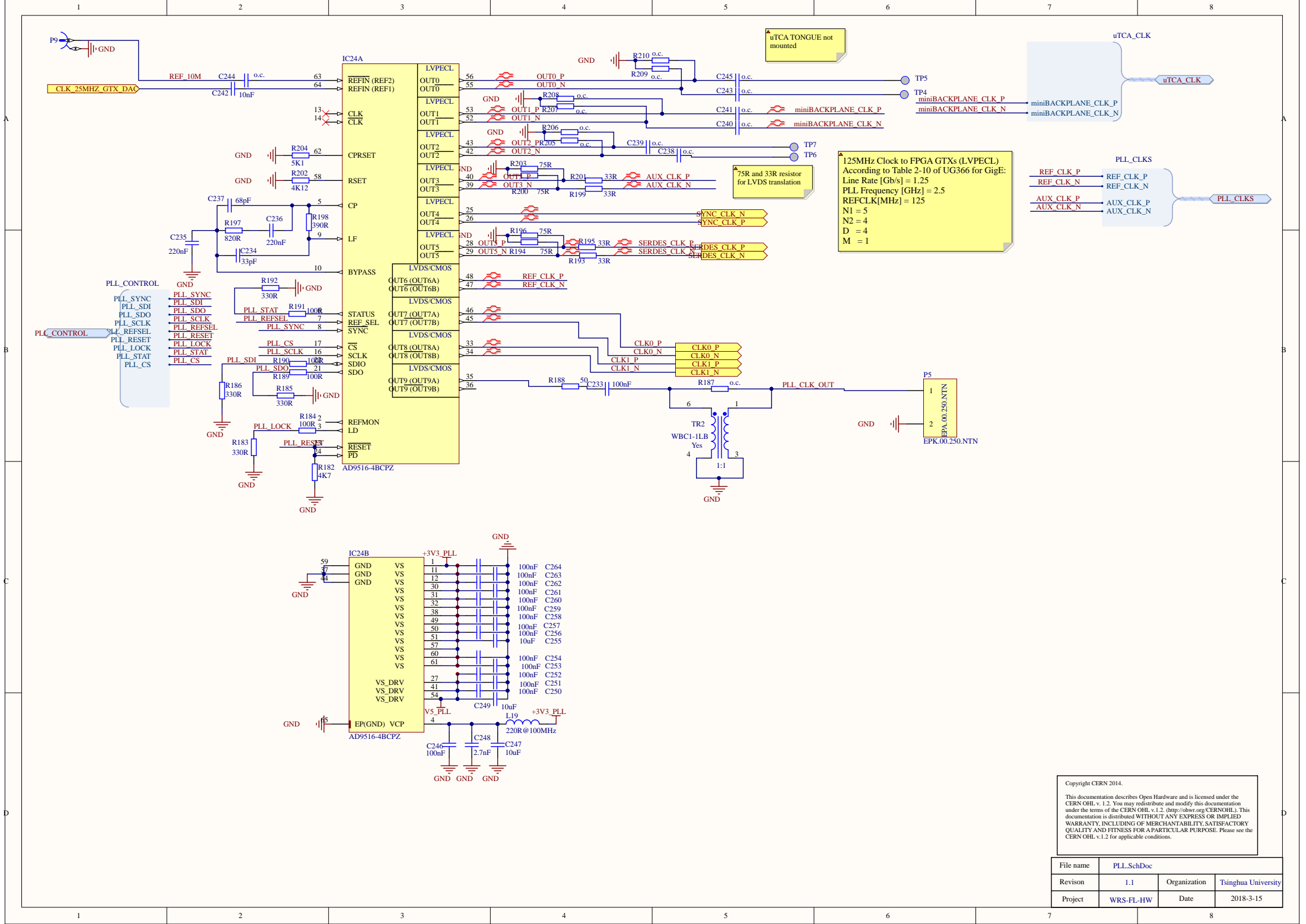


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File name	LVPECL_FANOUT.SchDoc		
Revision	1.1	Organization	Tsinghua University
Project	WRS-FL-HW	Date	2018-3-15



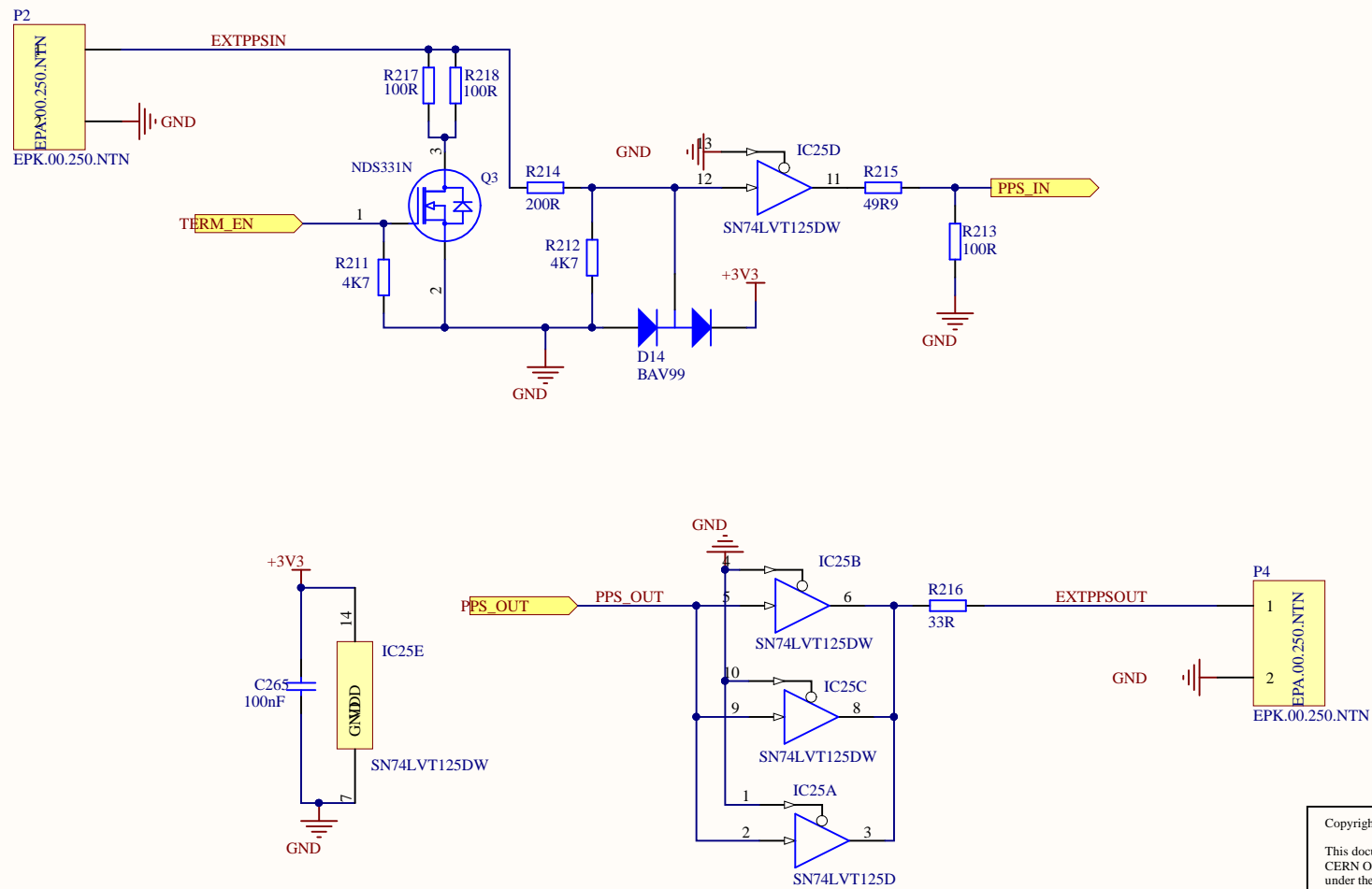


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File name	PLL_SchDoc		
Revision	1.1	Organization	Tsinghua University
Project	WRS-FL-HW	Date	2018-3-15

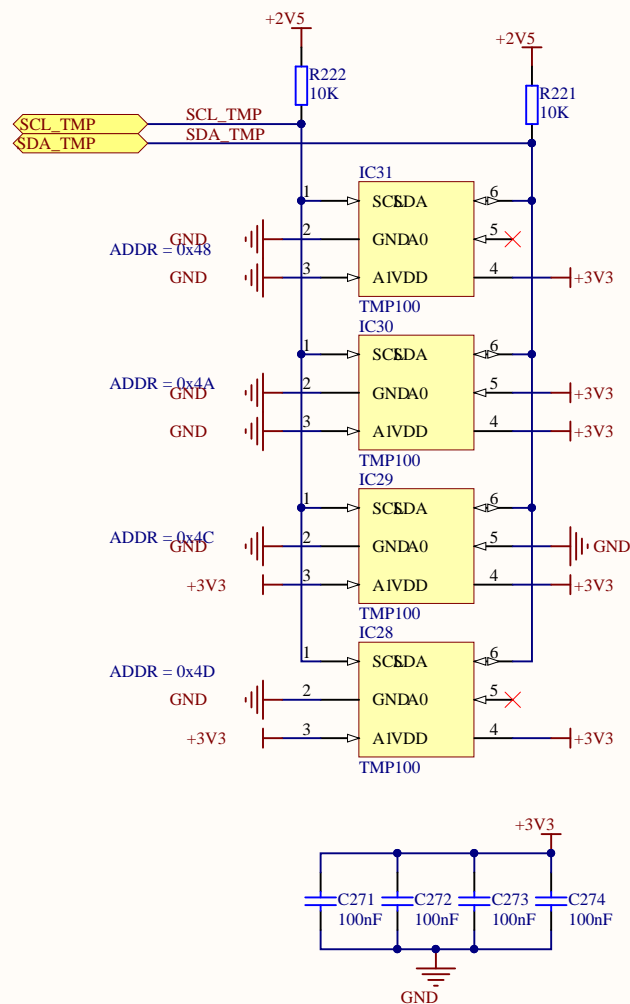




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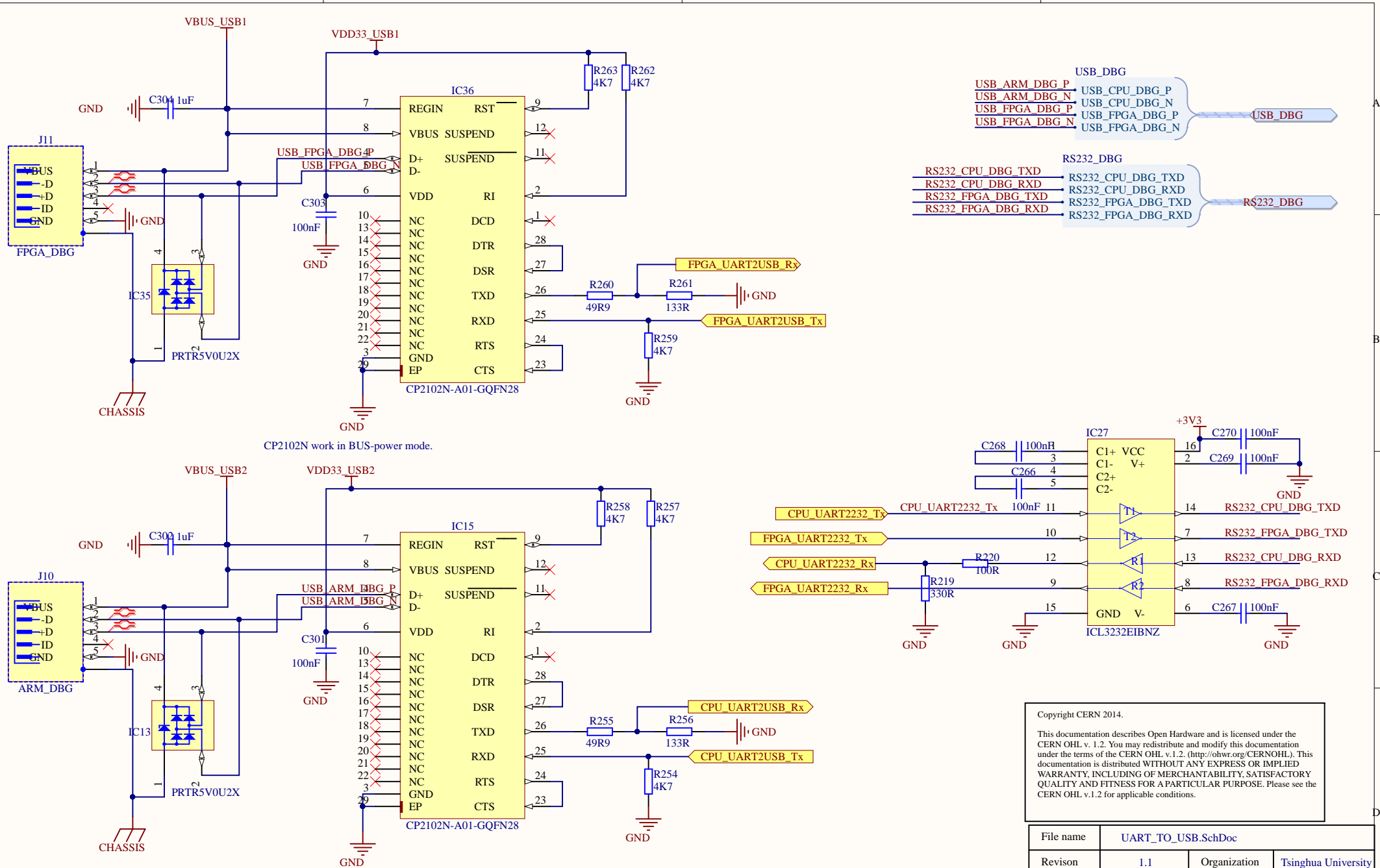
File name	PPS.SchDoc		
Revision	1.1	Organization	Tsinghua University
Project	WRS-FL-HW	Date	2018-3-15

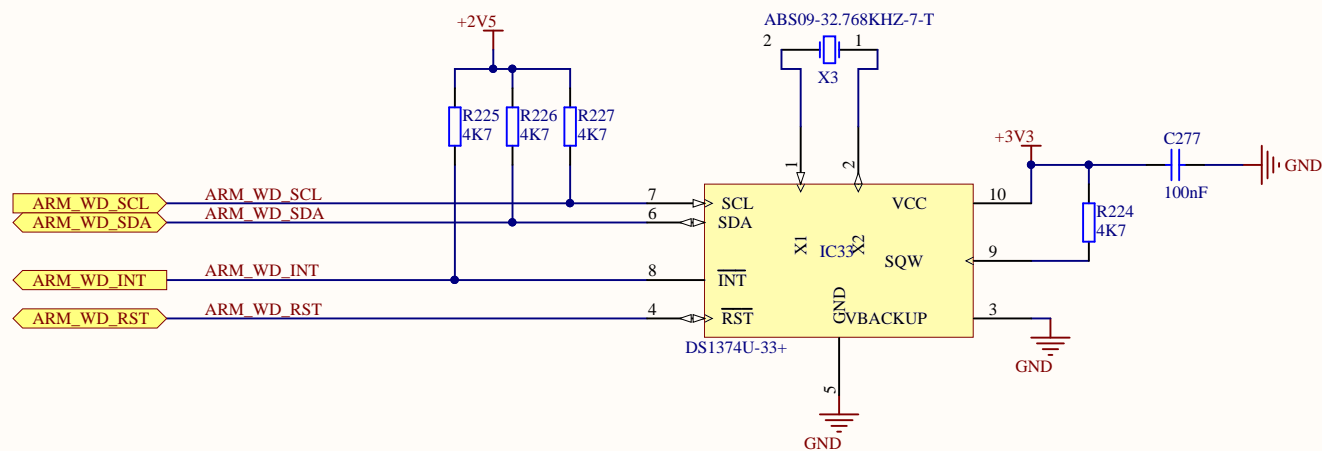


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File name	SENSOR.SchDoc		
Revision	1.1	Organization	Tsinghua University
Project	WRS-FL-HW	Date	2018-3-15

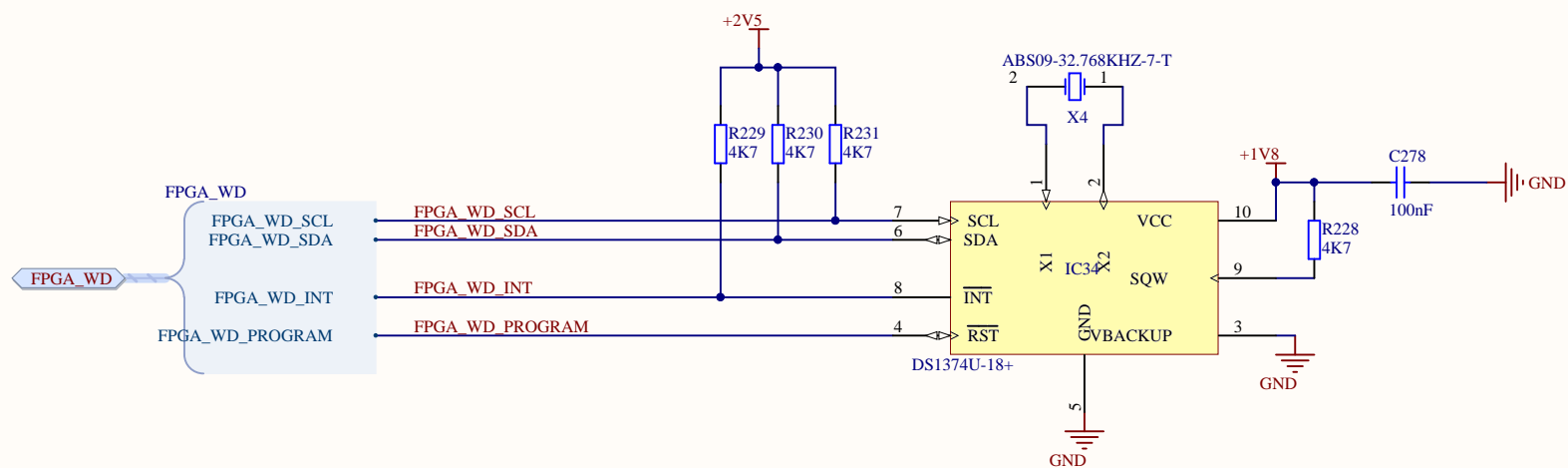




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File name	WDT_ARM.SchDoc		
Revision	1.1	Organization	Tsinghua University
Project	White Rabbit	Date	2018-3-15



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File name	WDT_FPGA.SchDoc		
Revision	1.1	Organization	Tsinghua University
Project	WRS-FL-HW	Date	2018-3-15