

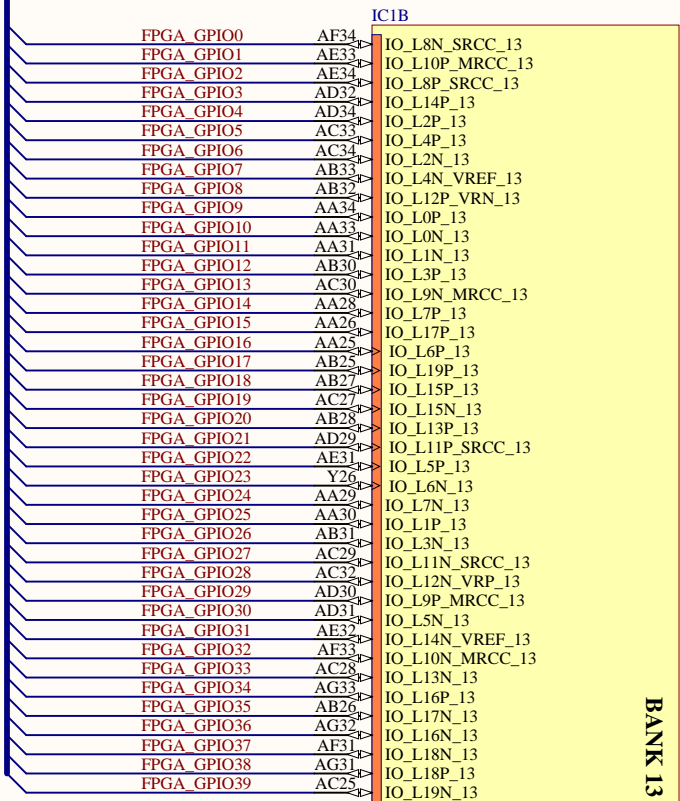
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File name	FPGA_Configuration.SchDoc		
Revision	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2018-11-6

FPGA_GPIO[0..39]

FPGA_GPIO[0..39]



IC1B

BANK 13

XC6VLX240T-2FF1156I

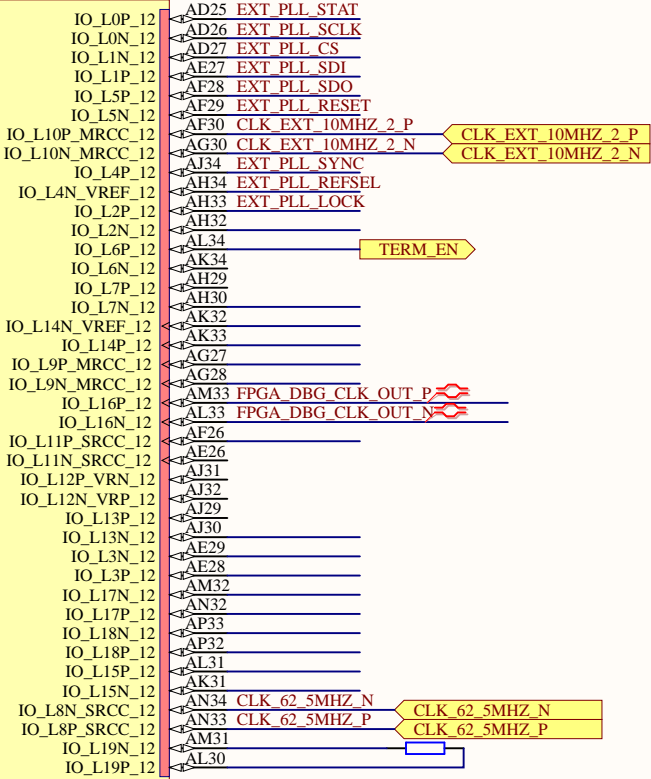
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File name	FPGA_GPIOs.SchDoc		
Revision	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2018-11-6

IC1A

BANK 12



XC6VLX240T-2FF1156I

R36 100R

EXT_PLL_CTRL

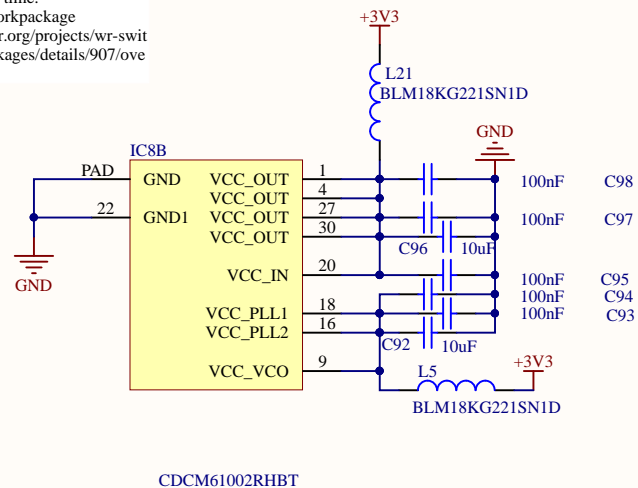
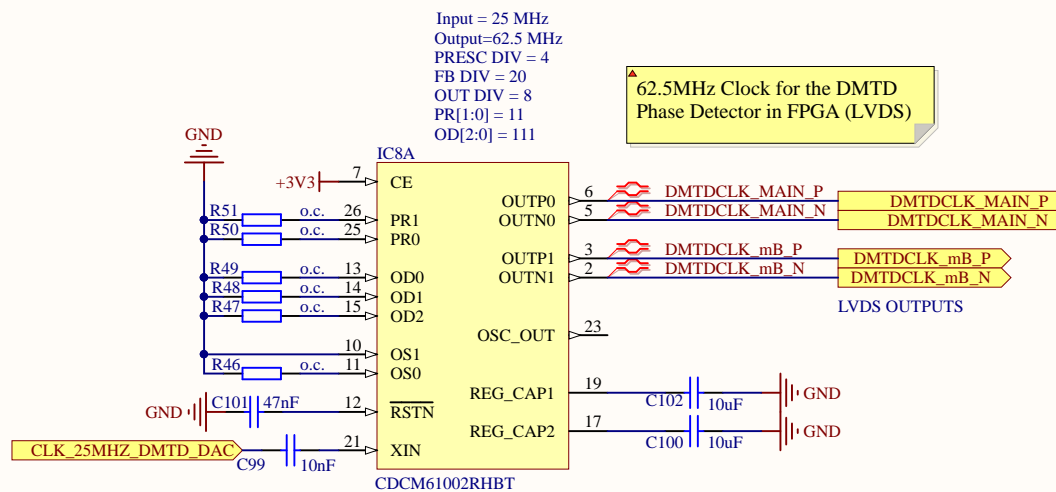
EXT_PLL_CTRL

EXT_PLL_SYNC	EXT_PLL_SYNC
EXT_PLL_SDI	EXT_PLL_SDI
EXT_PLL_SDO	EXT_PLL_SDO
EXT_PLL_SCLK	EXT_PLL_SCLK
EXT_PLL_REFSSEL	EXT_PLL_REFSSEL
EXT_PLL_RESET	EXT_PLL_RESET
EXT_PLL_LOCK	EXT_PLL_LOCK
EXT_PLL_STAT	EXT_PLL_STAT
EXT_PLL_CS	EXT_PLL_CS

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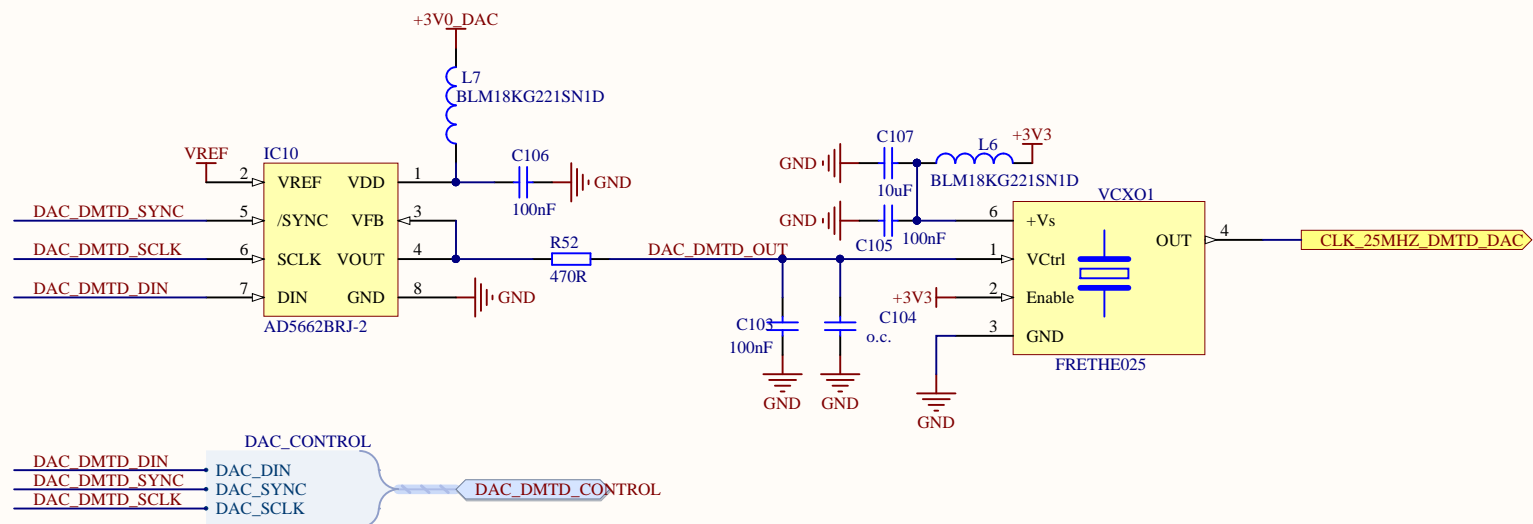
File name	FPGA_EXT_PLL.SchDoc		
Revision	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2018-11-6



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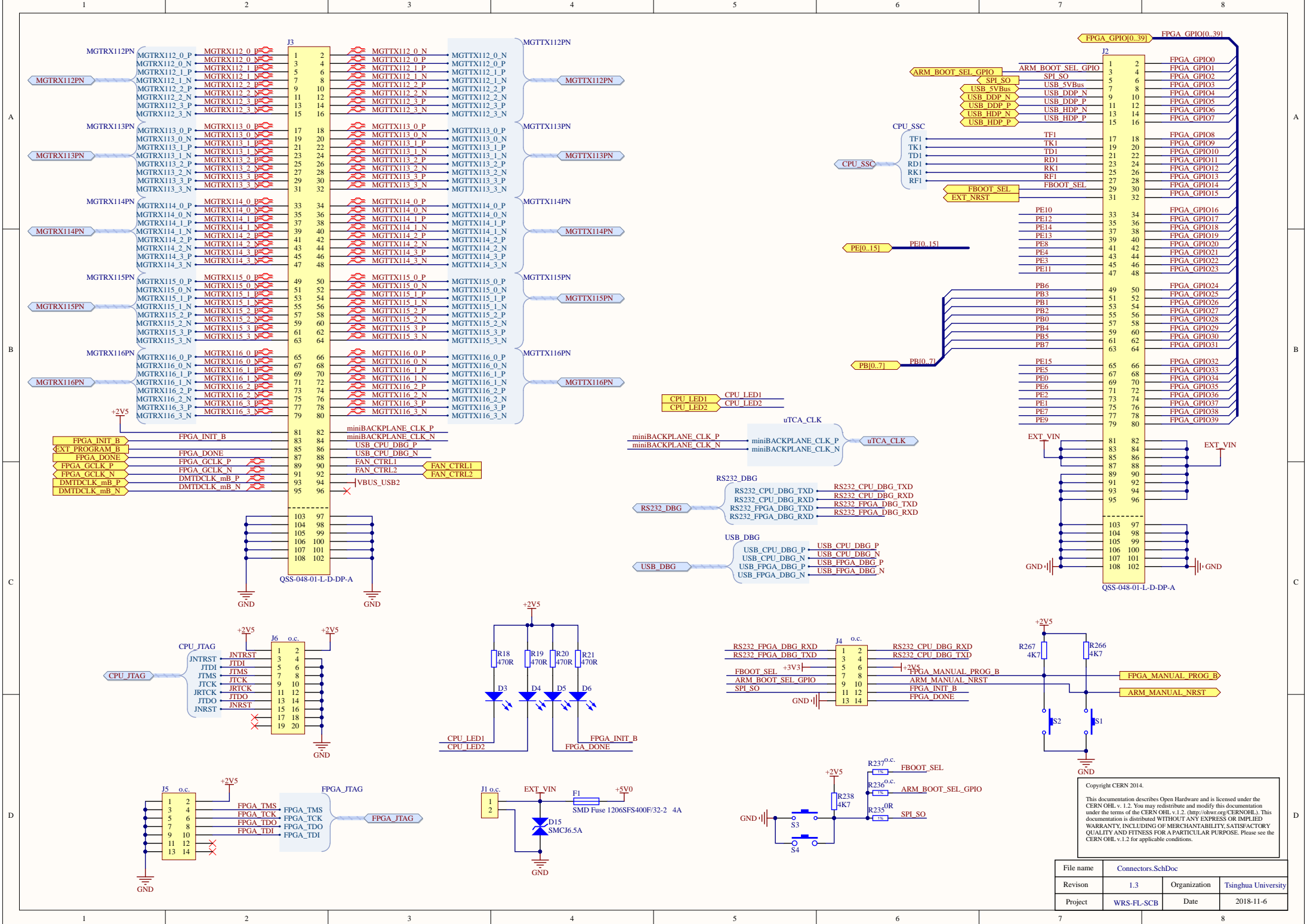
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Revision	1.3	Organization	Tsinghua University
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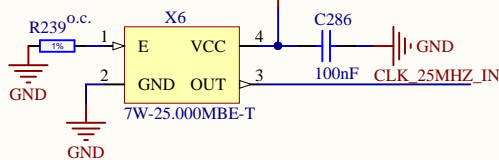
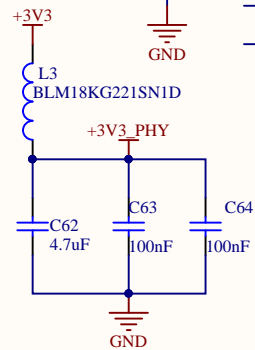
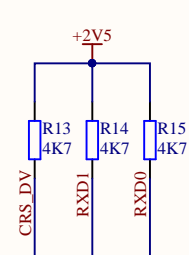
File name	CLK_25M_DMTD.SchDoc		
Revision	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2018-11-6



IC2L

PA10/ETX0
PA11/ETX1
PA12/ERX0
PA13/ERX1
PA14/ETXEN
PA15/ERXDV
PA16/ERXER
PA17/ETXCK
PA18/EMDC
PA19/EMDIO
PA27/MCI1_DA4/ETXER
PA28/MCI1_DA5/ERXCK
PA29/MCI1_DA6/ECRS
PA30/MCI1_DA7/ECOL
(Power Supply VDDIOPO)

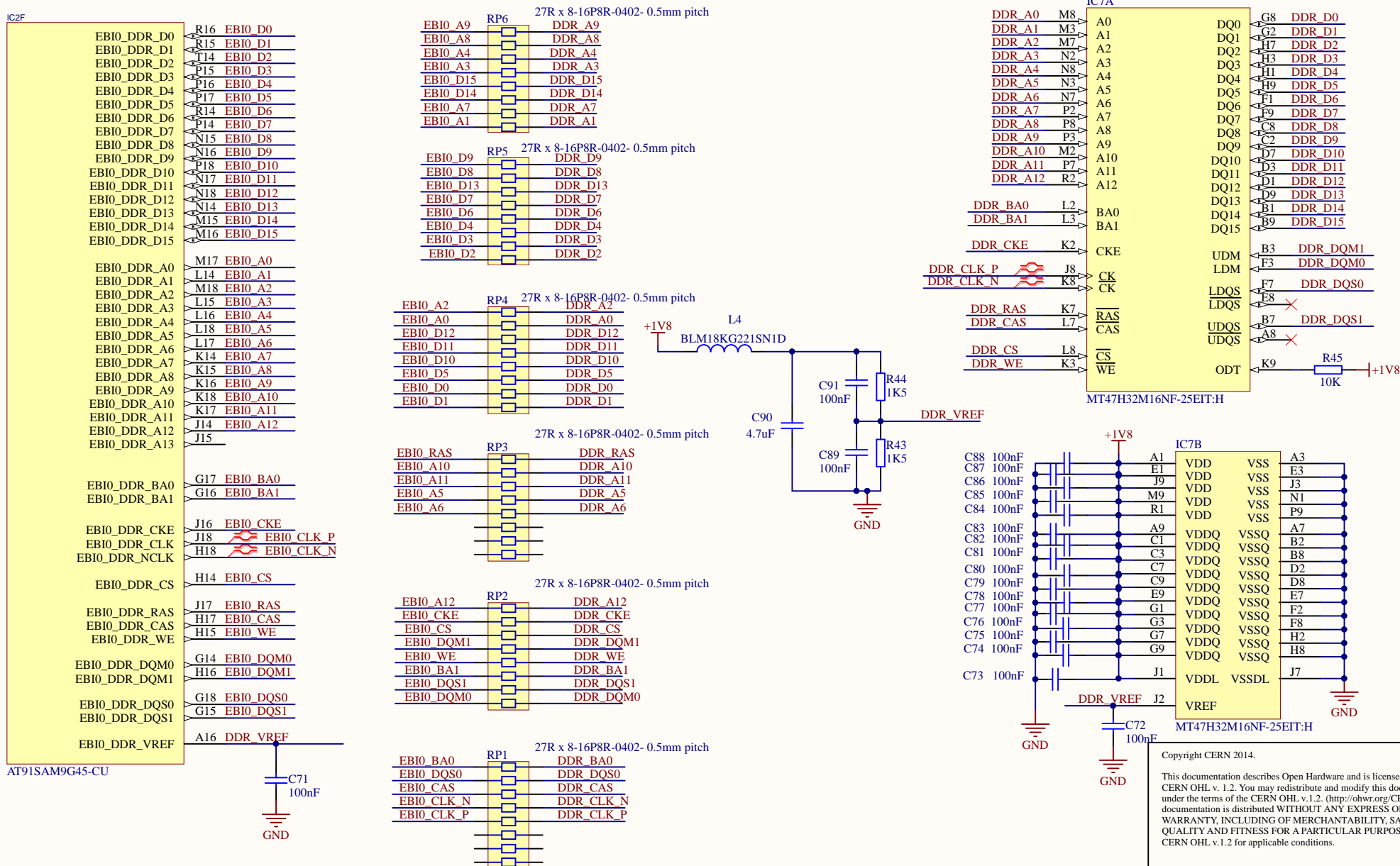
AT91SAM9G45-CU



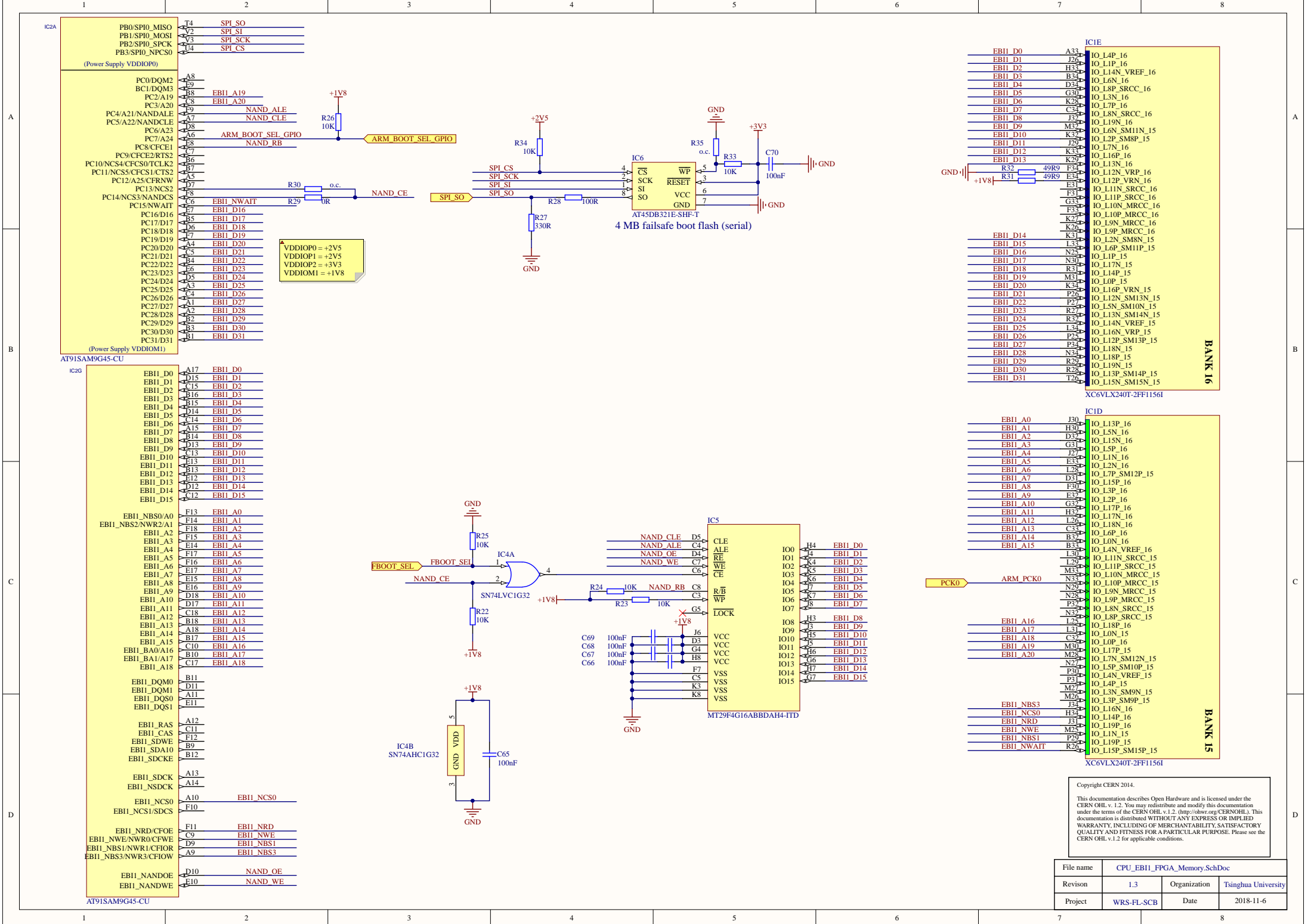
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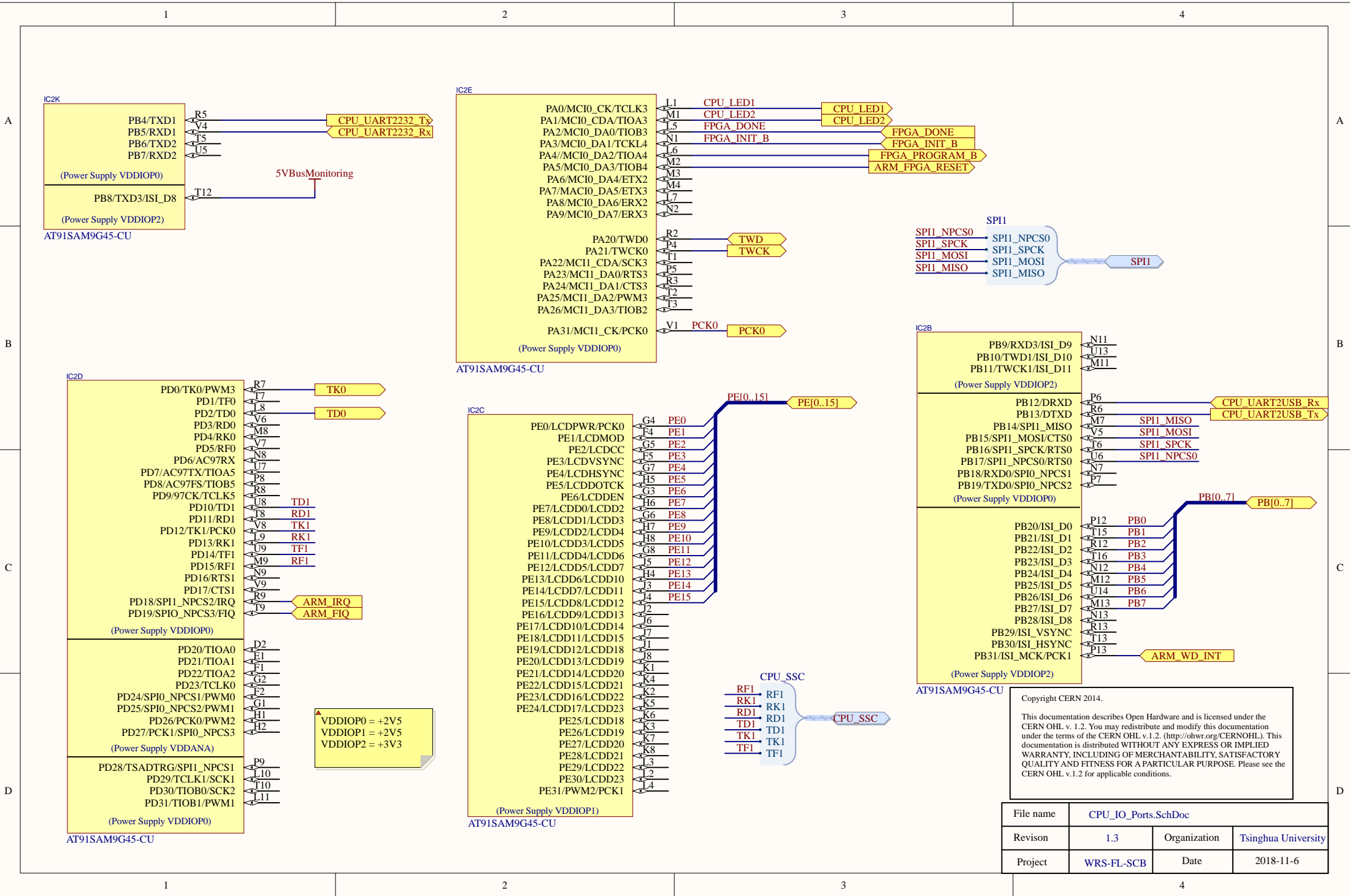
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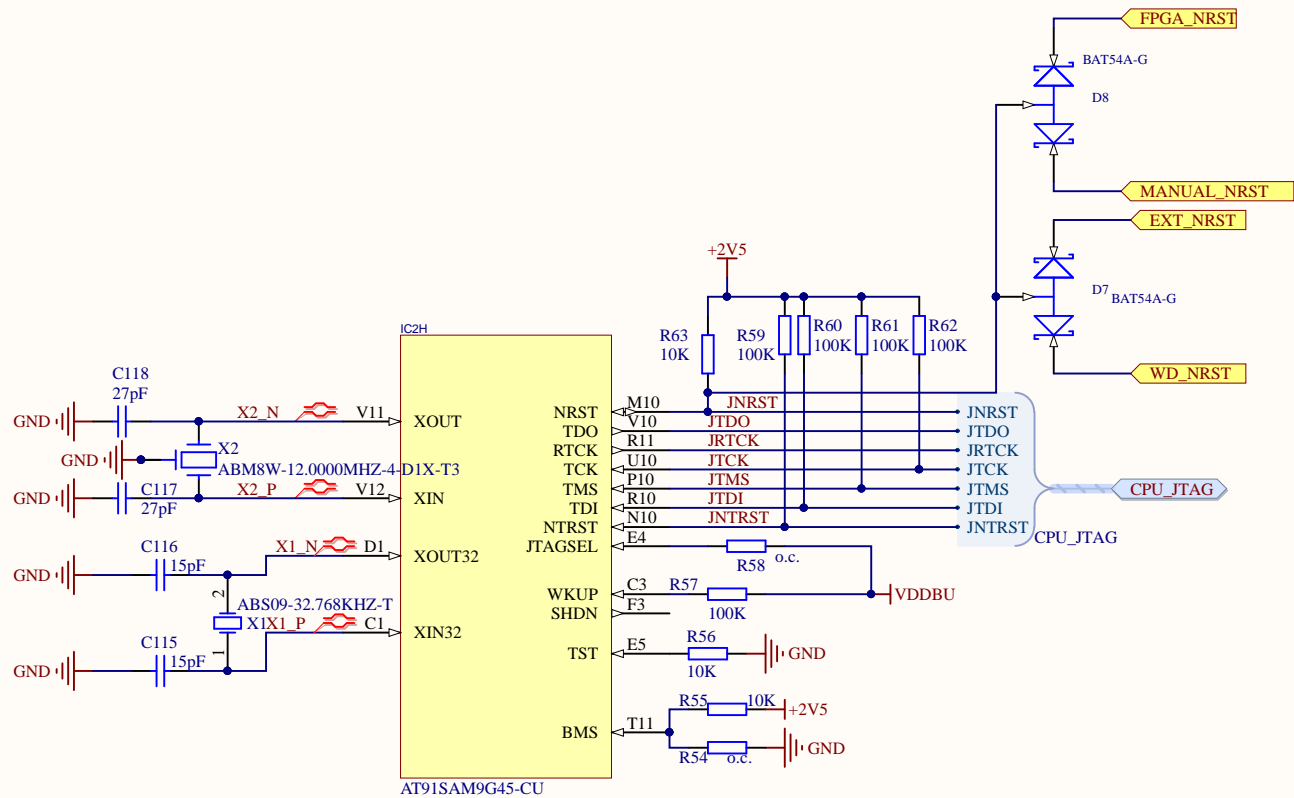
File name	CPU_100M_Ethernet.SchDoc		
Revision	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2018-11-6



File name	CPU_DDR2.SchDoc		
Revision	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2018-11-6



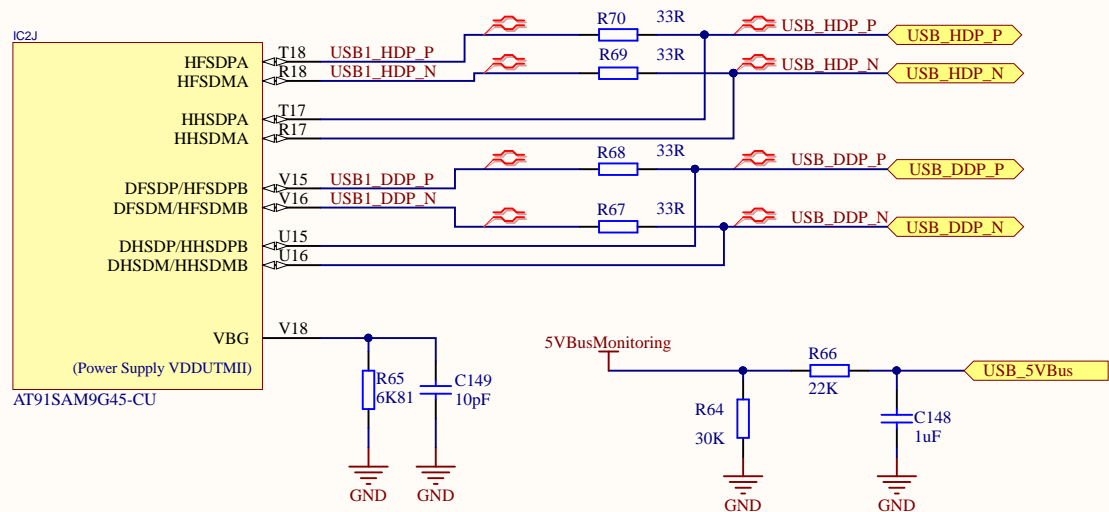




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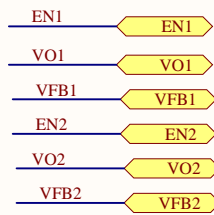
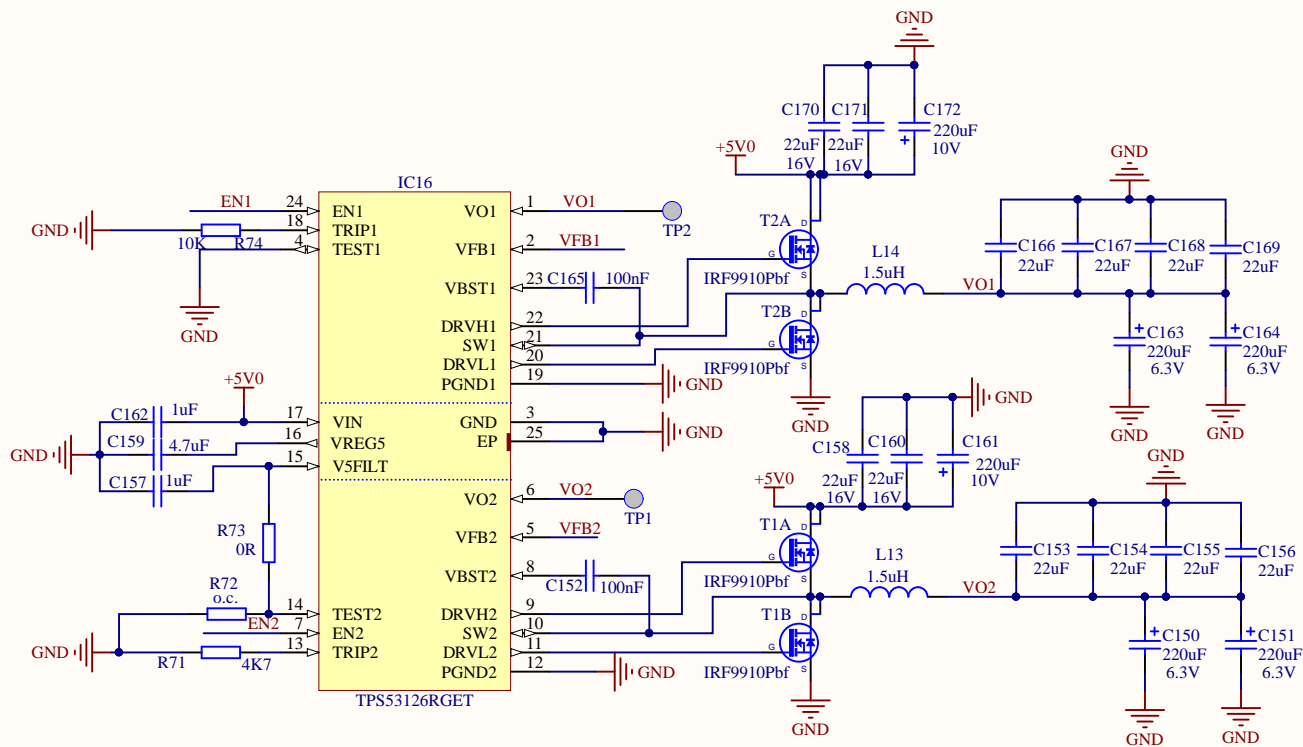
File name	CPU_JTAG.SchDoc		
Revision	1.3	Organization	Tsinghua University
Project	White Rabbit	Date	2018-11-6



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File name	CPU_USB.SchDoc		
Revision	1.3	Organization	Tsinghua University
Project	White Rabbit	Date	2018-11-6



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File name	DCDC.SchDoc		
Revision	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2018-11-6

A

B

C

D

A

B

C

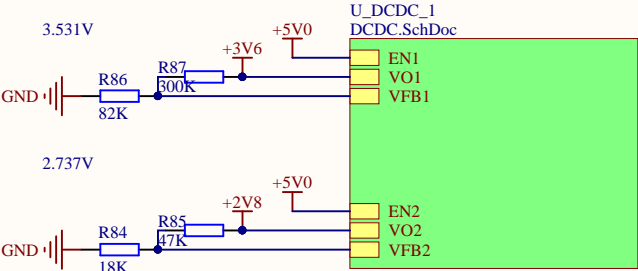
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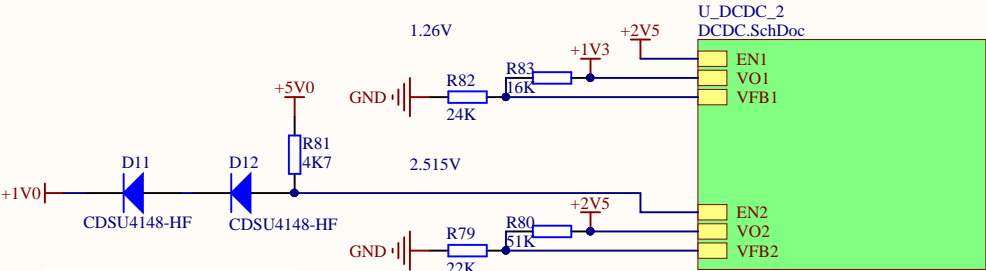
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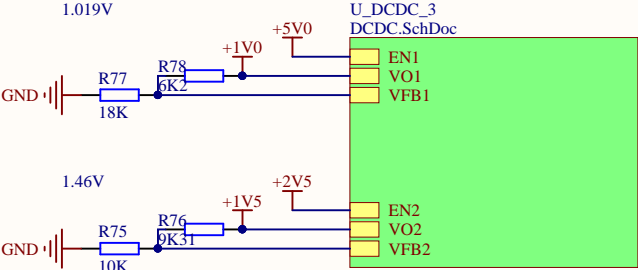
4



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The voltage threshold of EN is 2.0V, the Vf-max of D4148 is 1V. Very critical, measurement shows that the 2.5V and 1.0V ramps the same speed.



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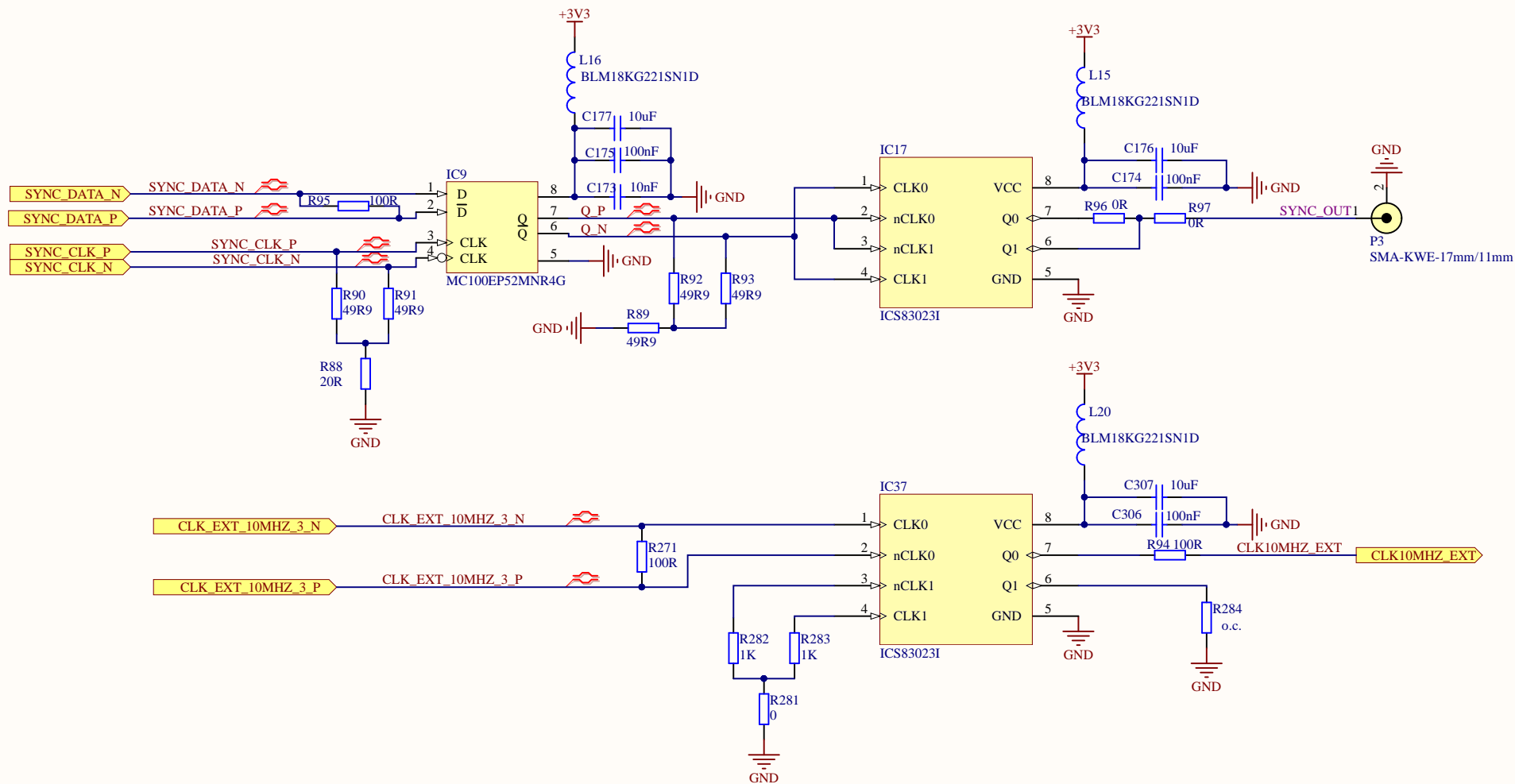
File name	DCDC_ALL.SchDoc		
Revision	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2018-11-6

1

2

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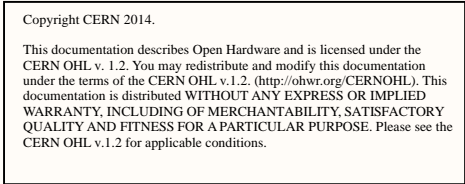
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File name	DFF_SYNC.SchDoc		
Revision	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2018-11-6



File name	EXT_10M_IN.SchDoc		
Revision	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2018-11-6

A

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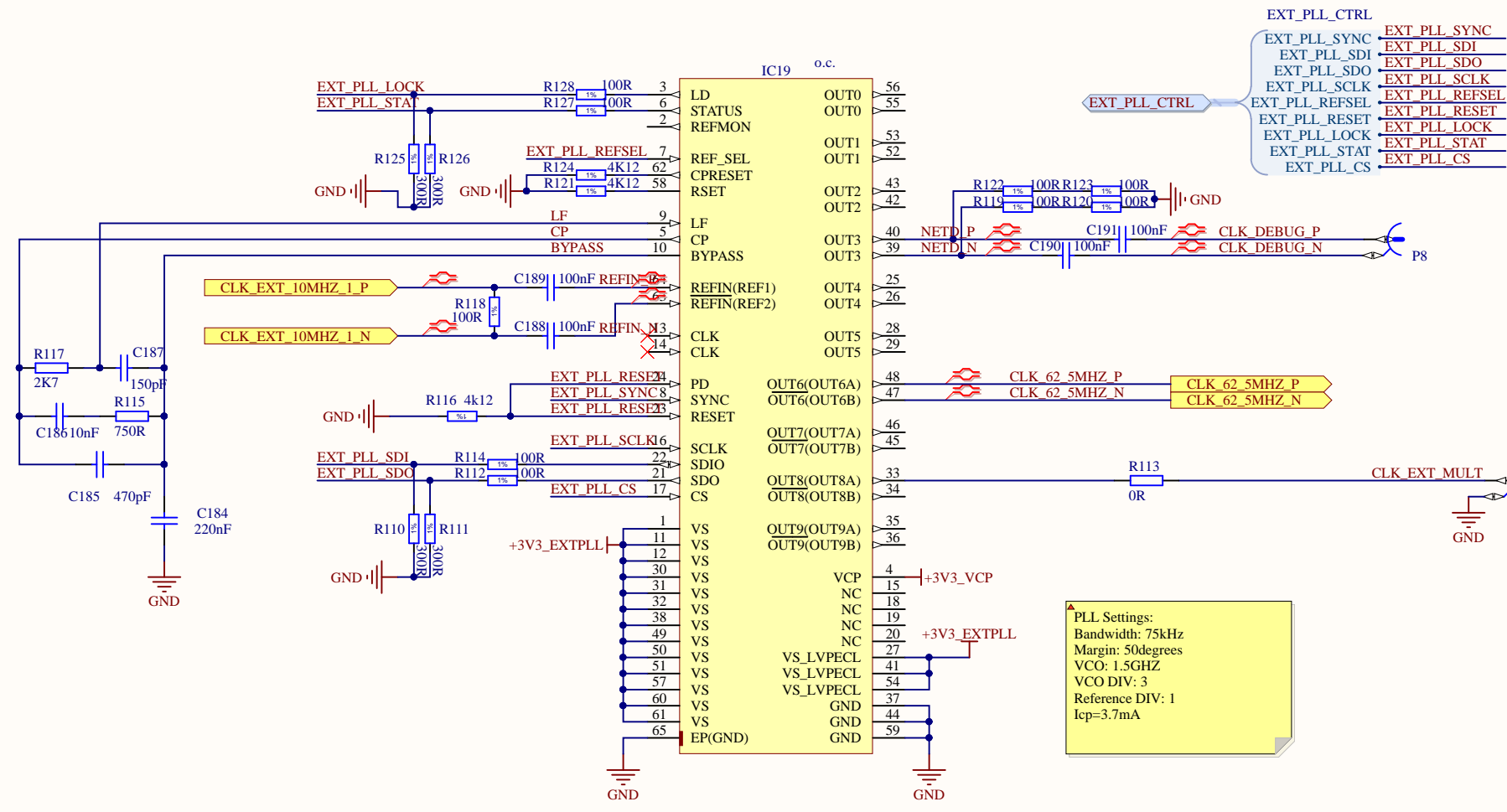
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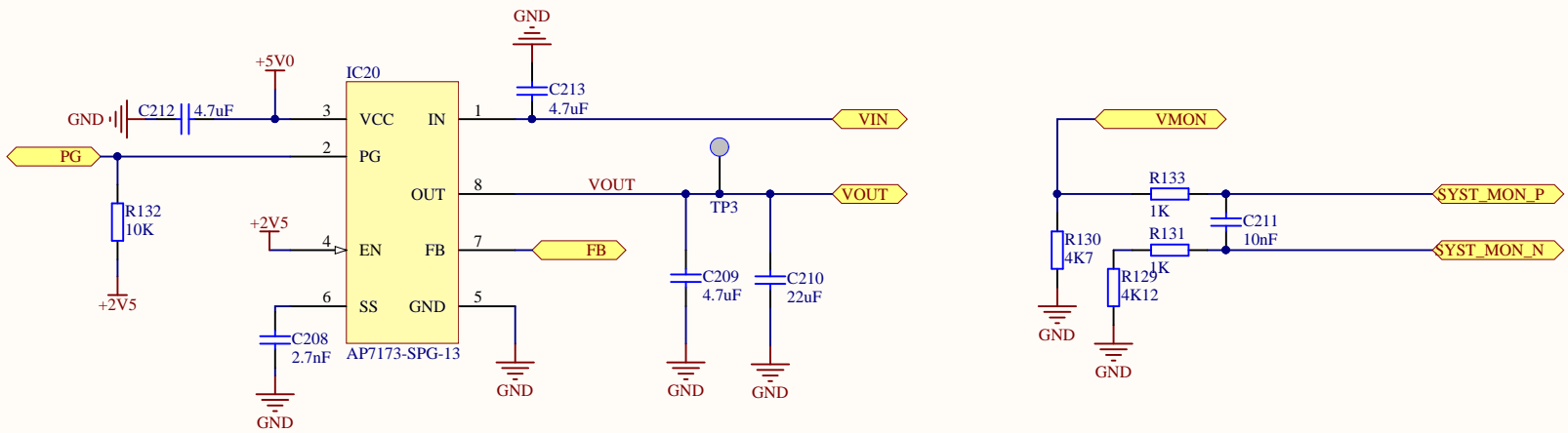
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File name	EXT_PLL.SchDoc		
Revision	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2018-11-6



A

A

B

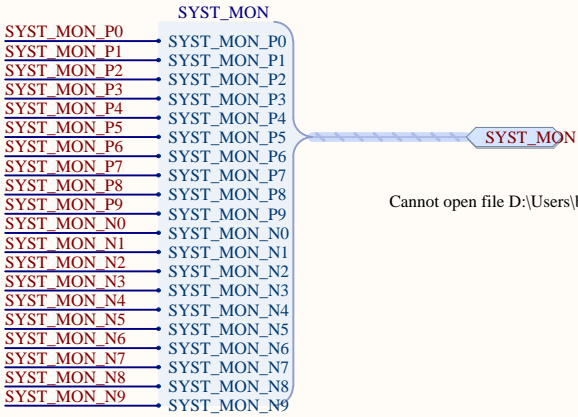
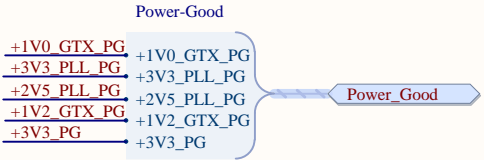
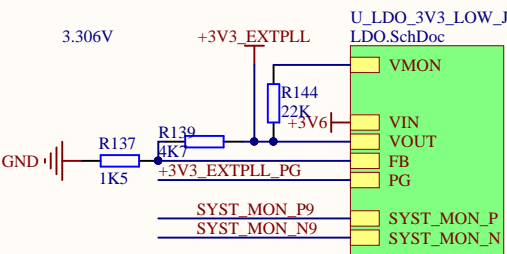
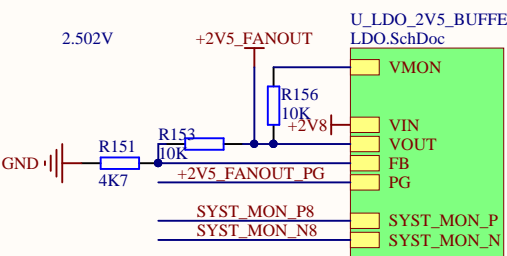
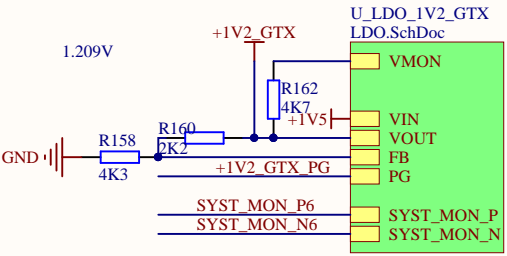
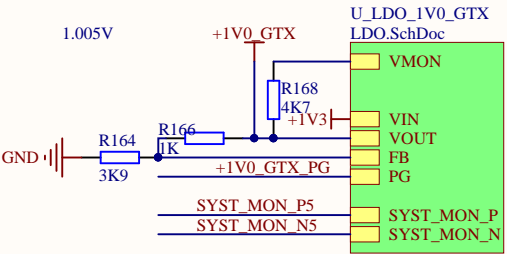
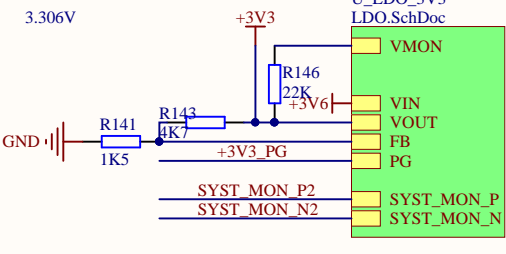
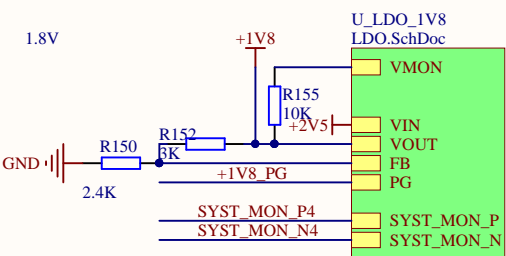
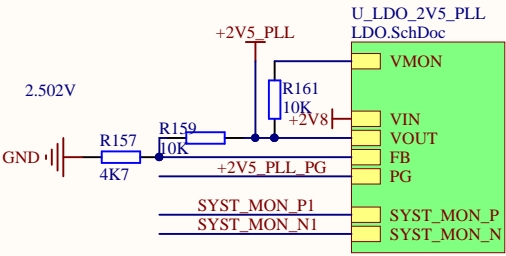
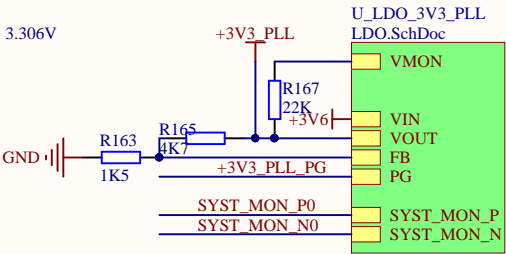
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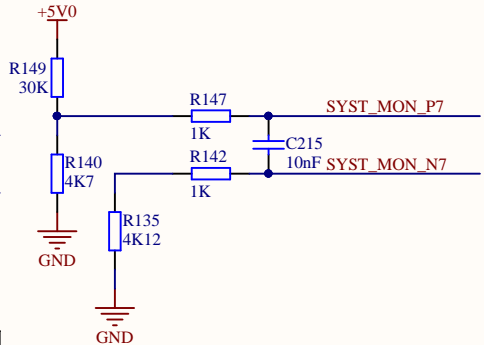
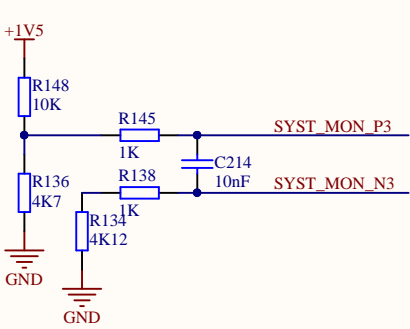
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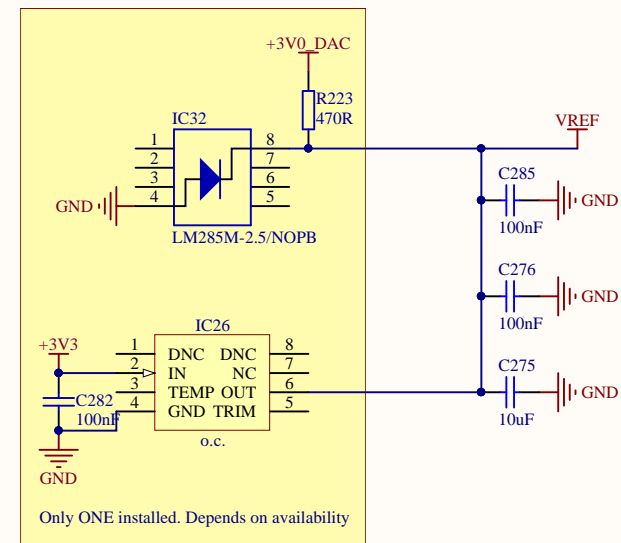
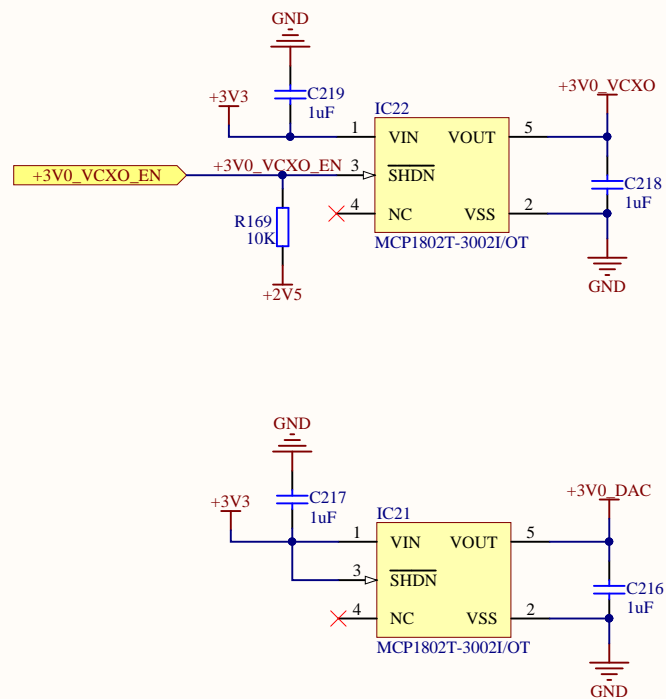
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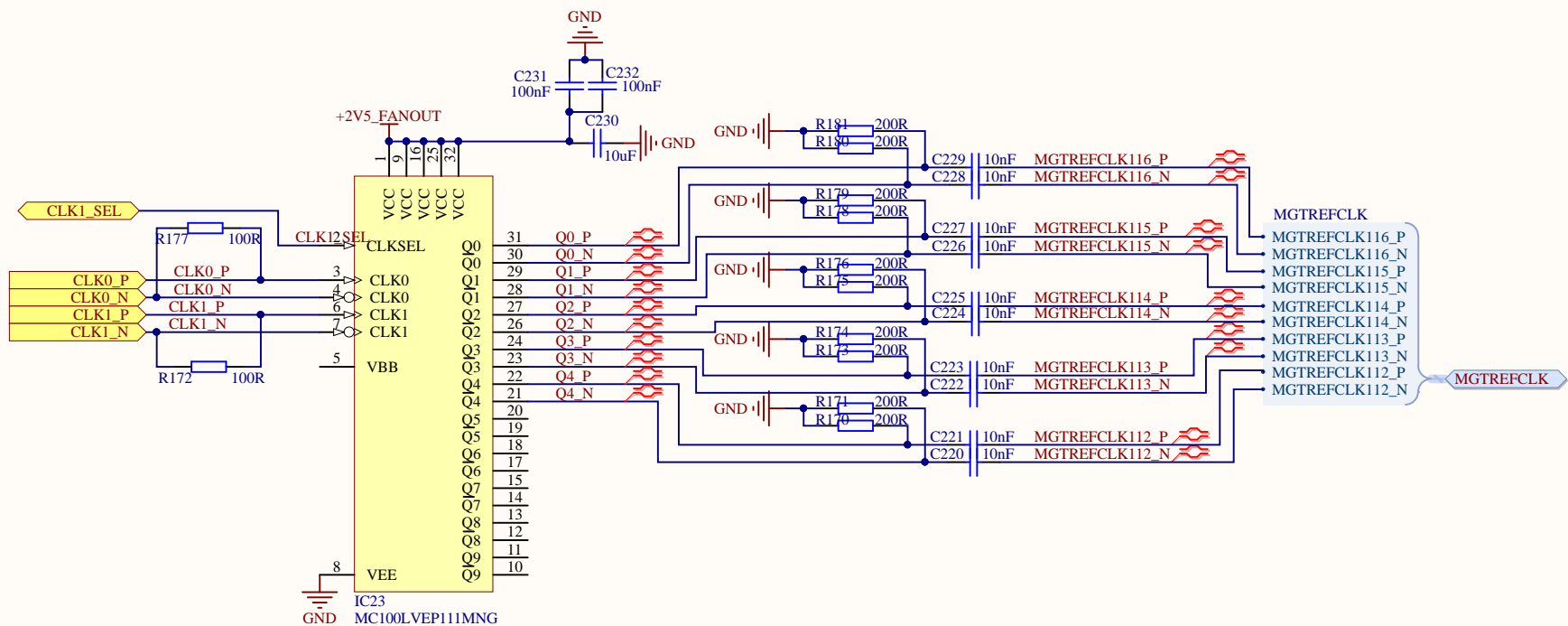
File name	LDO_ALL.SchDoc		
Revision	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2018-11-6



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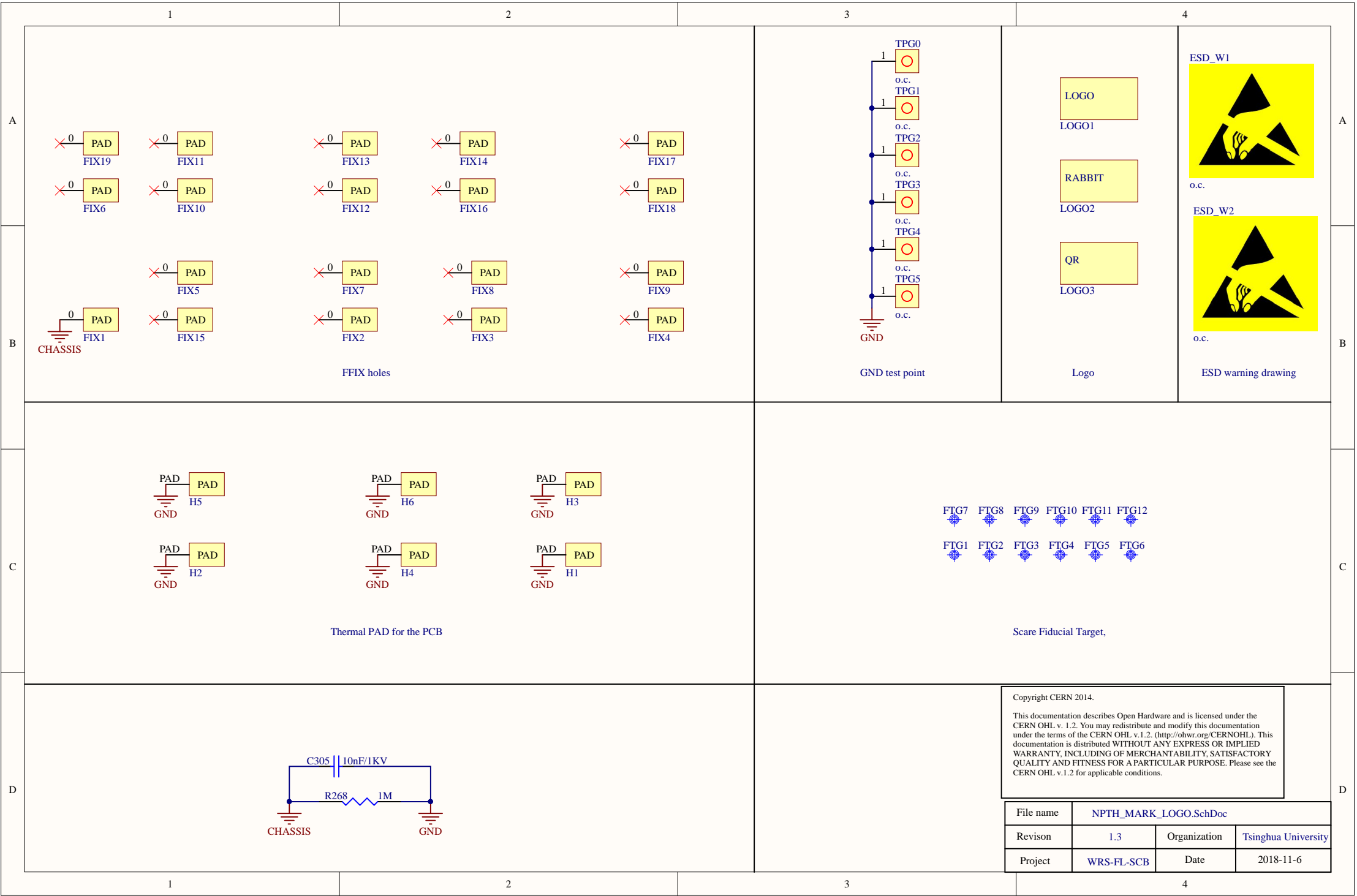
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Revision	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2018-11-6



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File name	LVPECL_FANOUT.SchDoc		
Revision	1.3	Organization	Tsinghua University
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PAD

FIX1

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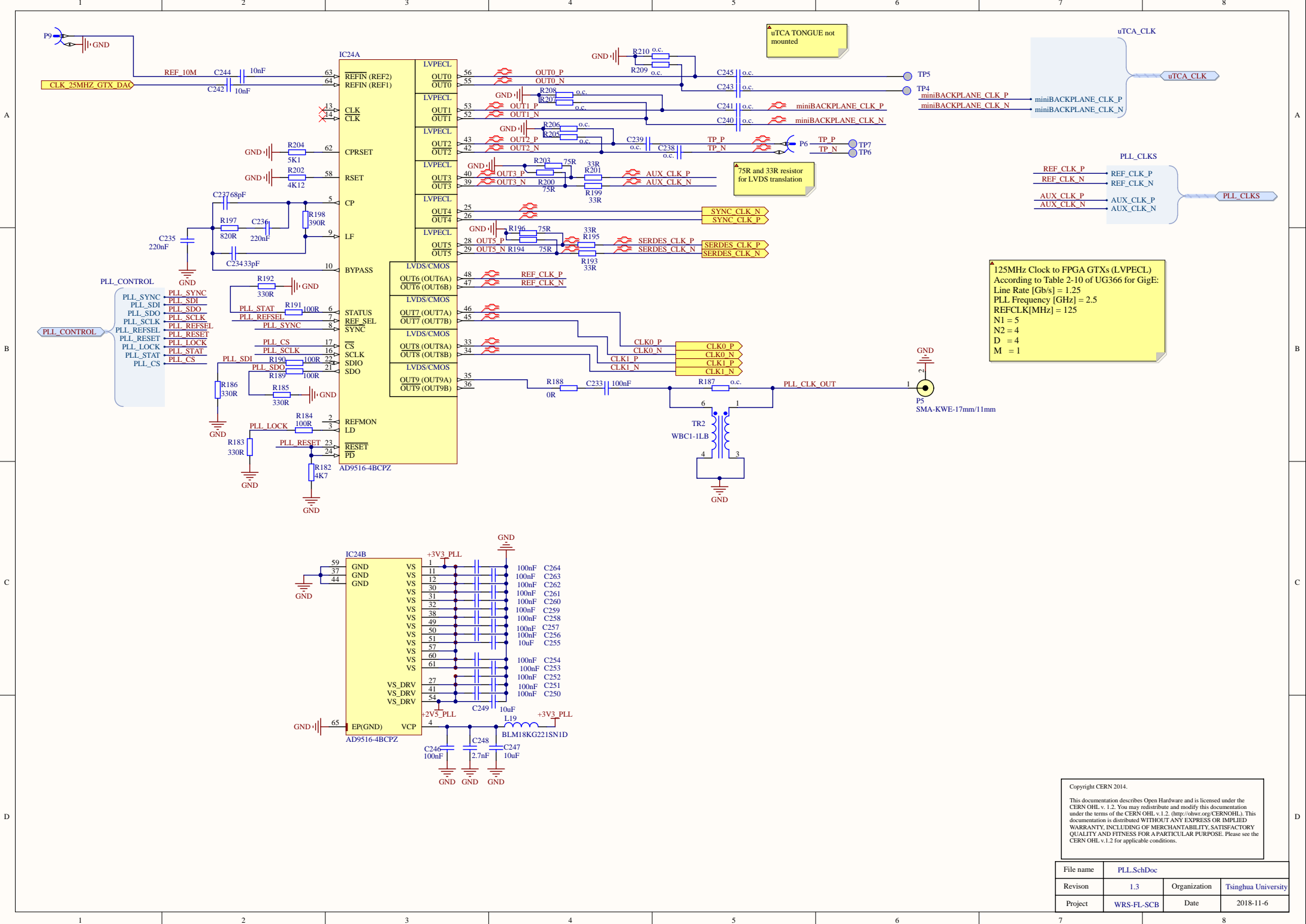
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PAD

FIX15

CHASSIS

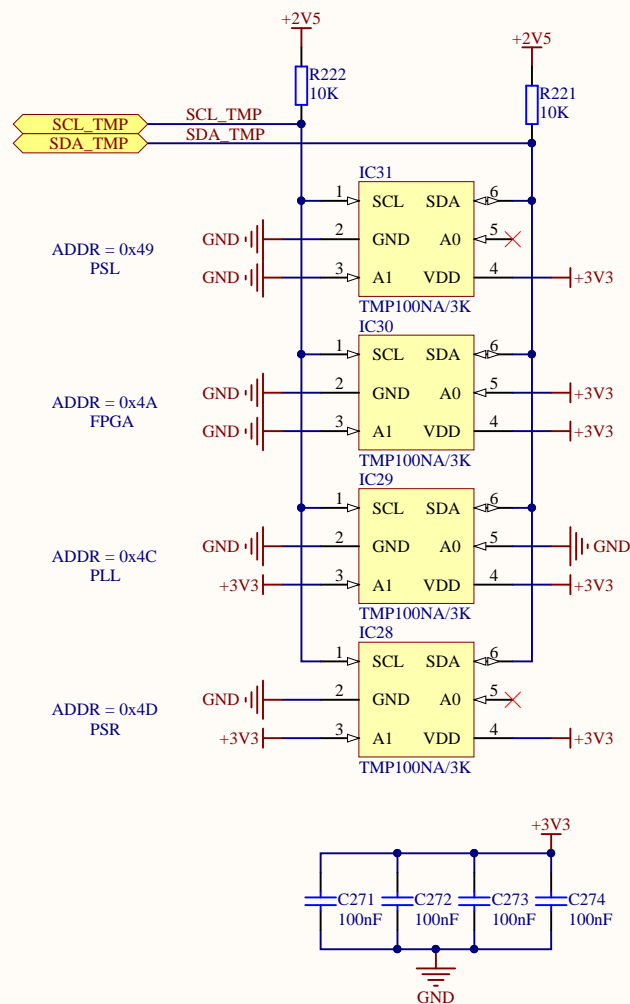
FFIX holes



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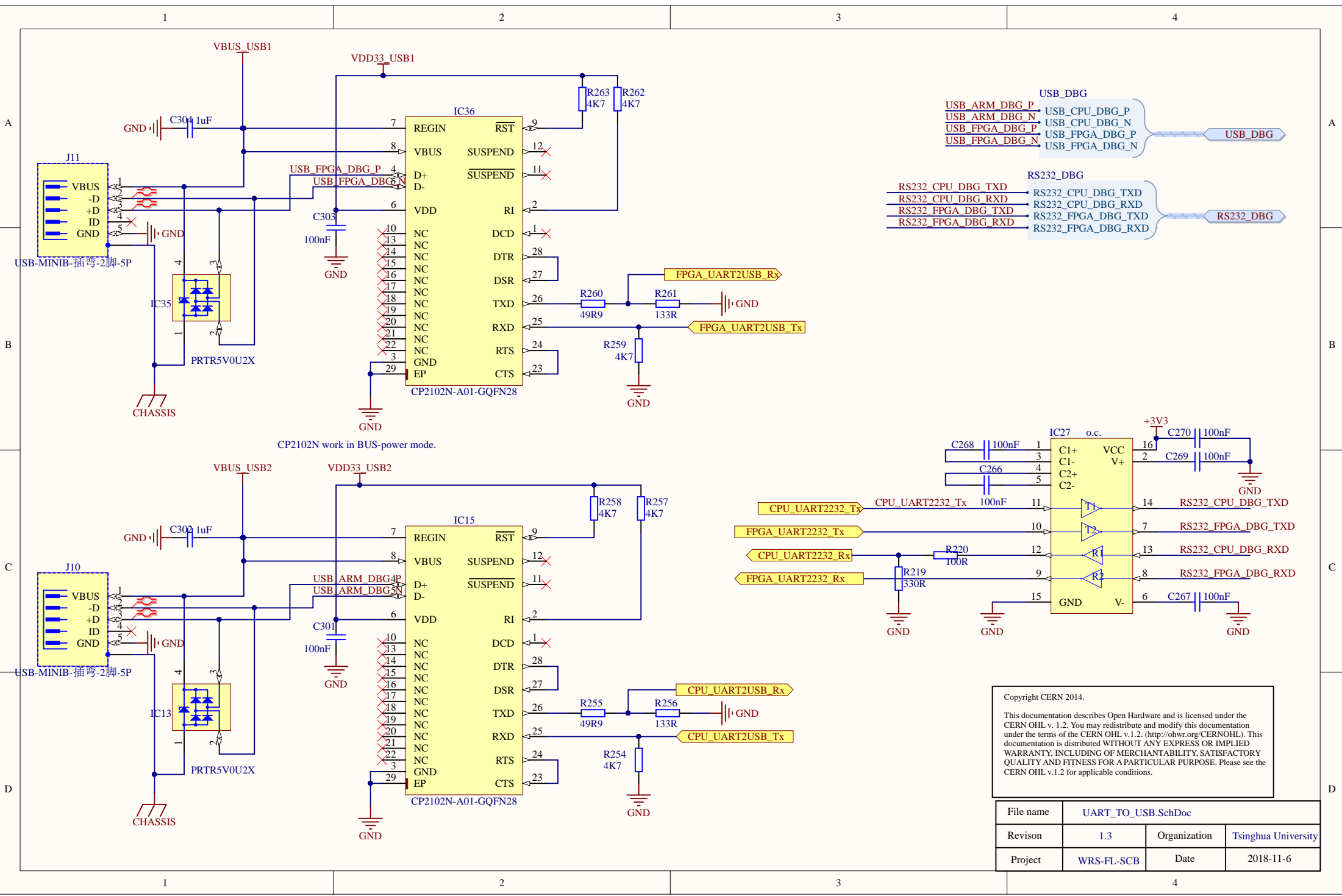
File name	PLL.SchDoc		
Revision	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2018-11-6



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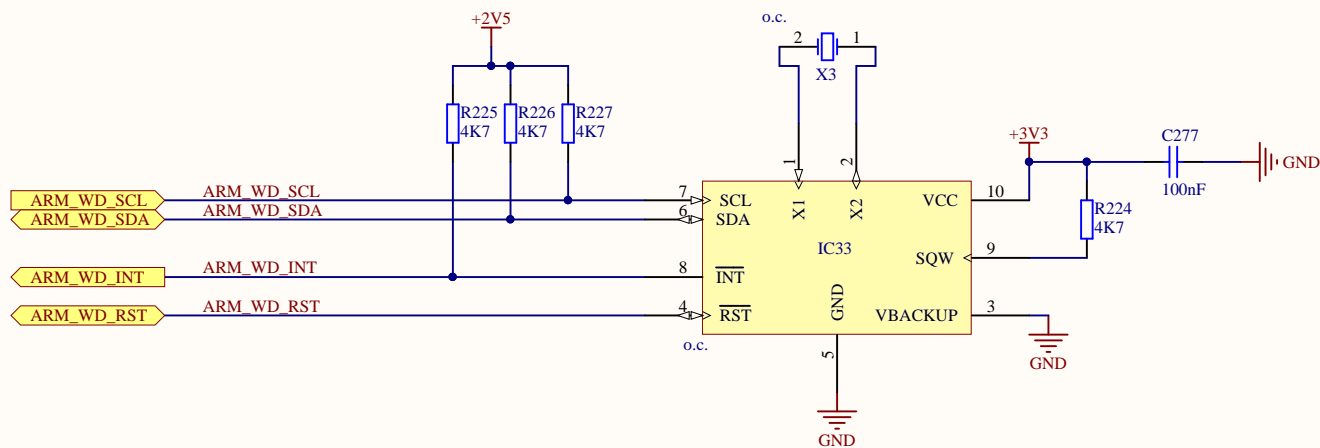
File name	SENSOR.SchDoc		
Revision	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2018-11-6



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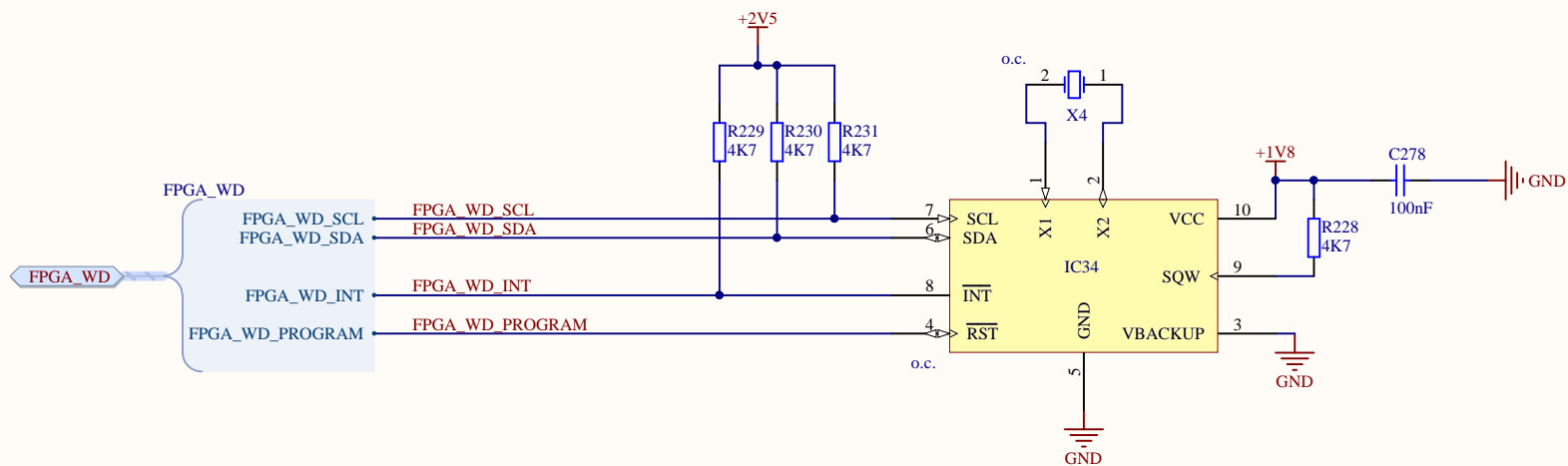
File name	UART_TO_USB.SchDoc		
Revision	1.3	Organization	Tsinghua University
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Revision	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2018-11-6