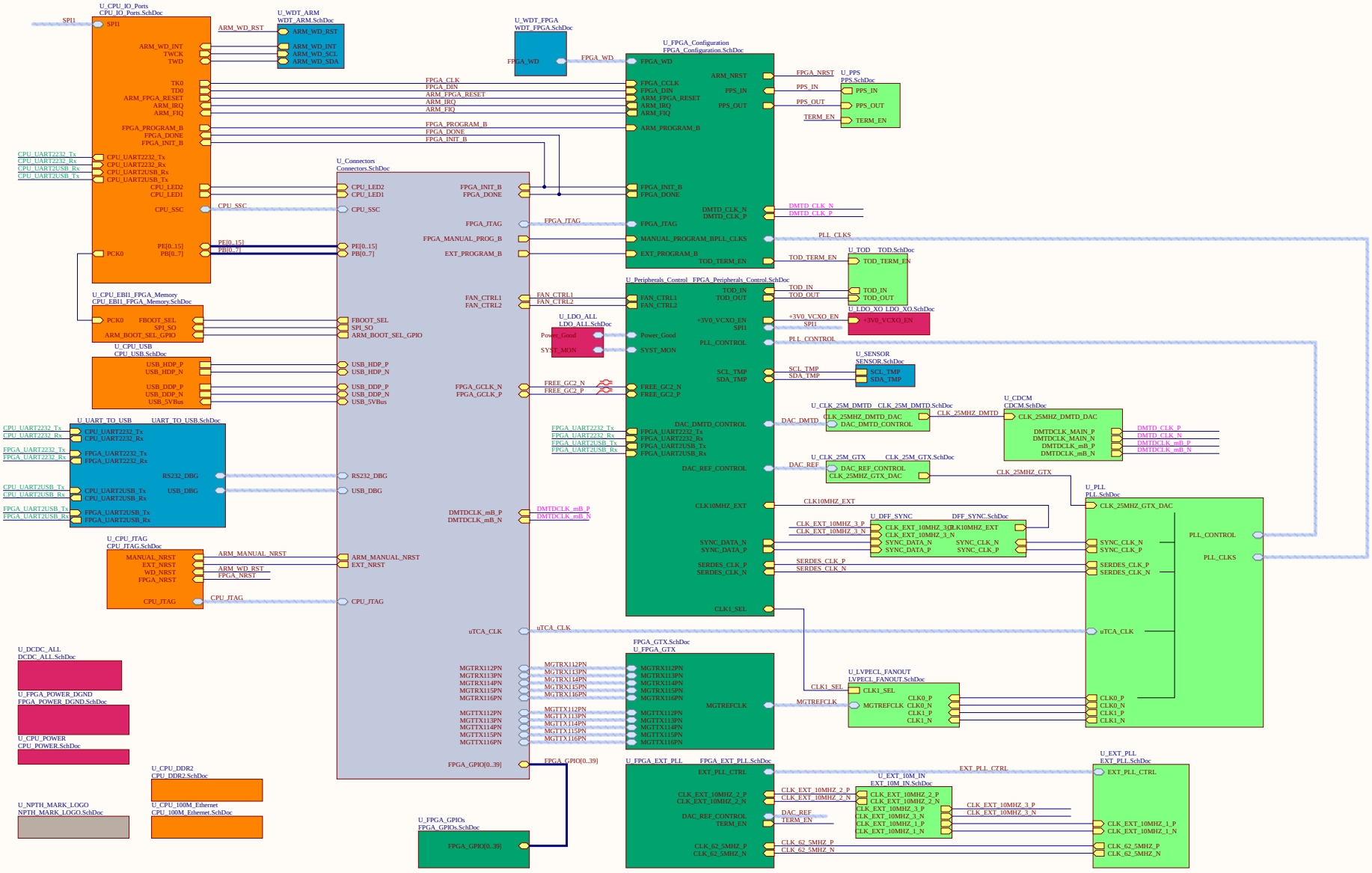
U_CPU_IO_Ports
CPU_IO_Ports.SchDoc
U_WDT_ARM
WDT_ARM.SchDoc
U_WDT_FPGA
WDT_FPGA.SchDoc
U_FPGA_Configuration
FPGA_Configuration.SchDoc
U_PPS
PPS.SchDoc
U_Connectors
Connectors.SchDoc
U_CPU_EBI1_FPGA_Memory
CPU_EBI1_FPGA_Memory.SchDoc
U_CPU_USB
CPU_USB.SchDoc
U_LDO_ALL
LDO_ALL.SchDoc
U_LDO_XO
LDO_XO.SchDoc
U_SENSOR
SENSOR.SchDoc
U_Peripherals_Control
FPGA_Peripherals_Control.SchDoc
U_TOD
TOD.SchDoc
U_CDCM
CDCM.SchDoc
U_CLK_25M_DMTD
CLK_25M_DMTD.SchDoc
U_CLK_25M_GTX
CLK_25M_GTX.SchDoc
U_UART_TO_USB
UART_TO_USB.SchDoc
U_CPU_JTAG
CPU_JTAG.SchDoc
U_PLL
PLL.SchDoc
U_DFF_SYNC
DFF_SYNC.SchDoc
U_LVPECL_FANOUT
LVPECL_FANOUT.SchDoc
U_FPGA_GTX
FPGA_GTX.SchDoc
U_FPGA_EXT_PLL
FPGA_EXT_PLL.SchDoc
U_EXT_10M_IN
EXT_10M_IN.SchDoc
U_EXT_PLL
EXT_PLL.SchDoc
U_FPGA_GPIOs
FPGA_GPIOs.SchDoc
U_DCDC_ALL
DCDC_ALL.SchDoc
U_FPGA_POWER_DGND
FPGA_POWER_DGND.SchDoc
U_CPU_POWER
CPU_POWER.SchDoc
U_CPU_DDR2
CPU_DDR2.SchDoc
U_NPTH_MARK_LOGO
NPTH_MARK_LOGO.SchDoc
U_CPU_100M_Ethernet
CPU_100M_Ethernet.SchDoc
SPI1
ARM_WD_RST
ARM_WD_INT
TWCK
TWD
TK0
TD0
ARM_FPGA_RESET
ARM_IRQ
ARM_FIQ
FPGA_PROGRAM_B
FPGA_DONE
FPGA_INIT_B
FPGA_CLK
FPGA_DIN
CPU_UART2232_Tx
CPU_UART2232_Rx
CPU_UART2USB_Rx
CPU_UART2USB_Tx
CPU_LED2
CPU_LED1
CPU_SSC
PE[0..15]
PB[0..7]
PCK0
FBOOT_SEL
SPI_SO
ARM_BOOT_SEL_GPIO
USB_HDP_P
USB_HDP_N
USB_DDP_P
USB_DDP_N
USB_5VBus
FPGA_JTAG
FPGA_MANUAL_PROG_B
EXT_PROGRAM_B
FAN_CTRL1
FAN_CTRL2
Power_Good
SYST_MON
FREE_GC2_N
FREE_GC2_P
FPGA_GCLK_N
FPGA_GCLK_P
FPGA_UART2232_Tx
FPGA_UART2232_Rx
FPGA_UART2USB_Tx
FPGA_UART2USB_Rx
RS232_DBG
USB_DBG
DMTDCLK_mB_P
DMTDCLK_mB_N
ARM_MANUAL_NRST
EXT_NRST
WD_NRST
FPGA_NRST
CPU_JTAG
uTCA_CLK
MGTRX112PN
MGTRX113PN
MGTRX114PN
MGTRX115PN
MGTRX116PN
MGTTX112PN
MGTTX113PN
MGTTX114PN
MGTTX115PN
MGTTX116PN
MGTREFCLK
FPGA_GPIO[0..39]
ARM_NRST
PPS_IN
PPS_OUT
TERM_EN
DMTD_CLK_N
DMTD_CLK_P
MANUAL_PROGRAM_BPLL_CLKS
PLL_CLKS
TOD_TERM_EN
TOD_IN
TOD_OUT
+3V0_VCXO_EN
SPI1
PLL_CONTROL
SCL_TMP
SDA_TMP
CLK_25MHZ_DMTD
DAC_DMTD
DAC_DMTD_CONTROL
DAC_REF
DAC_REF_CONTROL
CLK_25MHZ_GTX
CLK10MHZ_EXT
CLK_EXT_10MHZ_3_P
CLK_EXT_10MHZ_3_N
SYNC_DATA_N
SYNC_DATA_P
SERDES_CLK_P
SERDES_CLK_N
CLK1_SEL
EXT_PLL_CTRL
CLK_EXT_10MHZ_2_P
CLK_EXT_10MHZ_2_N
CLK_EXT_10MHZ_3_P
CLK_EXT_10MHZ_3_N
CLK_EXT_10MHZ_1_P
CLK_EXT_10MHZ_1_N
CLK_62_5MHZ_P
CLK_62_5MHZ_N
TERM_EN
CLK0_P
CLK0_N
CLK1_P
CLK1_N
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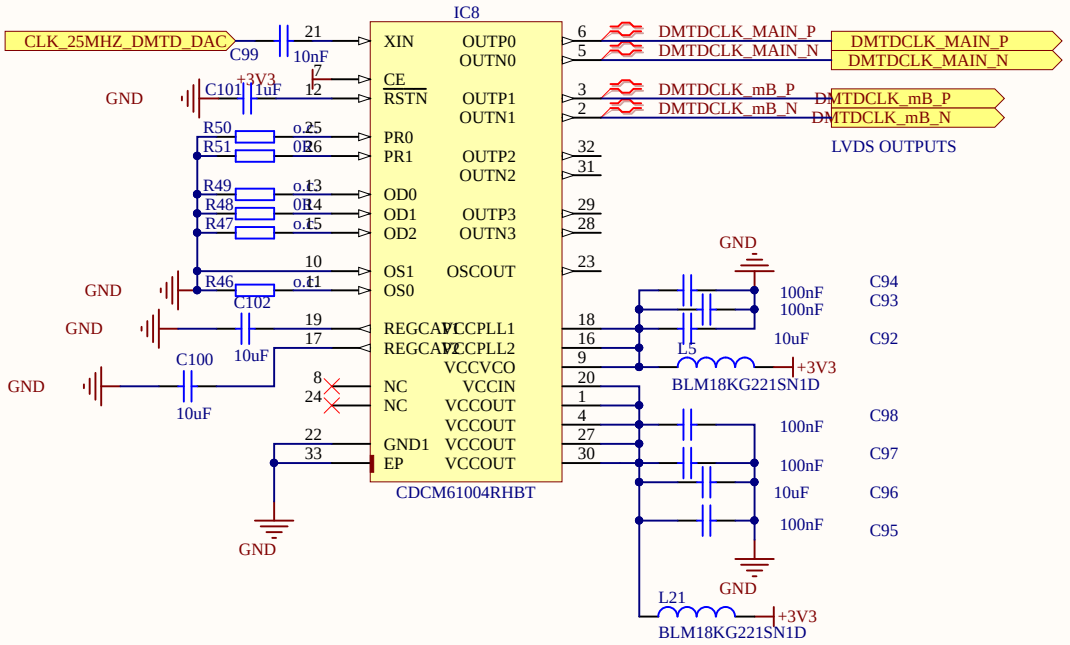
File name
SCB_MAIN.SchDoc
Revison
1.5
Organization
Tsinghua University
Project
WRS-FL-SCB
Date
2023/12/9

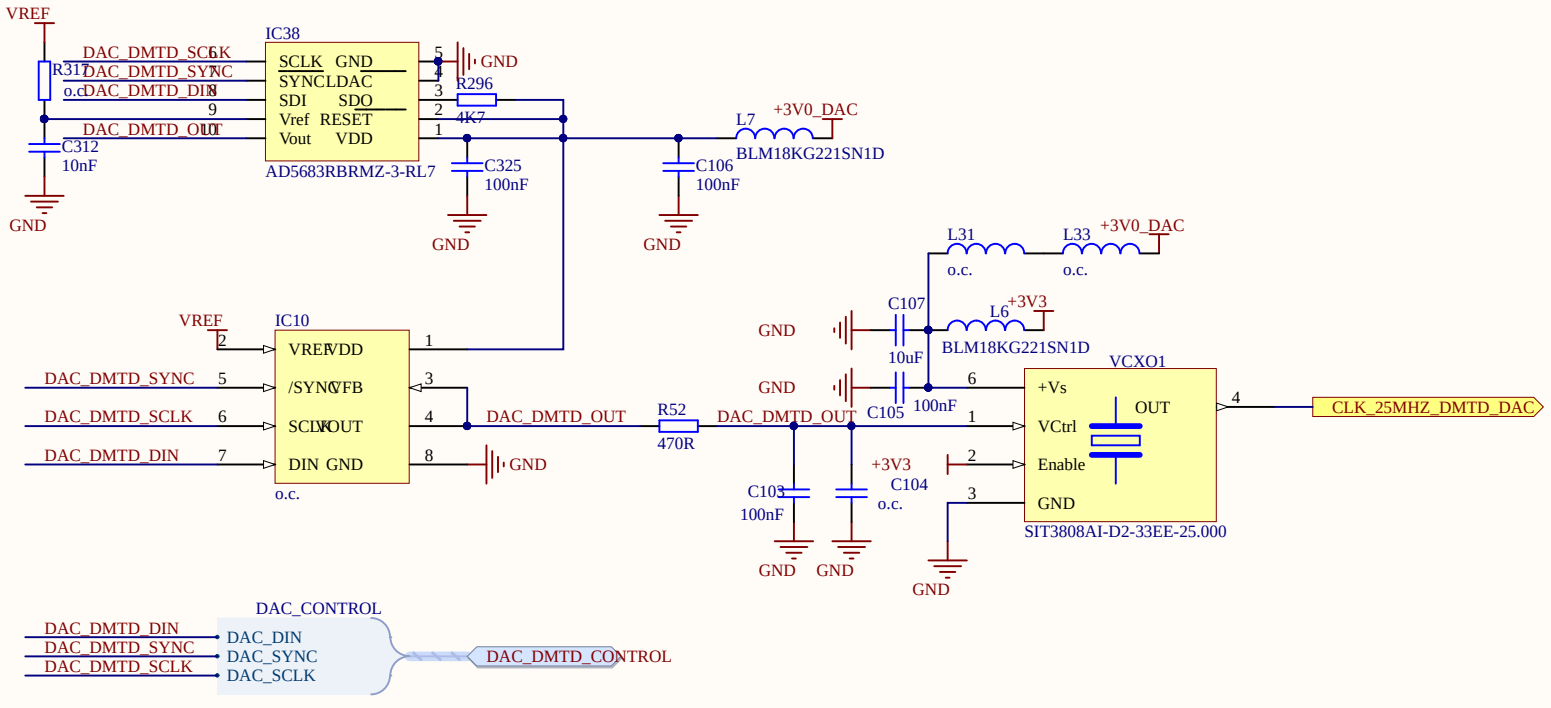
Input = 25 MHz
Output=62.5 MHz
PRESC DIV = 5
FB DIV = 15
OUT DIV = 6
PR[1:0] = 01
OD[2:0] = 101

62.5MHz Clock for the DMTD Phase Detector in FPGA (LVDS)

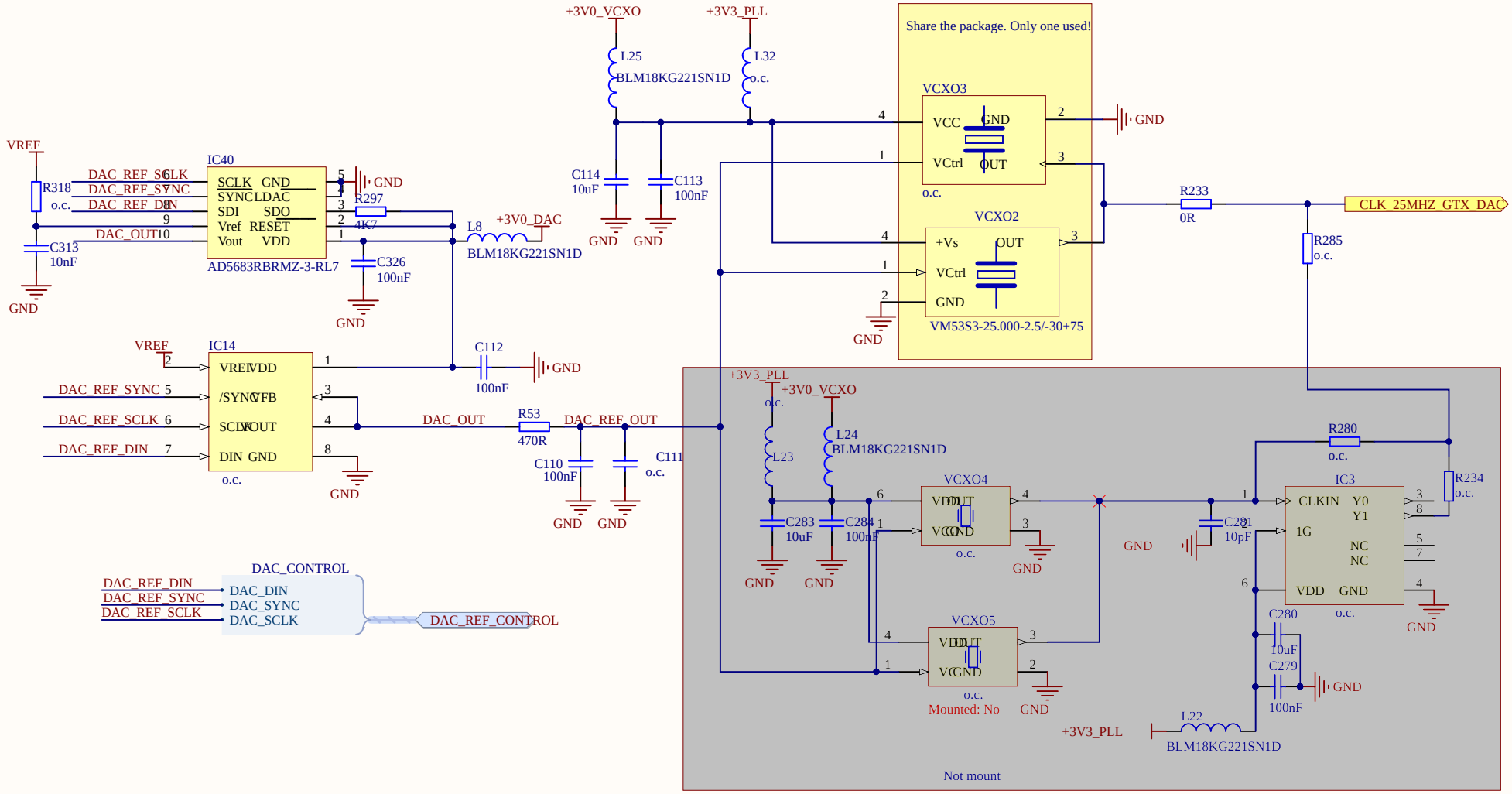
Change C101 to bigger value, to increase the reset time.
Refer to WRS-workpackage https://www.ohwr.org/projects/wr-switch-hw/work_packages/details/907/overview



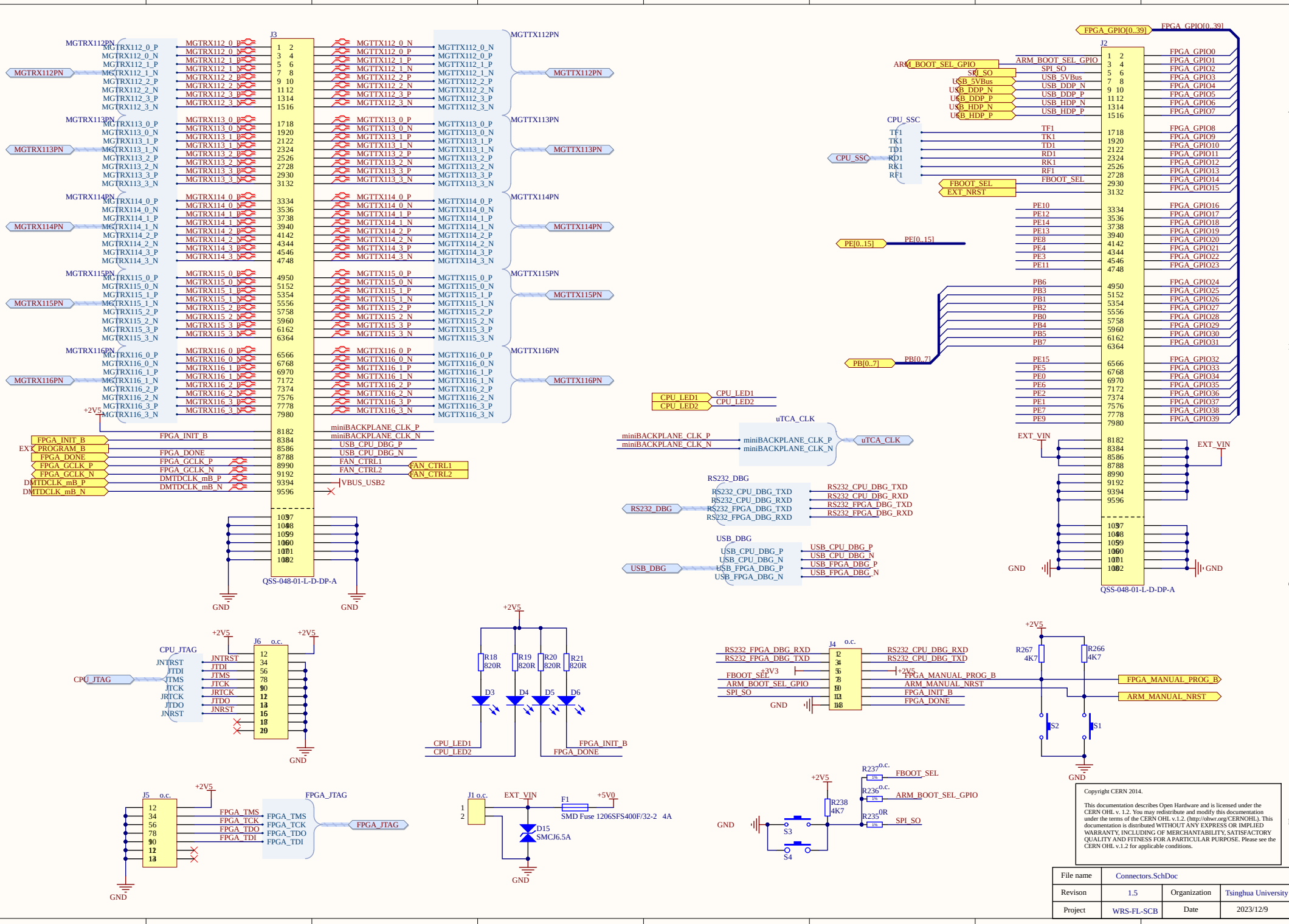
File name	CDCM.SchDoc		
Revison	1.5	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2023/12/9



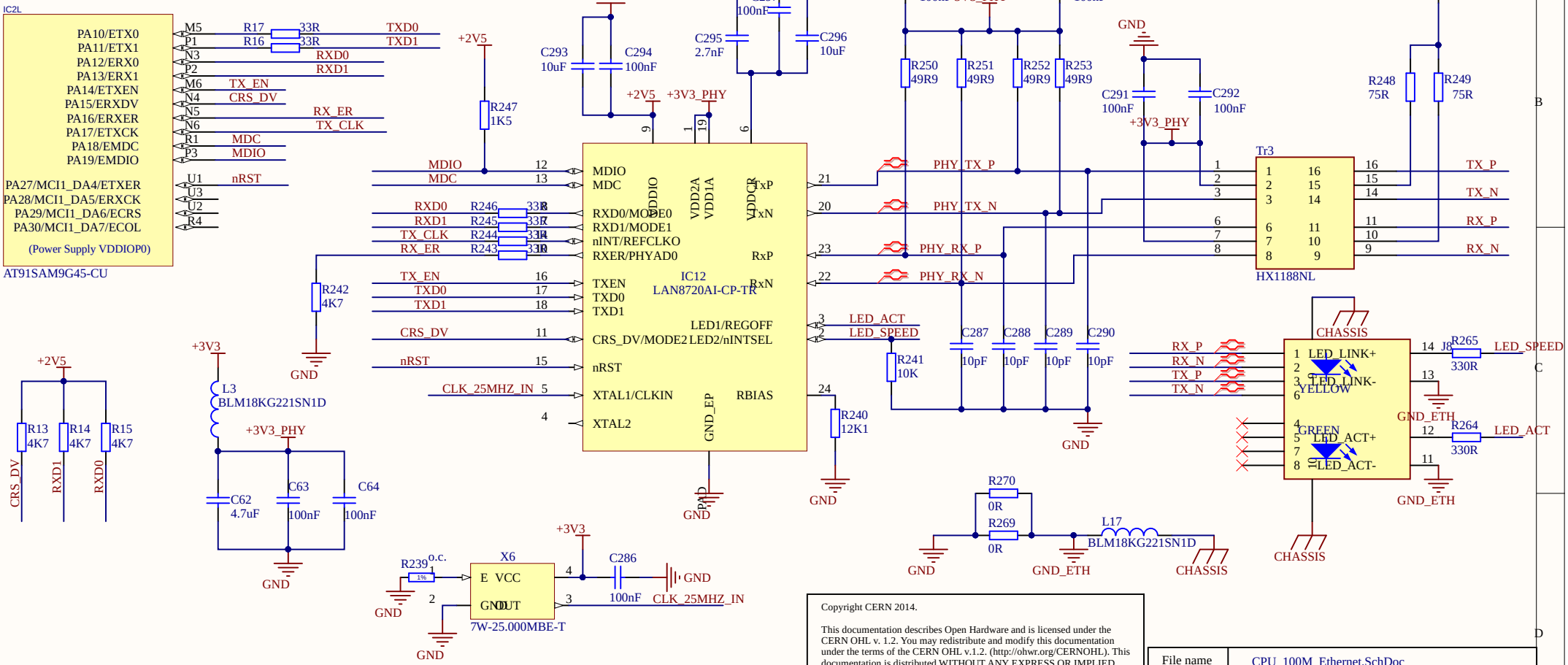
File name	CLK_25M_DMTD.SchDoc		
Revison	1.5	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2023/12/9



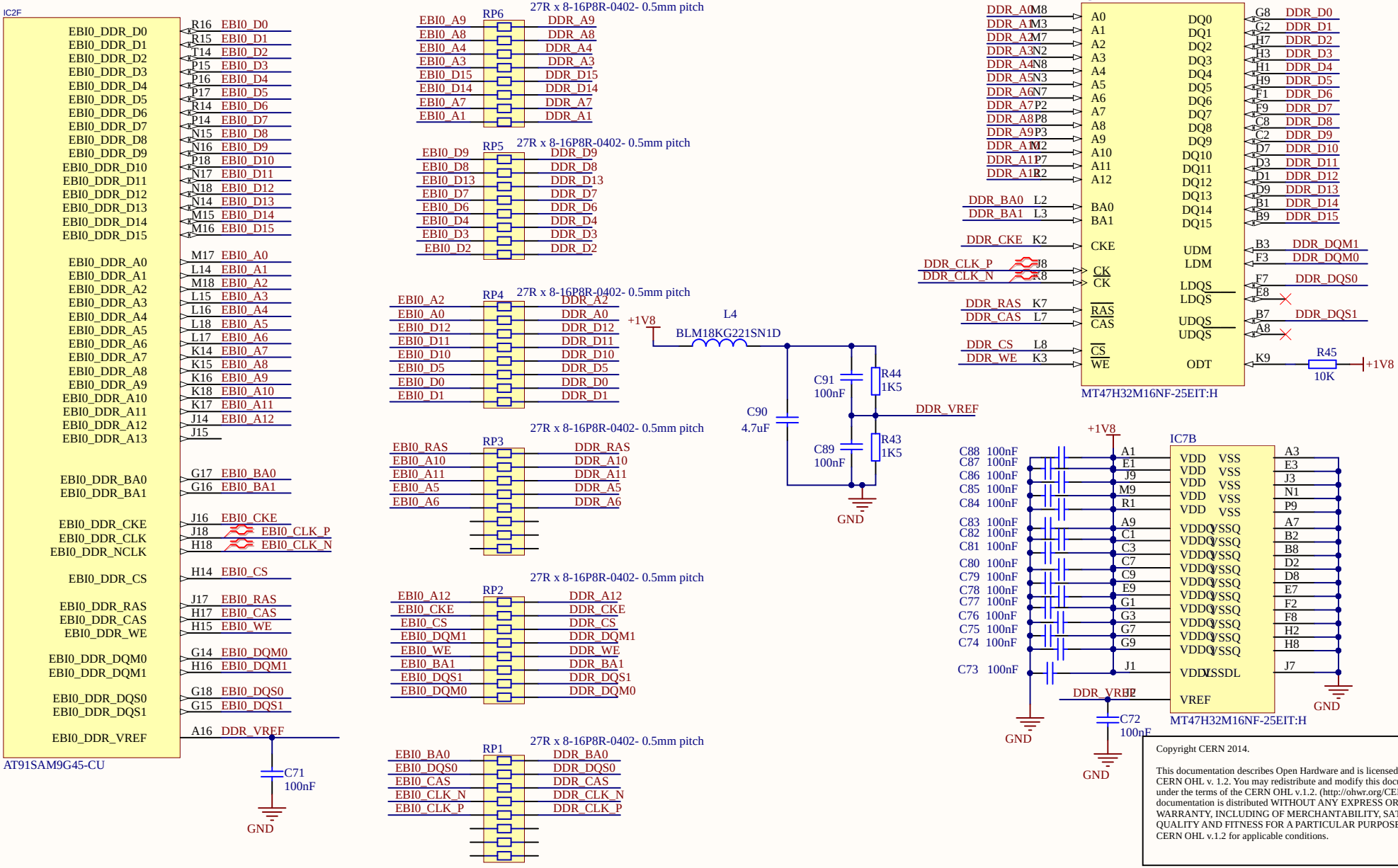
File name	CLK_25M_GTX.SchDoc		
Revison	1.5	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2023/12/9



File name	Connectors.SchDoc		
Revison	1.5	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2023/12/9



File name	CPU_100M_Ethernet.SchDoc		
Revison	1.5	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2023/12/9


IC2F
EBI0_DDR_D0
EBI0_DDR_D1
EBI0_DDR_D2
EBI0_DDR_D3
EBI0_DDR_D4
EBI0_DDR_D5
EBI0_DDR_D6
EBI0_DDR_D7
EBI0_DDR_D8
EBI0_DDR_D9
EBI0_DDR_D10
EBI0_DDR_D11
EBI0_DDR_D12
EBI0_DDR_D13
EBI0_DDR_D14
EBI0_DDR_D15
EBI0_DDR_A0
EBI0_DDR_A1
EBI0_DDR_A2
EBI0_DDR_A3
EBI0_DDR_A4
EBI0_DDR_A5
EBI0_DDR_A6
EBI0_DDR_A7
EBI0_DDR_A8
EBI0_DDR_A9
EBI0_DDR_A10
EBI0_DDR_A11
EBI0_DDR_A12
EBI0_DDR_A13
EBI0_DDR_BA0
EBI0_DDR_BA1
EBI0_DDR_CKE
EBI0_DDR_CLK
EBI0_DDR_NCLK
EBI0_DDR_CS
EBI0_DDR_RAS
EBI0_DDR_CAS
EBI0_DDR_WE
EBI0_DDR_DQM0
EBI0_DDR_DQM1
EBI0_DDR_DQS0
EBI0_DDR_DQS1
EBI0_DDR_VREF
R16 EBI0_D0
R15 EBI0_D1
T14 EBI0_D2
P15 EBI0_D3
P16 EBI0_D4
P17 EBI0_D5
R14 EBI0_D6
P14 EBI0_D7
N15 EBI0_D8
N16 EBI0_D9
P18 EBI0_D10
N17 EBI0_D11
N18 EBI0_D12
N14 EBI0_D13
M15 EBI0_D14
M16 EBI0_D15
M17 EBI0_A0
L14 EBI0_A1
M18 EBI0_A2
L15 EBI0_A3
L16 EBI0_A4
L18 EBI0_A5
L17 EBI0_A6
K14 EBI0_A7
K15 EBI0_A8
K16 EBI0_A9
K18 EBI0_A10
K17 EBI0_A11
J14 EBI0_A12
J15
G17 EBI0_BA0
G16 EBI0_BA1
J16 EBI0_CKE
J18 EBI0_CLK_P
H18 EBI0_CLK_N
H14 EBI0_CS
J17 EBI0_RAS
H17 EBI0_CAS
H15 EBI0_WE
G14 EBI0_DQM0
H16 EBI0_DQM1
G18 EBI0_DQS0
G15 EBI0_DQS1
A16 DDR_VREF
AT91SAM9G45-CU
C71
100nF
GND
RP6
27R x 8-16P8R-0402- 0.5mm pitch
EBI0_A9 DDR_A9
EBI0_A8 DDR_A8
EBI0_A4 DDR_A4
EBI0_A3 DDR_A3
EBI0_D15 DDR_D15
EBI0_D14 DDR_D14
EBI0_A7 DDR_A7
EBI0_A1 DDR_A1
RP5
27R x 8-16P8R-0402- 0.5mm pitch
EBI0_D9 DDR_D9
EBI0_D8 DDR_D8
EBI0_D13 DDR_D13
EBI0_D7 DDR_D7
EBI0_D6 DDR_D6
EBI0_D4 DDR_D4
EBI0_D3 DDR_D3
EBI0_D2 DDR_D2
RP4
27R x 8-16P8R-0402- 0.5mm pitch
EBI0_A2 DDR_A2
EBI0_A0 DDR_A0
EBI0_D12 DDR_D12
EBI0_D11 DDR_D11
EBI0_D10 DDR_D10
EBI0_D5 DDR_D5
EBI0_D0 DDR_D0
EBI0_D1 DDR_D1
RP3
27R x 8-16P8R-0402- 0.5mm pitch
EBI0_RAS DDR_RAS
EBI0_A10 DDR_A10
EBI0_A11 DDR_A11
EBI0_A5 DDR_A5
EBI0_A6 DDR_A6
RP2
27R x 8-16P8R-0402- 0.5mm pitch
EBI0_A12 DDR_A12
EBI0_CKE DDR_CKE
EBI0_CS DDR_CS
EBI0_DQM1 DDR_DQM1
EBI0_WE DDR_WE
EBI0_BA1 DDR_BA1
EBI0_DQS1 DDR_DQS1
EBI0_DQM0 DDR_DQM0
RP1
27R x 8-16P8R-0402- 0.5mm pitch
EBI0_BA0 DDR_BA0
EBI0_DQS0 DDR_DQS0
EBI0_CAS DDR_CAS
EBI0_CLK_N DDR_CLK_N
EBI0_CLK_P DDR_CLK_P
+1V8
L4
BLM18KG221SN1D
C91
100nF
C90
4.7uF
C89
100nF
R44
1K5
R43
1K5
DDR_VREF
GND
IC7A
DDR_A0 M8
DDR_A1 M3
DDR_A2 M7
DDR_A3 N2
DDR_A4 N8
DDR_A5 N3
DDR_A6 N7
DDR_A7 P2
DDR_A8 P8
DDR_A9 P3
DDR_A10 M2
DDR_A11 P7
DDR_A12 R2
DDR_BA0 L2
DDR_BA1 L3
DDR_CKE K2
DDR_CLK_P J8
DDR_CLK_N K8
DDR_RAS K7
DDR_CAS L7
DDR_CS L8
DDR_WE K3
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12
BA0 BA1
CKE
CK CK
RAS CAS CS WE
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15
UDM LDM LDQS UDQS UDQS
ODT
G8 DDR_D0
G2 DDR_D1
H7 DDR_D2
H3 DDR_D3
H1 DDR_D4
H9 DDR_D5
F1 DDR_D6
F9 DDR_D7
C8 DDR_D8
C2 DDR_D9
D7 DDR_D10
D3 DDR_D11
D1 DDR_D12
D9 DDR_D13
B1 DDR_D14
B9 DDR_D15
B3 DDR_DQM1
F3 DDR_DQM0
F7 DDR_DQS0
E8
B7 DDR_DQS1
A8
K9
R45
10K
+1V8
MT47H32M16NF-25EIT:H
+1V8
IC7B
C88 100nF
C87 100nF
C86 100nF
C85 100nF
C84 100nF
C83 100nF
C82 100nF
C81 100nF
C80 100nF
C79 100nF
C78 100nF
C77 100nF
C76 100nF
C75 100nF
C74 100nF
C73 100nF
A1 E1 J9 M9 R1
A9 C1 C3 C7 C9 E9 G1 G3 G7 G9 J1
VDD VSS
VDDQ VSSQ
VDDL VSSDL
VREF
A3 E3 J3 N1 P9 A7 B2 B8 D2 D8 E7 F2 F8 H2 H8 J7
DDR_VREF
C72
100nF
GND
MT47H32M16NF-25EIT:H
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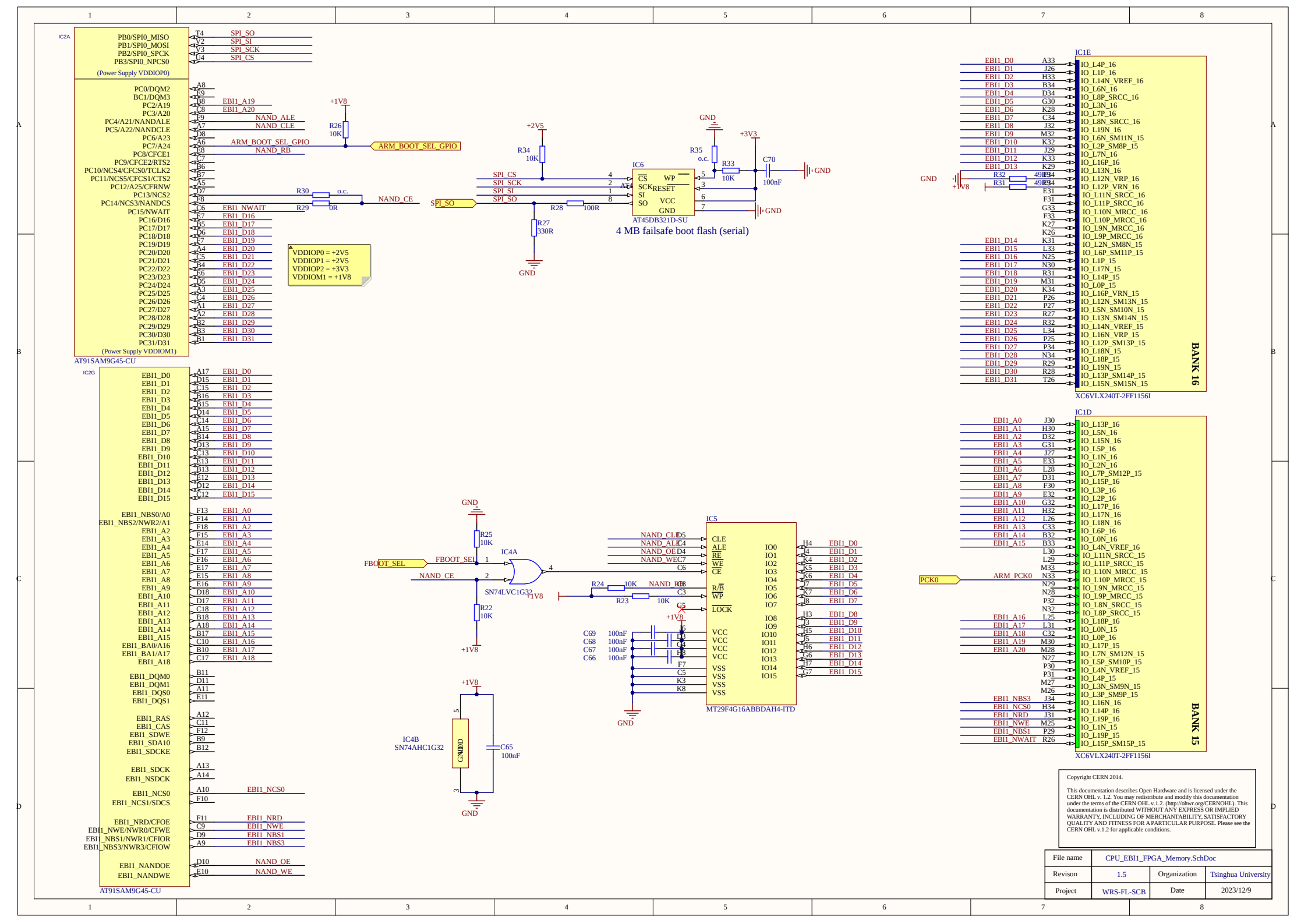
File name CPU_DDR2.SchDoc
Revison 1.5
Organization Tsinghua University
Project WRS-FL-SCB
Date 2023/12/9


IC2A
PB0/SPI0_MISO
PB1/SPI0_MOSI
PB2/SPI0_SPCK
PB3/SPI0_NPCS0
(Power Supply VDDIOP0)
PC0/DQM2
PC1/DQM3
PC2/A19
PC3/A20
PC4/A21/NANDALE
PC5/A22/NANDCLE
PC6/A23
PC7/A24
PC8/CFCE1
PC9/CFCE2/RTS2
PC10/NCS4/CFCS0/TCLK2
PC11/NCS5/CFCS1/CTS2
PC12/A25/CFRNW
PC13/NCS2
PC14/NCS3/NANDCS
PC15/NWAIT
PC16/D16
PC17/D17
PC18/D18
PC19/D19
PC20/D20
PC21/D21
PC22/D22
PC23/D23
PC24/D24
PC25/D25
PC26/D26
PC27/D27
PC28/D28
PC29/D29
PC30/D30
PC31/D31
(Power Supply VDDIOM1)
AT91SAM9G45-CU
SPI_SO
SPI_SI
SPI_SCK
SPI_CS
EBI1_A19
EBI1_A20
NAND_ALE
NAND_CLE
ARM_BOOT_SEL_GPIO
NAND_RB
EBI1_NWAIT
EBI1_D16
EBI1_D17
EBI1_D18
EBI1_D19
EBI1_D20
EBI1_D21
EBI1_D22
EBI1_D23
EBI1_D24
EBI1_D25
EBI1_D26
EBI1_D27
EBI1_D28
EBI1_D29
EBI1_D30
EBI1_D31
+1V8
R26
10K
R30
o.c.
0R
R29
NAND_CE
VDDIOP0 = +2V5
VDDIOP1 = +2V5
VDDIOP2 = +3V3
VDDIOM1 = +1V8
+2V5
R34
10K
SPI_CS
SPI_SCK
SPI_SI
SPI_SO
SPI_SO
R28
100R
R27
330R
GND
IC6
CS
SCK
SI
SO
WP
RESET
VCC
GND
AT45DB321D-SU
4 MB failsafe boot flash (serial)
+3V3
R35
o.c.
R33
10K
C70
100nF
GND
IC1E
EBI1_D0
EBI1_D1
EBI1_D2
EBI1_D3
EBI1_D4
EBI1_D5
EBI1_D6
EBI1_D7
EBI1_D8
EBI1_D9
EBI1_D10
EBI1_D11
EBI1_D12
EBI1_D13
R32
R31
EBI1_D14
EBI1_D15
EBI1_D16
EBI1_D17
EBI1_D18
EBI1_D19
EBI1_D20
EBI1_D21
EBI1_D22
EBI1_D23
EBI1_D24
EBI1_D25
EBI1_D26
EBI1_D27
EBI1_D28
EBI1_D29
EBI1_D30
EBI1_D31
IO_L4P_16
IO_L1P_16
IO_L14N_VREF_16
IO_L6N_16
IO_L8P_SRCC_16
IO_L3N_16
IO_L7P_16
IO_L8N_SRCC_16
IO_L19N_16
IO_L6N_SM11N_15
IO_L2P_SM8P_15
IO_L7N_16
IO_L16P_16
IO_L13N_16
IO_L12N_VRP_16
IO_L12P_VRN_16
IO_L11N_SRCC_16
IO_L11P_SRCC_16
IO_L10N_MRCC_16
IO_L10P_MRCC_16
IO_L9N_MRCC_16
IO_L9P_MRCC_16
IO_L2N_SM8N_15
IO_L6P_SM11P_15
IO_L1P_15
IO_L17N_15
IO_L14P_15
IO_L0P_15
IO_L16P_VRN_15
IO_L12N_SM13N_15
IO_L5N_SM10N_15
IO_L13N_SM14N_15
IO_L14N_VREF_15
IO_L16N_VRP_15
IO_L12P_SM13P_15
IO_L18N_15
IO_L18P_15
IO_L19N_15
IO_L13P_SM14P_15
IO_L15N_SM15N_15
BANK 16
XC6VLX240T-2FF1156I
IC2G
EBI1_NBS0/A0
EBI1_NBS2/NWR2/A1
EBI1_BA0/A16
EBI1_BA1/A17
EBI1_DQM0
EBI1_DQM1
EBI1_DQS0
EBI1_DQS1
EBI1_RAS
EBI1_CAS
EBI1_SDWE
EBI1_SDA10
EBI1_SDCKE
EBI1_SDCK
EBI1_NSDCK
EBI1_NCS0
EBI1_NCS1/SDCS
EBI1_NRD/CFOE
EBI1_NWE/NWR0/CFWE
EBI1_NBS1/NWR1/CFIOR
EBI1_NBS3/NWR3/CFIOW
EBI1_NANDOE
EBI1_NANDWE
EBI1_NCS0
EBI1_NRD
EBI1_NWE
EBI1_NBS1
EBI1_NBS3
NAND_OE
NAND_WE
AT91SAM9G45-CU
GND
R25
10K
FBOOT_SEL
IC4A
SN74LVC1G32
R22
10K
+1V8
NAND_CLE
NAND_ALE
NAND_OE
NAND_WE
R24
10K
R23
10K
IC5
CLE
ALE
RE
WE
CE
R/B
WP
LOCK
VCC
VSS
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
IO10
IO11
IO12
IO13
IO14
IO15
MT29F4G16ABBDAH4-ITD
C69
C68
C67
C66
100nF
IC4B
SN74AHC1G32
C65
100nF
IC1D
EBI1_A0
EBI1_A1
EBI1_A2
EBI1_A3
EBI1_A4
EBI1_A5
EBI1_A6
EBI1_A7
EBI1_A8
EBI1_A9
EBI1_A10
EBI1_A11
EBI1_A12
EBI1_A13
EBI1_A14
EBI1_A15
PCK0
ARM_PCK0
EBI1_A16
EBI1_A17
EBI1_A18
EBI1_A19
EBI1_A20
EBI1_NBS3
EBI1_NCS0
EBI1_NRD
EBI1_NWE
EBI1_NBS1
EBI1_NWAIT
IO_L13P_16
IO_L5N_16
IO_L15N_16
IO_L5P_16
IO_L1N_16
IO_L2N_16
IO_L7P_SM12P_15
IO_L15P_16
IO_L3P_16
IO_L2P_16
IO_L17P_16
IO_L17N_16
IO_L18N_16
IO_L6P_16
IO_L0N_16
IO_L4N_VREF_16
IO_L11N_SRCC_15
IO_L11P_SRCC_15
IO_L10N_MRCC_15
IO_L10P_MRCC_15
IO_L9N_MRCC_15
IO_L9P_MRCC_15
IO_L8N_SRCC_15
IO_L8P_SRCC_15
IO_L18P_16
IO_L0N_15
IO_L0P_16
IO_L17P_15
IO_L7N_SM12N_15
IO_L5P_SM10P_15
IO_L4N_VREF_15
IO_L4P_15
IO_L3N_SM9N_15
IO_L3P_SM9P_15
IO_L16N_16
IO_L14P_16
IO_L19P_16
IO_L1N_15
IO_L19P_15
IO_L15P_SM15P_15
BANK 15
XC6VLX240T-2FF1156I
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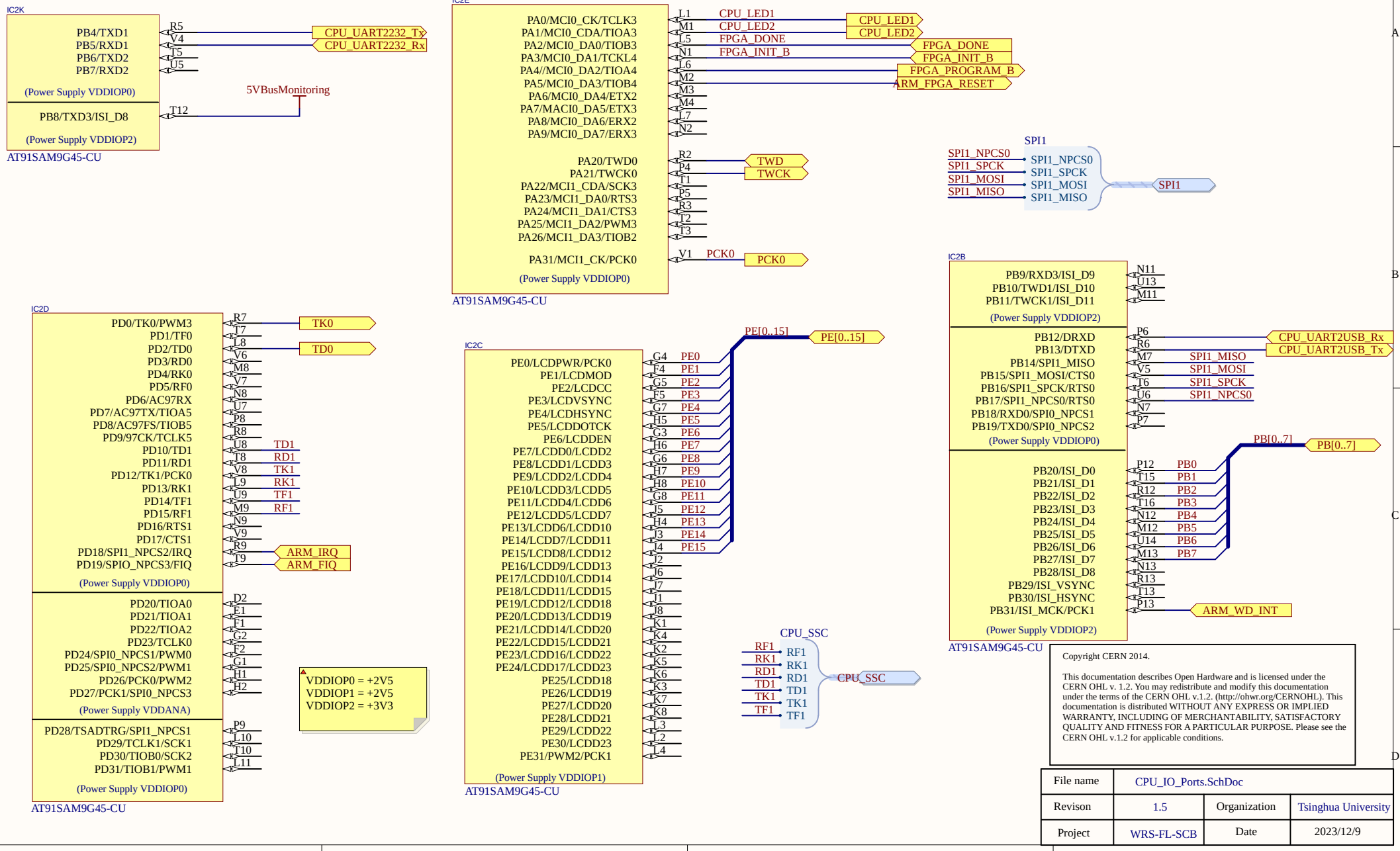
File name
CPU_EBI1_FPGA_Memory.SchDoc
Revison
1.5
Organization
Tsinghua University
Project
WRS-FL-SCB
Date
2023/12/9


IC2K
PB4/TXD1
PB5/RXD1
PB6/TXD2
PB7/RXD2
(Power Supply VDDIOP0)
PB8/TXD3/ISI_D8
(Power Supply VDDIOP2)
AT91SAM9G45-CU
R5
V4
T5
U5
T12
CPU_UART2232_Tx
CPU_UART2232_Rx
5VBusMonitoring
IC2E
PA0/MCI0_CK/TCLK3
PA1/MCI0_CDA/TIOA3
PA2/MCI0_DA0/TIOB3
PA3/MCI0_DA1/TCKL4
PA4//MCI0_DA2/TIOA4
PA5/MCI0_DA3/TIOB4
PA6/MCI0_DA4/ETX2
PA7/MACI0_DA5/ETX3
PA8/MCI0_DA6/ERX2
PA9/MCI0_DA7/ERX3
PA20/TWD0
PA21/TWCK0
PA22/MCI1_CDA/SCK3
PA23/MCI1_DA0/RTS3
PA24/MCI1_DA1/CTS3
PA25/MCI1_DA2/PWM3
PA26/MCI1_DA3/TIOB2
PA31/MCI1_CK/PCK0
(Power Supply VDDIOP0)
AT91SAM9G45-CU
L1
M1
L5
N1
L6
M2
M3
M4
L7
N2
R2
P4
T1
P5
R3
T2
T3
V1
CPU_LED1
CPU_LED2
FPGA_DONE
FPGA_INIT_B
FPGA_PROGRAM_B
ARM_FPGA_RESET
TWD
TWCK
PCK0
SPI1
SPI1_NPCS0
SPI1_SPCK
SPI1_MOSI
SPI1_MISO
IC2B
PB9/RXD3/ISI_D9
PB10/TWD1/ISI_D10
PB11/TWCK1/ISI_D11
(Power Supply VDDIOP2)
PB12/DRXD
PB13/DTXD
PB14/SPI1_MISO
PB15/SPI1_MOSI/CTS0
PB16/SPI1_SPCK/RTS0
PB17/SPI1_NPCS0/RTS0
PB18/RXD0/SPI0_NPCS1
PB19/TXD0/SPI0_NPCS2
(Power Supply VDDIOP0)
PB20/ISI_D0
PB21/ISI_D1
PB22/ISI_D2
PB23/ISI_D3
PB24/ISI_D4
PB25/ISI_D5
PB26/ISI_D6
PB27/ISI_D7
PB28/ISI_D8
PB29/ISI_VSYNC
PB30/ISI_HSYNC
PB31/ISI_MCK/PCK1
(Power Supply VDDIOP2)
AT91SAM9G45-CU
N11
U13
M11
P6
R6
M7
V5
T6
U6
N7
P7
P12
T15
R12
T16
N12
M12
U14
M13
N13
R13
T13
P13
CPU_UART2USB_Rx
CPU_UART2USB_Tx
SPI1_MISO
SPI1_MOSI
SPI1_SPCK
SPI1_NPCS0
PB[0..7]
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
ARM_WD_INT
IC2D
PD0/TK0/PWM3
PD1/TF0
PD2/TD0
PD3/RD0
PD4/RK0
PD5/RF0
PD6/AC97RX
PD7/AC97TX/TIOA5
PD8/AC97FS/TIOB5
PD9/97CK/TCLK5
PD10/TD1
PD11/RD1
PD12/TK1/PCK0
PD13/RK1
PD14/TF1
PD15/RF1
PD16/RTS1
PD17/CTS1
PD18/SPI1_NPCS2/IRQ
PD19/SPIO_NPCS3/FIQ
(Power Supply VDDIOP0)
PD20/TIOA0
PD21/TIOA1
PD22/TIOA2
PD23/TCLK0
PD24/SPI0_NPCS1/PWM0
PD25/SPI0_NPCS2/PWM1
PD26/PCK0/PWM2
PD27/PCK1/SPI0_NPCS3
(Power Supply VDDANA)
PD28/TSADTRG/SPI1_NPCS1
PD29/TCLK1/SCK1
PD30/TIOB0/SCK2
PD31/TIOB1/PWM1
(Power Supply VDDIOP0)
AT91SAM9G45-CU
R7
T7
L8
V6
M8
V7
N8
U7
P8
R8
U8
T8
V8
L9
U9
M9
N9
V9
R9
T9
D2
E1
F1
G2
F2
G1
H1
H2
P9
L10
T10
L11
TK0
TD0
TD1
RD1
TK1
RK1
TF1
RF1
ARM_IRQ
ARM_FIQ
VDDIOP0 = +2V5
VDDIOP1 = +3V3
VDDIOP2 = +3V3
IC2C
PE0/LCDPWR/PCK0
PE1/LCDMOD
PE2/LCDCC
PE3/LCDVSYNC
PE4/LCDHSYNC
PE5/LCDDOTCK
PE6/LCDDEN
PE7/LCDD0/LCDD2
PE8/LCDD1/LCDD3
PE9/LCDD2/LCDD4
PE10/LCDD3/LCDD5
PE11/LCDD4/LCDD6
PE12/LCDD5/LCDD7
PE13/LCDD6/LCDD10
PE14/LCDD7/LCDD11
PE15/LCDD8/LCDD12
PE16/LCDD9/LCDD13
PE17/LCDD10/LCDD14
PE18/LCDD11/LCDD15
PE19/LCDD12/LCDD18
PE20/LCDD13/LCDD19
PE21/LCDD14/LCDD20
PE22/LCDD15/LCDD21
PE23/LCDD16/LCDD22
PE24/LCDD17/LCDD23
PE25/LCDD18
PE26/LCDD19
PE27/LCDD20
PE28/LCDD21
PE29/LCDD22
PE30/LCDD23
PE31/PWM2/PCK1
(Power Supply VDDIOP1)
AT91SAM9G45-CU
G4
F4
G5
F5
G7
H5
G3
H6
G6
H7
H8
G8
J5
H4
J3
J4
J2
J6
J7
J1
J8
K1
K4
K2
K5
K6
K3
K7
K8
L3
L2
L4
PE0
PE1
PE2
PE3
PE4
PE5
PE6
PE7
PE8
PE9
PE10
PE11
PE12
PE13
PE14
PE15
PE[0..15]
CPU_SSC
RF1
RK1
RD1
TD1
TK1
TF1
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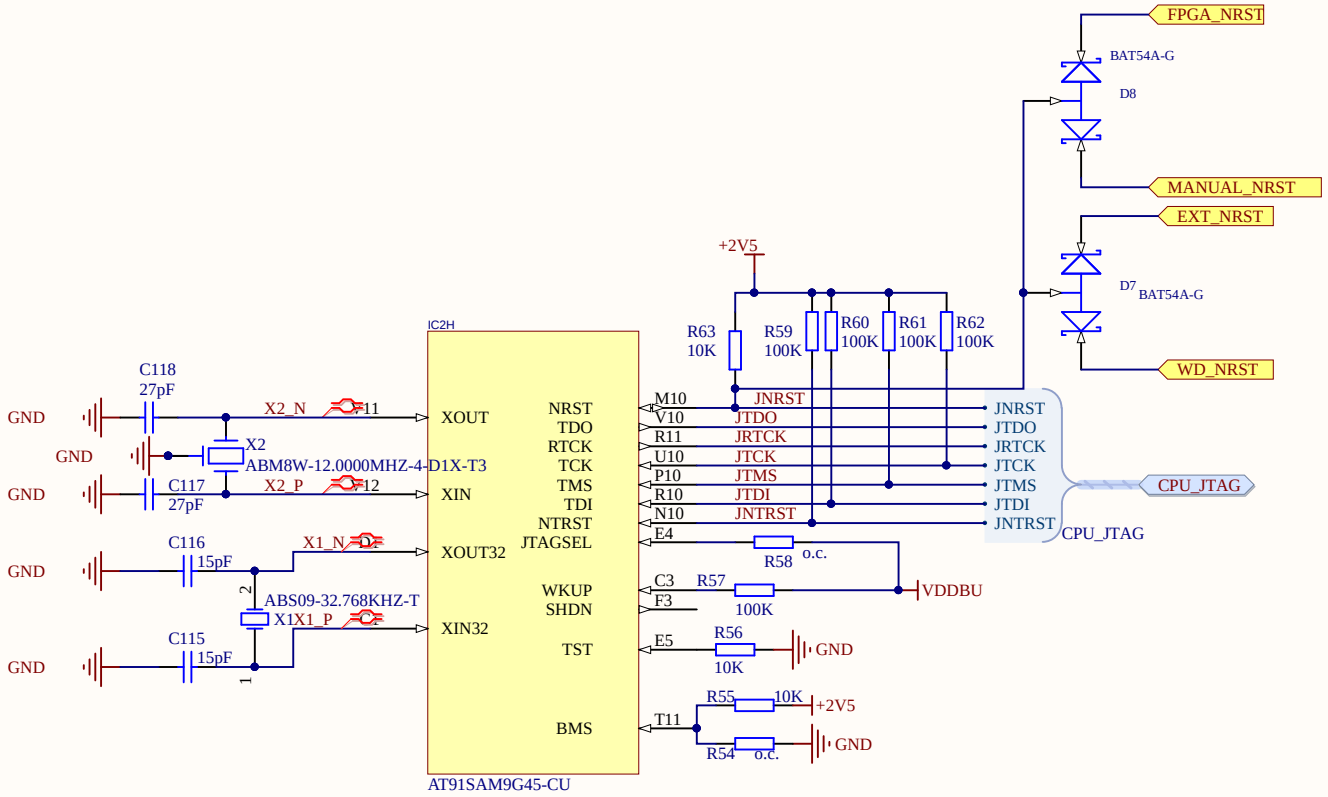
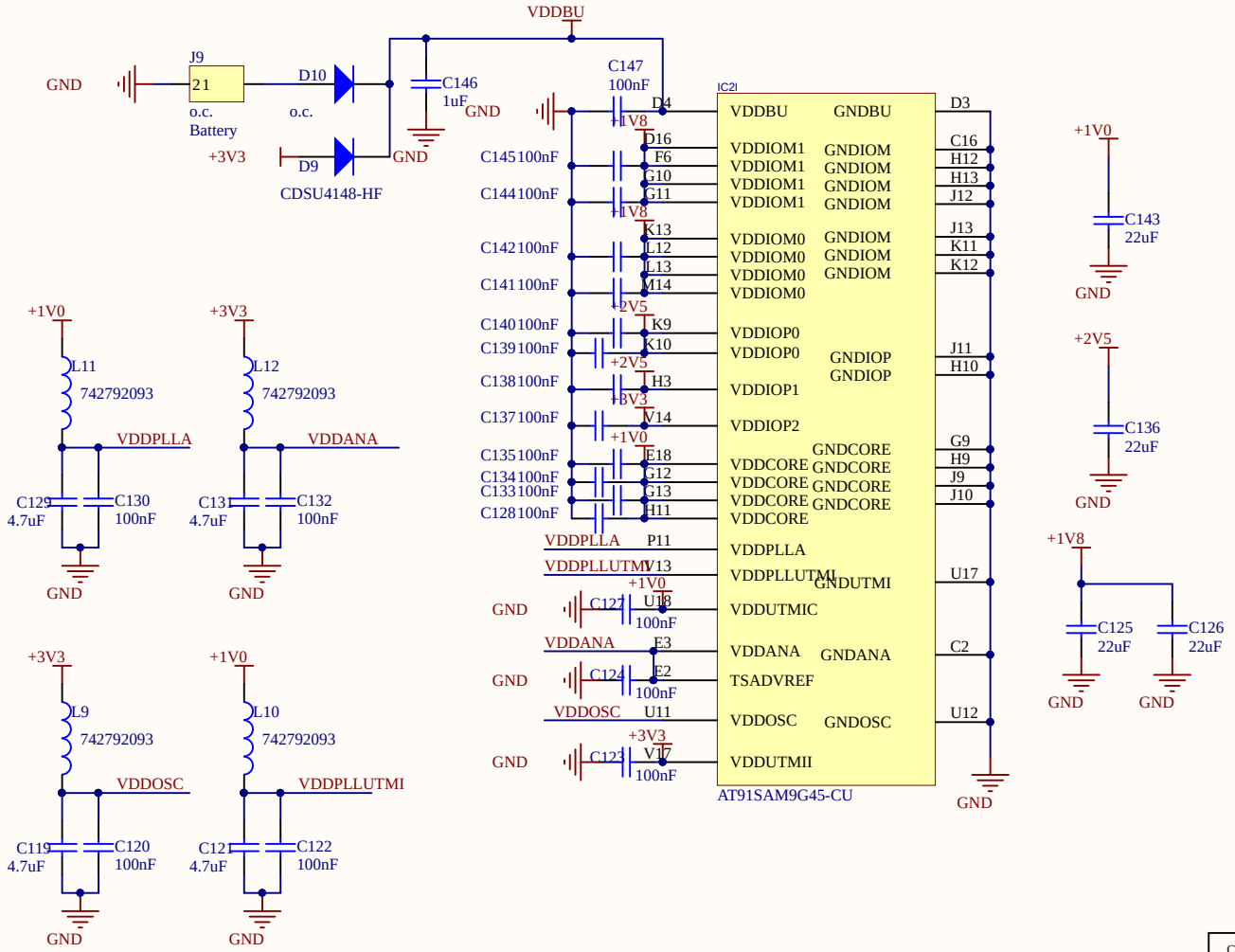
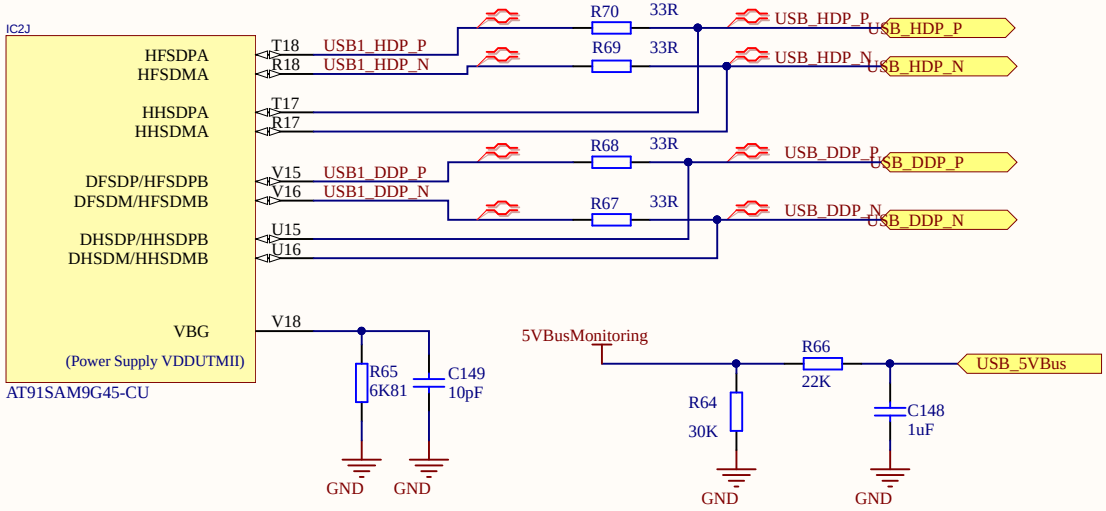
File name
CPU_IO_Ports.SchDoc
Revison
1.5
Organization
Tsinghua University
Project
WRS-FL-SCB
Date
2023/12/9



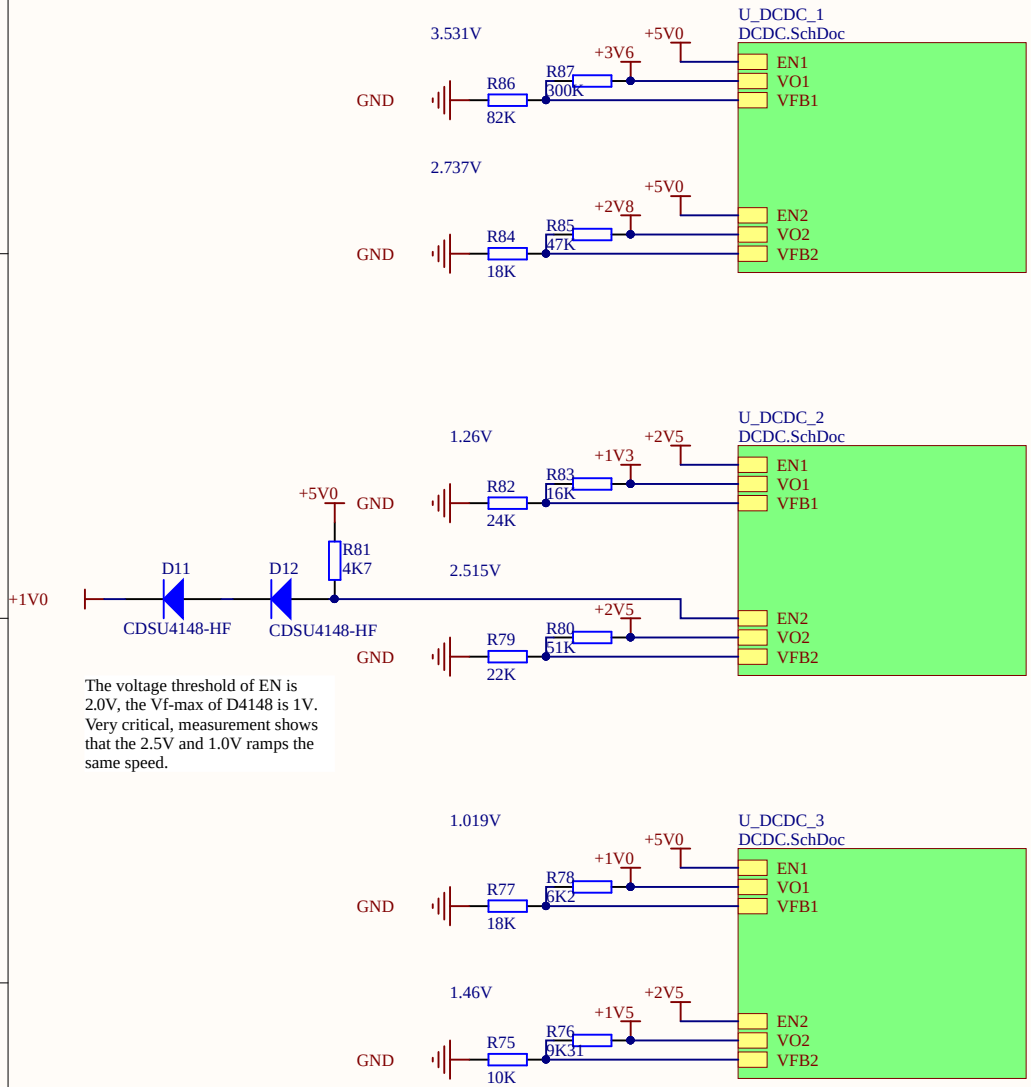
File name	CPU_JTAG.SchDoc		
Revison	1.5	Organization	Tsinghua University
Project	White Rabbit	Date	2023/12/9



File name	CPU_POWER.SchDoc		
Revison	1.5	Organization	Tsinghua University
Project	White Rabbit	Date	2023/12/9



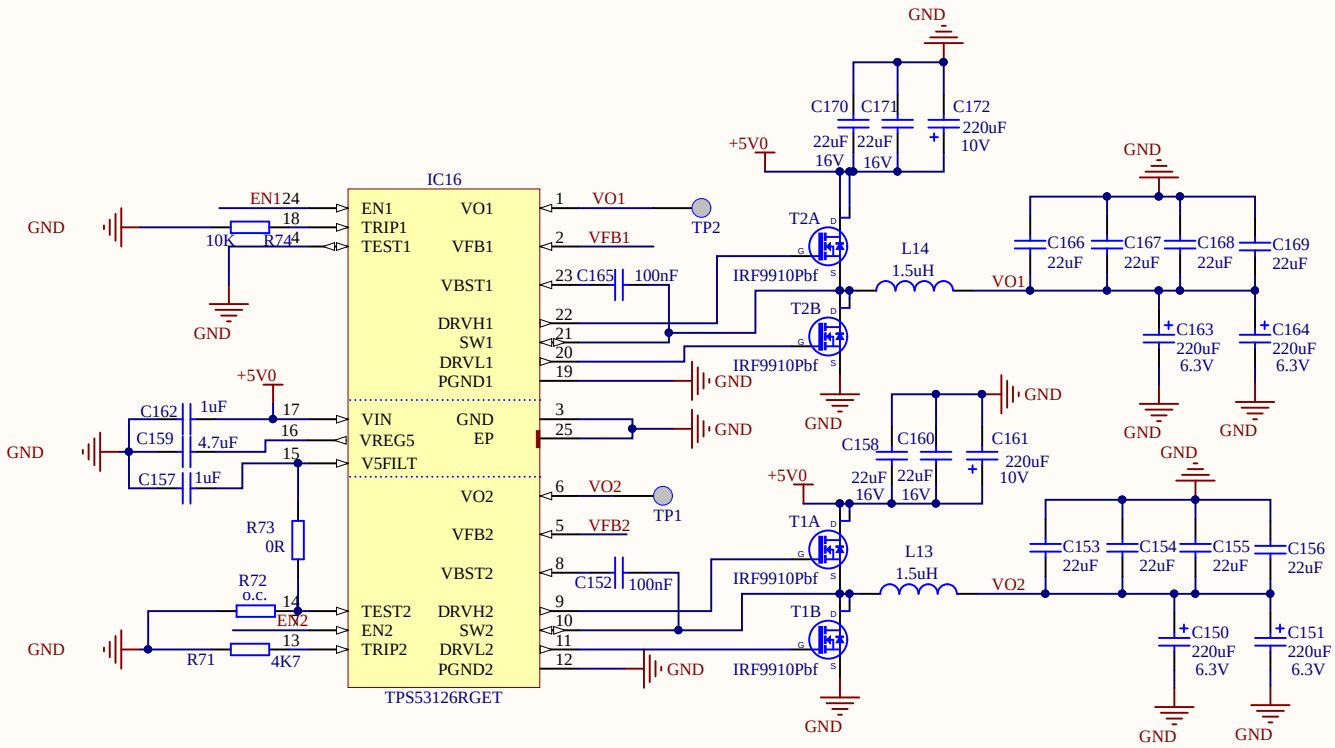
File name	CPU_USB.SchDoc		
Revison	1.5	Organization	Tsinghua University
Project	White Rabbit	Date	2023/12/9

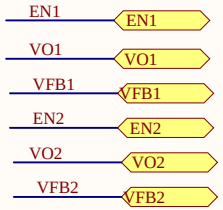


The voltage threshold of EN is 2.0V, the Vf-max of D4148 is 1V. Very critical, measurement shows that the 2.5V and 1.0V ramps the same speed.

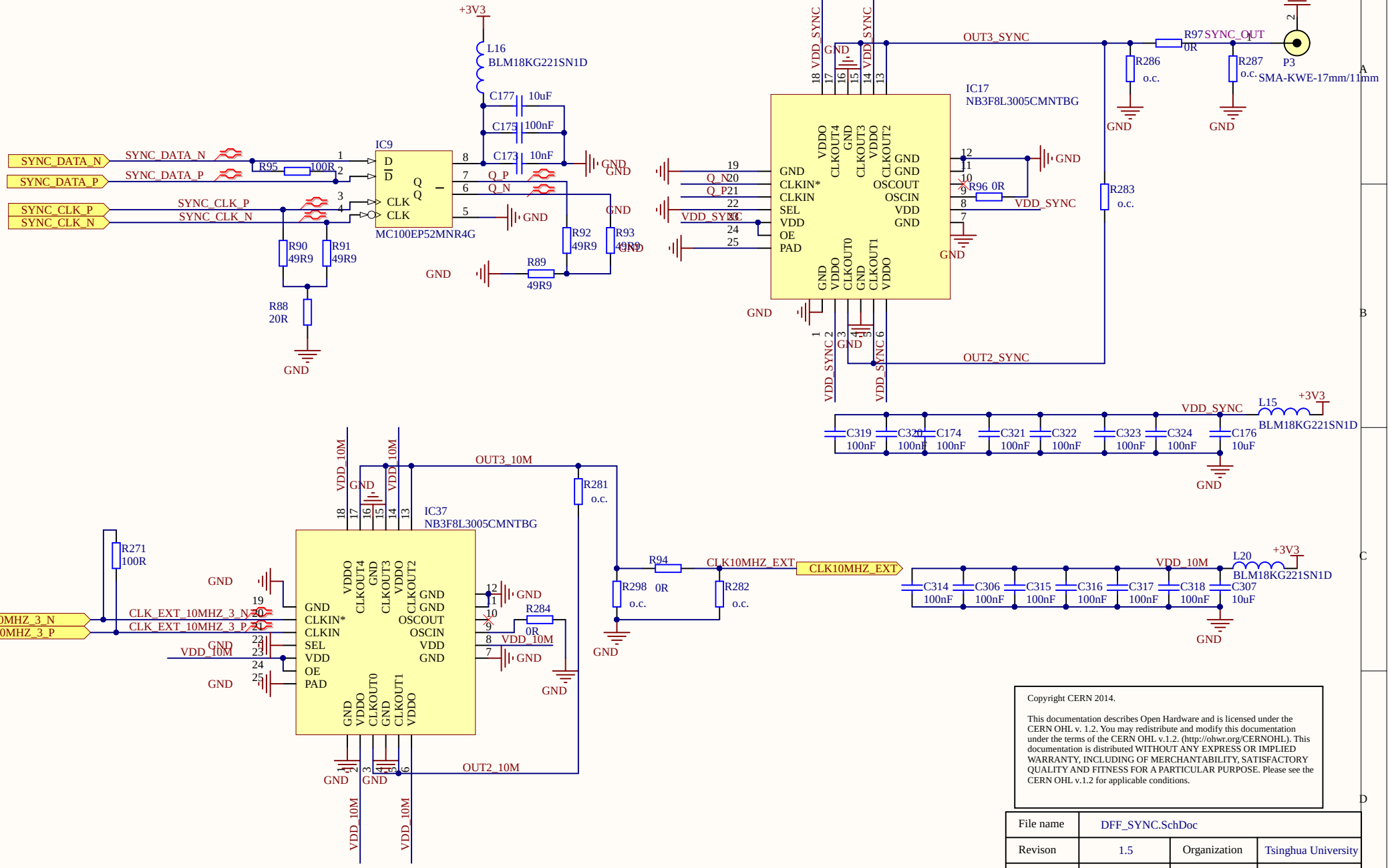
Cannot open file D:\Users\baotw\Pictures\tps53126.PNG

File name	DCDC_ALL.SchDoc		
Revison	1.5	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2023/12/9

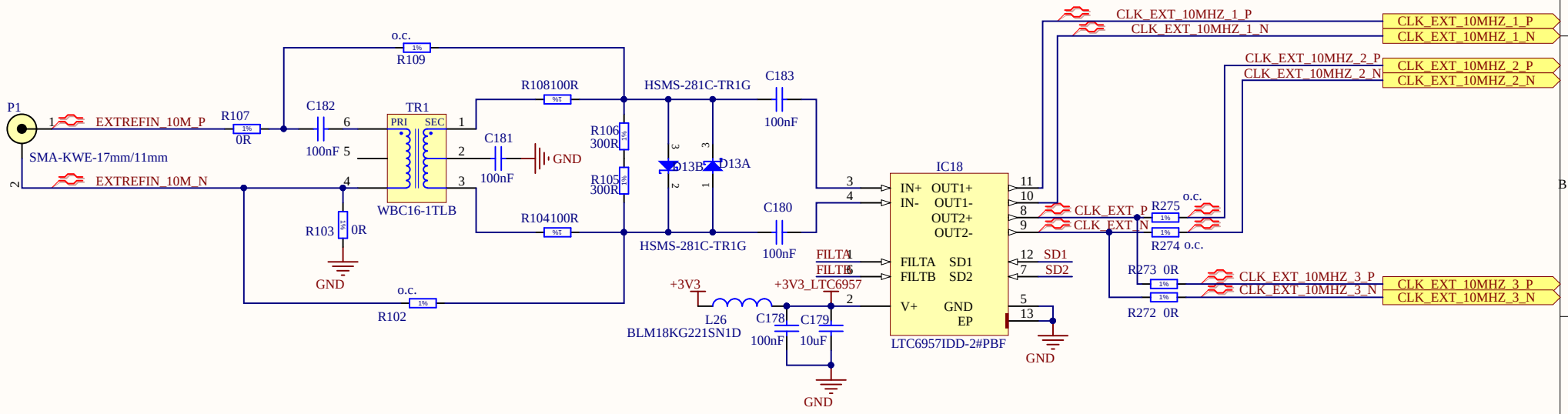




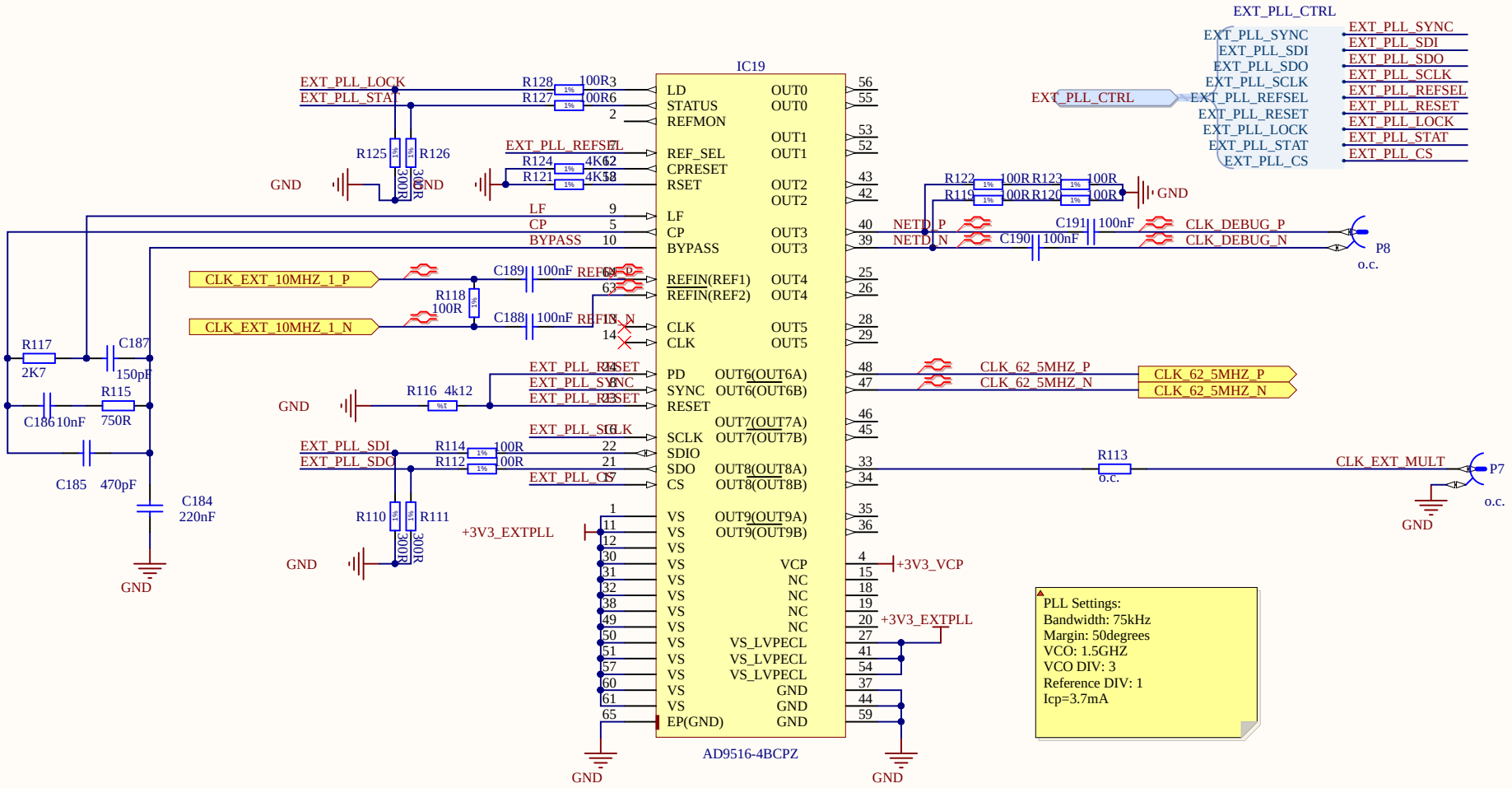
File name	DCDC.SchDoc		
Revison	1.5	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2023/12/9



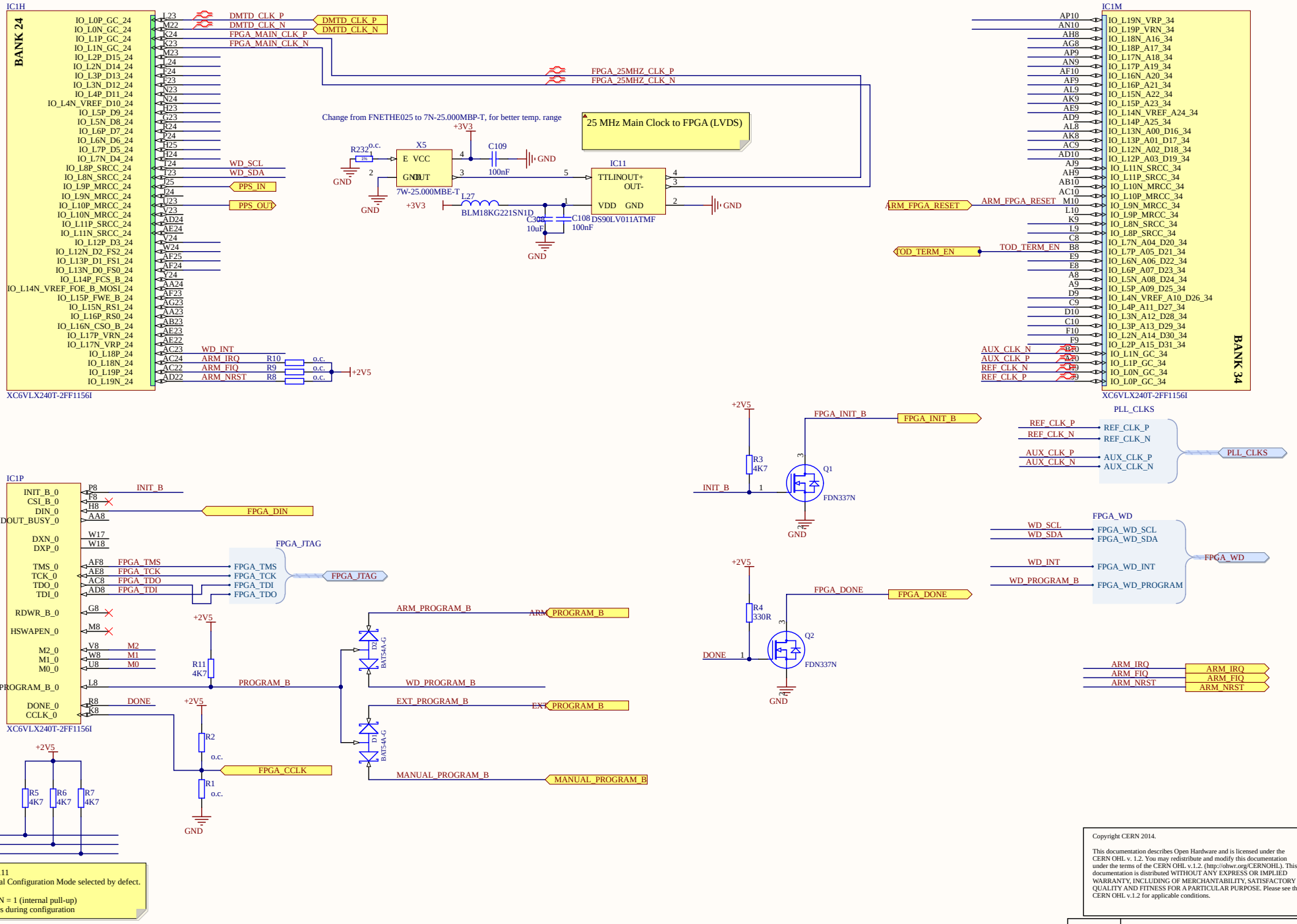
File name	DFF_SYNC.SchDoc		
Revison	1.5	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2023/12/9



File name	EXT_10M_IN.SchDoc		
Revison	1.5	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2023/12/9



File name	EXT_PLL.SchDoc		
Revison	1.5	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2023/12/9


IC1H
BANK 24
XC6VLX240T-2FF1156I
DMTD_CLK_P
DMTD_CLK_N
FPGA_MAIN_CLK_P
FPGA_MAIN_CLK_N
FPGA_25MHZ_CLK_P
FPGA_25MHZ_CLK_N
WD_SCL
WD_SDA
PPS_IN
PPS_OUT
WD_INT
ARM_IRQ
ARM_FIQ
ARM_NRST
+2V5
Change from FNETHE025 to 7N-25.000MBP-T, for better temp. range
25 MHz Main Clock to FPGA (LVDS)
+3V3
R232
X5
7W-25.000MBE-T
C109
100nF
IC11
DS90LV011ATMF
L27
BLM18KG221SN1D
C30
10uF
C108
100nF
GND
IC1M
BANK 34
XC6VLX240T-2FF1156I
ARM_FPGA_RESET
TOD_TERM_EN
AUX_CLK_N
AUX_CLK_P
REF_CLK_N
REF_CLK_P
IC1P
INIT_B
FPGA_DIN
FPGA_JTAG
FPGA_TMS
FPGA_TCK
FPGA_TDI
FPGA_TDO
PROGRAM_B
DONE
FPGA_CCLK
ARM_PROGRAM_B
WD_PROGRAM_B
EXT_PROGRAM_B
MANUAL_PROGRAM_B
D2
D1
BAT54A-G
R11
4K7
R2
R1
o.c.
R5
R6
R7
4K7
M2
M1
M0
M[2:0] = 111
Slave Serial Configuration Mode selected by defect.
HSWAPEN = 1 (internal pull-up)
3-state I/Os during configuration
FPGA_INIT_B
R3
4K7
Q1
FDN337N
PLL_CLKS
FPGA_WD
FPGA_WD_SCL
FPGA_WD_SDA
FPGA_WD_INT
FPGA_WD_PROGRAM
FPGA_DONE
R4
330R
Q2
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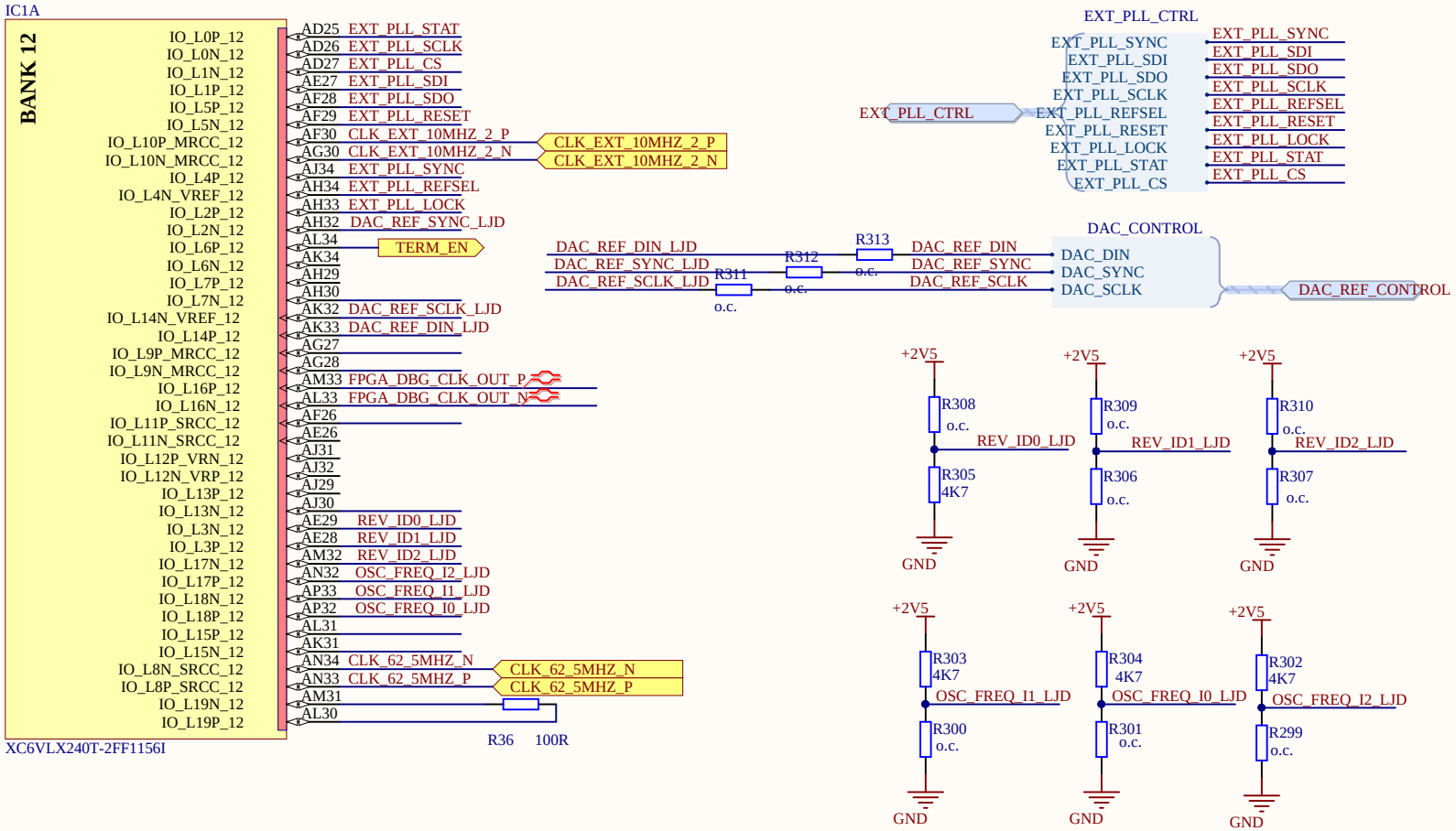
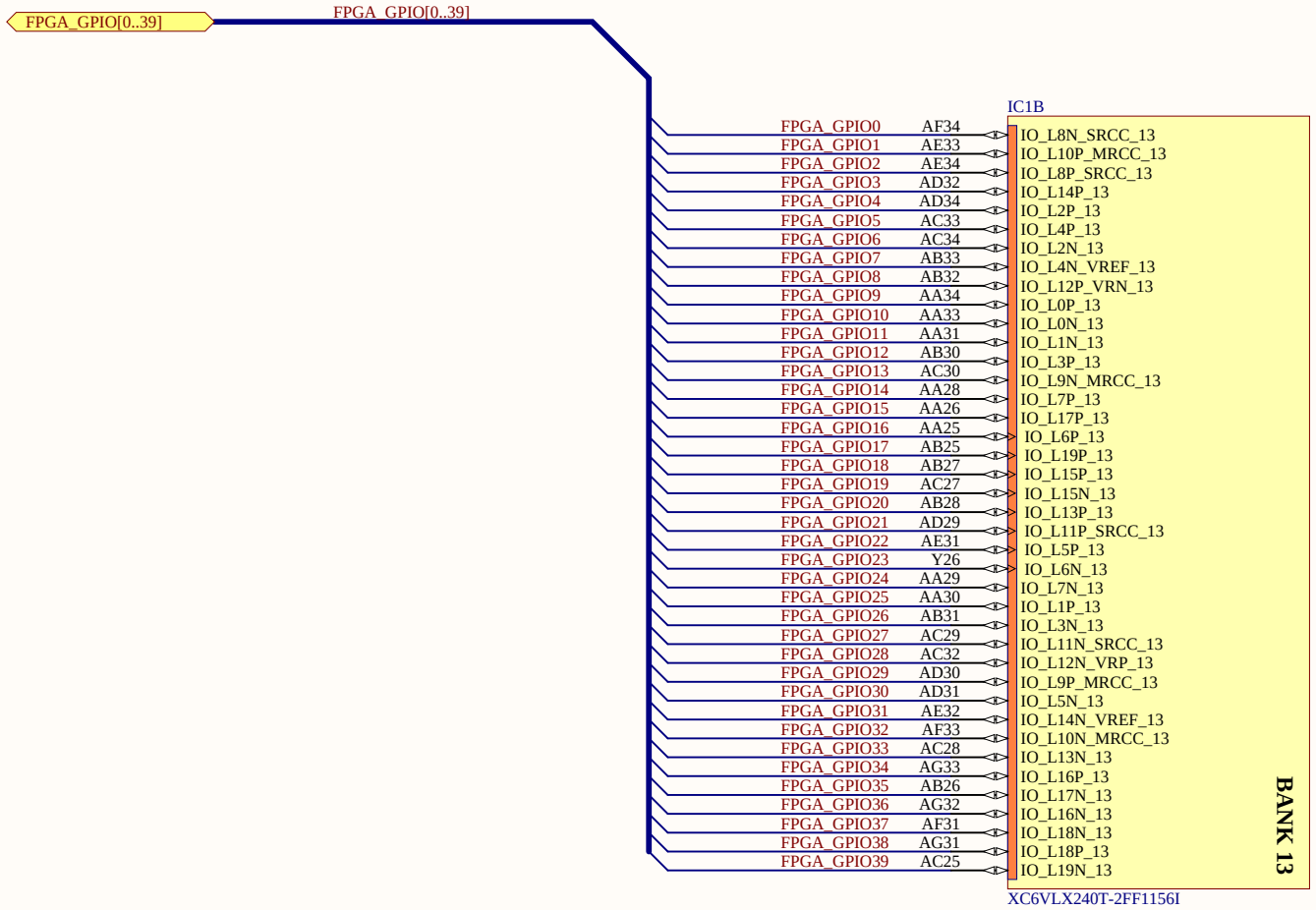
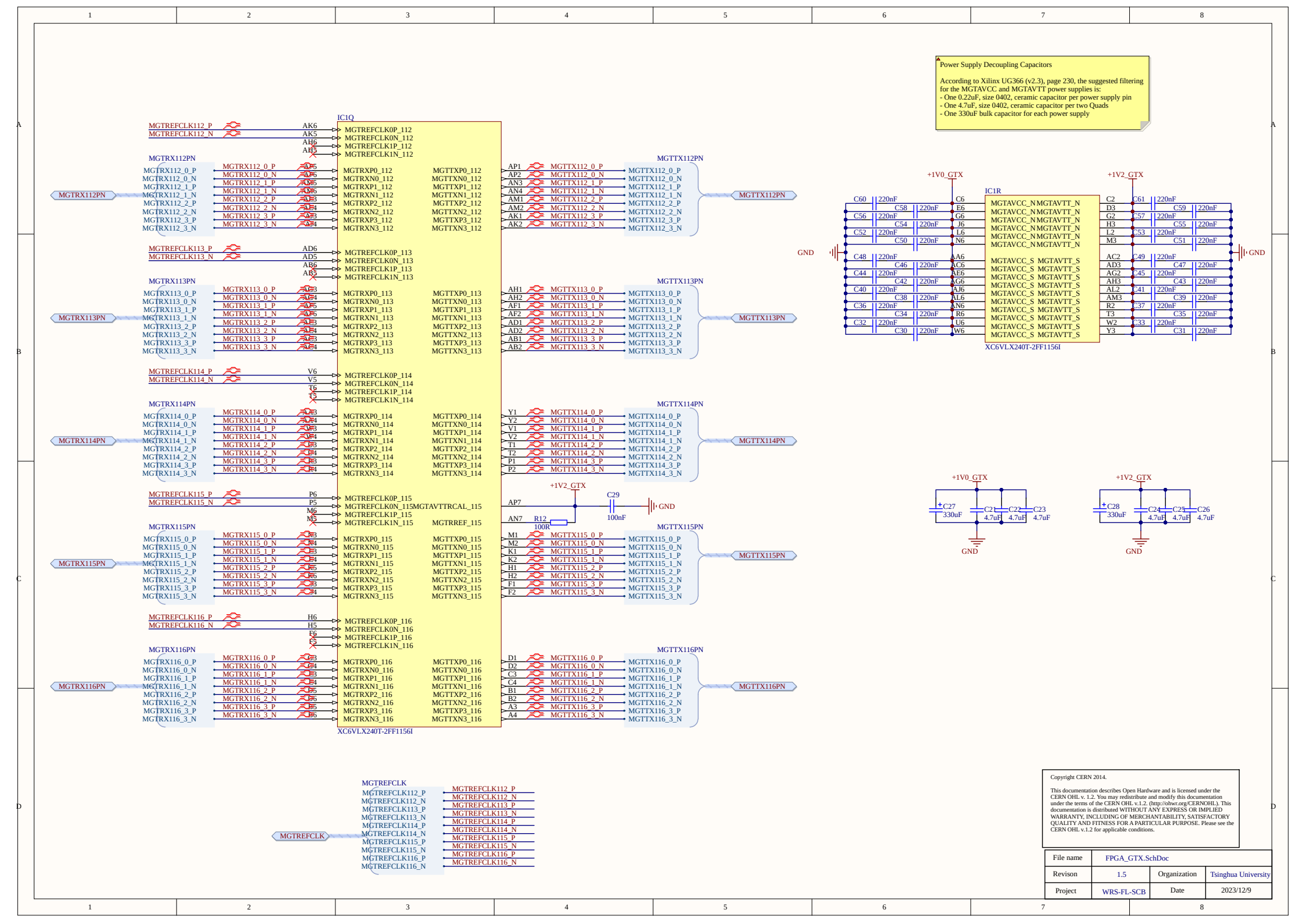
File name
FPGA_Configuration.SchDoc
Revison
1.5
Organization
Tsinghua University
Project
WRS-FL-SCB
Date
2023/12/9



File name	FPGA_EXT_PLL.SchDoc		
Revison	1.5	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2023/12/9



File name	FPGA_GPIOs.SchDoc		
Revison	1.5	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2023/12/9


IC1Q
XC6VLX240T-2FF1156I
MGTREFCLK112_P
MGTREFCLK112_N
MGTREFCLK113_P
MGTREFCLK113_N
MGTREFCLK114_P
MGTREFCLK114_N
MGTREFCLK115_P
MGTREFCLK115_N
MGTREFCLK116_P
MGTREFCLK116_N
MGTREFCLK0P_112
MGTREFCLK0N_112
MGTREFCLK1P_112
MGTREFCLK1N_112
MGTREFCLK0P_113
MGTREFCLK0N_113
MGTREFCLK1P_113
MGTREFCLK1N_113
MGTREFCLK0P_114
MGTREFCLK0N_114
MGTREFCLK1P_114
MGTREFCLK1N_114
MGTREFCLK0P_115
MGTREFCLK0N_115
MGTAVTTRCAL_115
MGTREFCLK1P_115
MGTREFCLK1N_115
MGTRREF_115
MGTREFCLK0P_116
MGTREFCLK0N_116
MGTREFCLK1P_116
MGTREFCLK1N_116
MGTRX112PN
MGTRX113PN
MGTRX114PN
MGTRX115PN
MGTRX116PN
MGTTX112PN
MGTTX113PN
MGTTX114PN
MGTTX115PN
MGTTX116PN
+1V2_GTX
C29
100nF
GND
R12
100R
AN7
AP7
IC1R
XC6VLX240T-2FF1156I
+1V0_GTX
+1V2_GTX
MGTAVCC_N
MGTAVTT_N
MGTAVCC_S
MGTAVTT_S
C27
330uF
C28
330uF
4.7uF
220nF
GND
Power Supply Decoupling Capacitors
According to Xilinx UG366 (v2.3), page 230, the suggested filtering for the MGTAVCC and MGTAVTT power supplies is:
- One 0.22uF, size 0402, ceramic capacitor per power supply pin
- One 4.7uF, size 0402, ceramic capacitor per two Quads
- One 330uF bulk capacitor for each power supply
MGTREFCLK
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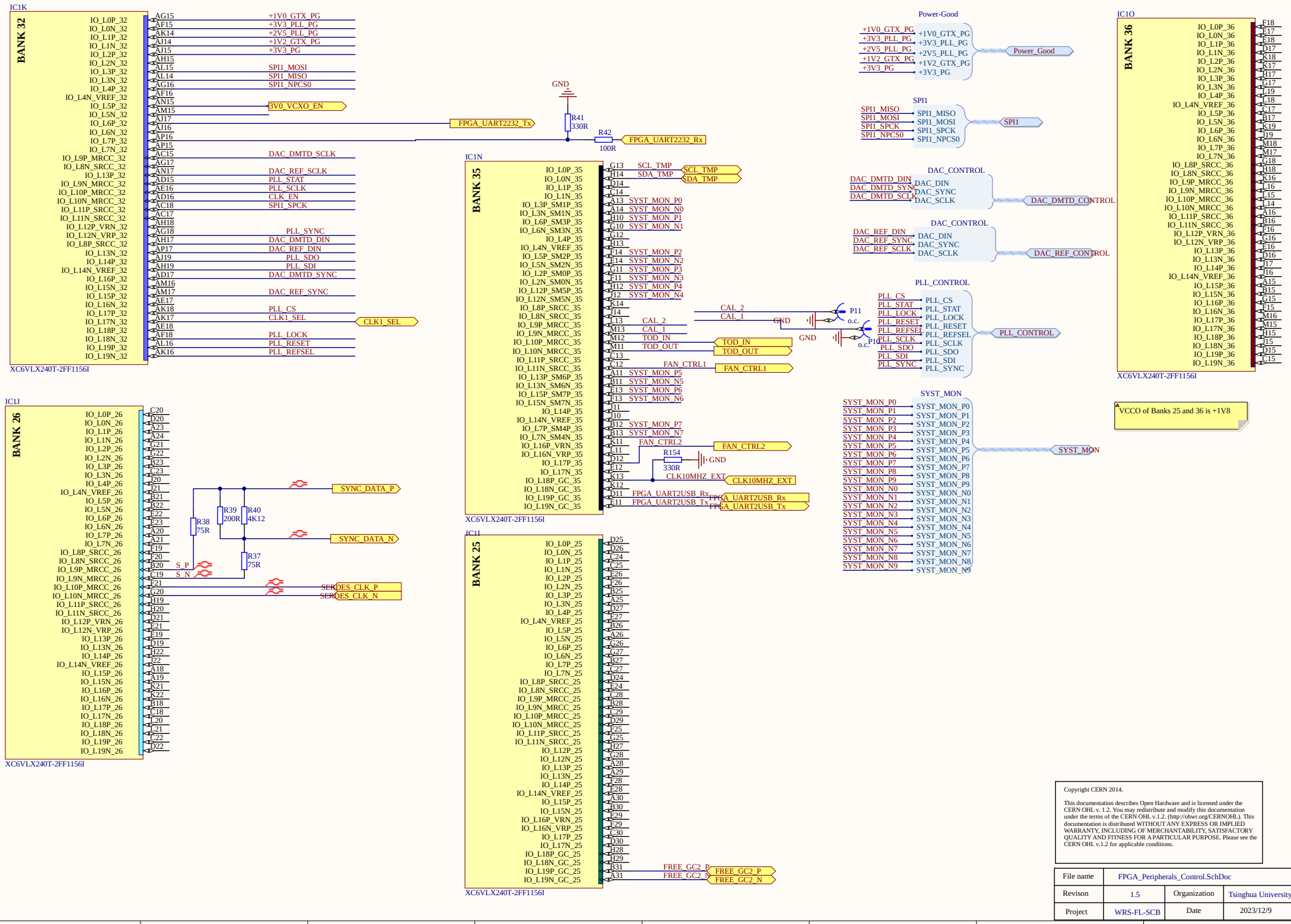
File name
FPGA_GTX.SchDoc
Revison
1.5
Organization
Tsinghua University
Project
WRS-FL-SCB
Date
2023/12/9


IC1K
BANK 32
IO_L0P_32
IO_L0N_32
IO_L1P_32
IO_L1N_32
IO_L2P_32
IO_L2N_32
IO_L3P_32
IO_L3N_32
IO_L4P_32
IO_L4N_VREF_32
IO_L5P_32
IO_L5N_32
IO_L6P_32
IO_L6N_32
IO_L7P_32
IO_L7N_32
IO_L9P_MRCC_32
IO_L8N_SRCC_32
IO_L13P_32
IO_L9N_MRCC_32
IO_L10P_MRCC_32
IO_L10N_MRCC_32
IO_L11P_SRCC_32
IO_L11N_SRCC_32
IO_L12P_VRN_32
IO_L12N_VRP_32
IO_L8P_SRCC_32
IO_L13N_32
IO_L14P_32
IO_L14N_VREF_32
IO_L16P_32
IO_L15N_32
IO_L15P_32
IO_L16N_32
IO_L17P_32
IO_L17N_32
IO_L18P_32
IO_L18N_32
IO_L19P_32
IO_L19N_32
AG15
AF15
AK14
AJ14
AJ15
AH15
AL15
AL14
AG16
AF16
AN15
AM15
AJ17
AJ16
AP16
AP15
AC15
AG17
AN17
AD15
AE16
AD16
AC18
AC17
AH18
AG18
AH17
AP17
AJ19
AH19
AD17
AM16
AM17
AE17
AK18
AK17
AE18
AF18
AL16
AK16
+1V0_GTX_PG
+3V3_PLL_PG
+2V5_PLL_PG
+1V2_GTX_PG
+3V3_PG
SPI1_MOSI
SPI1_MISO
SPI1_NPCS0
3V0_VCXO_EN
FPGA_UART2232_Tx
FPGA_UART2232_Rx
DAC_DMTD_SCLK
DAC_REF_SCLK
PLL_STAT
PLL_SCLK
CLK_EN
SPI1_SPCK
PLL_SYNC
DAC_DMTD_DIN
DAC_REF_DIN
PLL_SDO
PLL_SDI
DAC_DMTD_SYNC
DAC_REF_SYNC
PLL_CS
CLK1_SEL
PLL_LOCK
PLL_RESET
PLL_REFSEL
XC6VLX240T-2FF1156I
GND
R41
330R
R42
100R
IC1N
BANK 35
IO_L0P_35
IO_L0N_35
IO_L1P_35
IO_L1N_35
IO_L3P_SM1P_35
IO_L3N_SM1N_35
IO_L6P_SM3P_35
IO_L6N_SM3N_35
IO_L4P_35
IO_L4N_VREF_35
IO_L5P_SM2P_35
IO_L5N_SM2N_35
IO_L2P_SM0P_35
IO_L2N_SM0N_35
IO_L12P_SM5P_35
IO_L12N_SM5N_35
IO_L8P_SRCC_35
IO_L8N_SRCC_35
IO_L9P_MRCC_35
IO_L9N_MRCC_35
IO_L10P_MRCC_35
IO_L10N_MRCC_35
IO_L11P_SRCC_35
IO_L11N_SRCC_35
IO_L13P_SM6P_35
IO_L13N_SM6N_35
IO_L15P_SM7P_35
IO_L15N_SM7N_35
IO_L14P_35
IO_L14N_VREF_35
IO_L7P_SM4P_35
IO_L7N_SM4N_35
IO_L16P_VRN_35
IO_L16N_VRP_35
IO_L17P_35
IO_L17N_35
IO_L18P_GC_35
IO_L18N_GC_35
IO_L19P_GC_35
IO_L19N_GC_35
G13
H14
D14
C14
A13
A14
H10
G10
G12
H13
F14
E14
G11
F11
H12
J12
K14
J14
L13
M13
M12
M11
C13
C12
A11
B11
E13
F13
J11
J10
B12
B13
K11
L11
D12
F12
K13
K12
D11
E11
SCL_TMP
SDA_TMP
SYST_MON_P0
SYST_MON_N0
SYST_MON_P1
SYST_MON_N1
SYST_MON_P2
SYST_MON_N2
SYST_MON_P3
SYST_MON_N3
SYST_MON_P4
SYST_MON_N4
CAL_2
CAL_1
TOD_IN
TOD_OUT
FAN_CTRL1
SYST_MON_P5
SYST_MON_N5
SYST_MON_P6
SYST_MON_N6
SYST_MON_P7
SYST_MON_N7
FAN_CTRL2
CLK10MHZ_EXT
FPGA_UART2USB_Rx
FPGA_UART2USB_Tx
P11
P10
o.c.
R154
330R
IC1J
BANK 26
IO_L0P_26
IO_L0N_26
IO_L1P_26
IO_L1N_26
IO_L2P_26
IO_L2N_26
IO_L3P_26
IO_L3N_26
IO_L4P_26
IO_L4N_VREF_26
IO_L5P_26
IO_L5N_26
IO_L6P_26
IO_L6N_26
IO_L7P_26
IO_L7N_26
IO_L8P_SRCC_26
IO_L8N_SRCC_26
IO_L9P_MRCC_26
IO_L9N_MRCC_26
IO_L10P_MRCC_26
IO_L10N_MRCC_26
IO_L11P_SRCC_26
IO_L11N_SRCC_26
IO_L12P_VRN_26
IO_L12N_VRP_26
IO_L13P_26
IO_L13N_26
IO_L14P_26
IO_L14N_VREF_26
IO_L15P_26
IO_L15N_26
IO_L16P_26
IO_L16N_26
IO_L17P_26
IO_L17N_26
IO_L18P_26
IO_L18N_26
IO_L19P_26
IO_L19N_26
C20
D20
A23
A24
G21
G22
B23
C23
C20
G21
B21
B22
E22
C23
A20
A21
F19
F20
B20
C19
F21
G20
H19
H20
D21
F21
E19
D19
H22
J22
A18
A19
K21
K22
B18
C18
E20
F21
E22
D22
S_P
S_N
R38
75R
R39
200R
R40
4K12
R37
75R
SYNC_DATA_P
SYNC_DATA_N
SERDES_CLK_P
SERDES_CLK_N
IC1I
BANK 25
IO_L0P_25
IO_L0N_25
IO_L1P_25
IO_L1N_25
IO_L2P_25
IO_L2N_25
IO_L3P_25
IO_L3N_25
IO_L4P_25
IO_L4N_VREF_25
IO_L5P_25
IO_L5N_25
IO_L6P_25
IO_L6N_25
IO_L7P_25
IO_L7N_25
IO_L8P_SRCC_25
IO_L8N_SRCC_25
IO_L9P_MRCC_25
IO_L9N_MRCC_25
IO_L10P_MRCC_25
IO_L10N_MRCC_25
IO_L11P_SRCC_25
IO_L11N_SRCC_25
IO_L12P_25
IO_L12N_25
IO_L13P_25
IO_L13N_25
IO_L14P_25
IO_L14N_VREF_25
IO_L15P_25
IO_L15N_25
IO_L16P_VRN_25
IO_L16N_VRP_25
IO_L17P_25
IO_L17N_25
IO_L18P_GC_25
IO_L18N_GC_25
IO_L19P_GC_25
IO_L19N_GC_25
D25
D26
C24
C25
E26
F26
B25
A25
D27
E27
B26
A26
G26
G27
B27
C27
D24
E24
C28
B28
C29
D29
E25
G25
H27
G28
A28
A29
E28
F28
A30
B30
E29
F29
C30
D30
H28
H29
B31
A31
FREE_GC2_P
FREE_GC2_N
Power-Good
+1V0_GTX_PG
+3V3_PLL_PG
+2V5_PLL_PG
+1V2_GTX_PG
+3V3_PG
Power_Good
SPI1
SPI1_MISO
SPI1_MOSI
SPI1_SPCK
SPI1_NPCS0
DAC_CONTROL
DAC_DMTD_DIN
DAC_DMTD_SYNC
DAC_DMTD_SCLK
DAC_DIN
DAC_SYNC
DAC_SCLK
DAC_DMTD_CONTROL
DAC_REF_DIN
DAC_REF_SYNC
DAC_REF_SCLK
DAC_REF_CONTROL
PLL_CONTROL
PLL_CS
PLL_STAT
PLL_LOCK
PLL_RESET
PLL_REFSEL
PLL_SCLK
PLL_SDO
PLL_SDI
PLL_SYNC
SYST_MON
SYST_MON_P0
SYST_MON_P1
SYST_MON_P2
SYST_MON_P3
SYST_MON_P4
SYST_MON_P5
SYST_MON_P6
SYST_MON_P7
SYST_MON_P8
SYST_MON_P9
SYST_MON_N0
SYST_MON_N1
SYST_MON_N2
SYST_MON_N3
SYST_MON_N4
SYST_MON_N5
SYST_MON_N6
SYST_MON_N7
SYST_MON_N8
SYST_MON_N9
IC1O
BANK 36
IO_L0P_36
IO_L0N_36
IO_L1P_36
IO_L1N_36
IO_L2P_36
IO_L2N_36
IO_L3P_36
IO_L3N_36
IO_L4P_36
IO_L4N_VREF_36
IO_L5P_36
IO_L5N_36
IO_L6P_36
IO_L6N_36
IO_L7P_36
IO_L7N_36
IO_L8P_SRCC_36
IO_L8N_SRCC_36
IO_L9P_MRCC_36
IO_L9N_MRCC_36
IO_L10P_MRCC_36
IO_L10N_MRCC_36
IO_L11P_SRCC_36
IO_L11N_SRCC_36
IO_L12P_VRN_36
IO_L12N_VRP_36
IO_L13P_36
IO_L13N_36
IO_L14P_36
IO_L14N_VREF_36
IO_L15P_36
IO_L15N_36
IO_L16P_36
IO_L16N_36
IO_L17P_36
IO_L17N_36
IO_L18P_36
IO_L18N_36
IO_L19P_36
IO_L19N_36
F18
E17
E18
D17
K18
K17
H17
G17
L19
L18
C17
B17
K19
J19
M18
M17
G18
H18
K16
L16
L15
L14
A16
B16
F16
G16
E16
D16
J17
J16
A15
B15
E15
F15
M16
M15
E15
L15
E15
L15
VCCO of Banks 25 and 36 is +1V8
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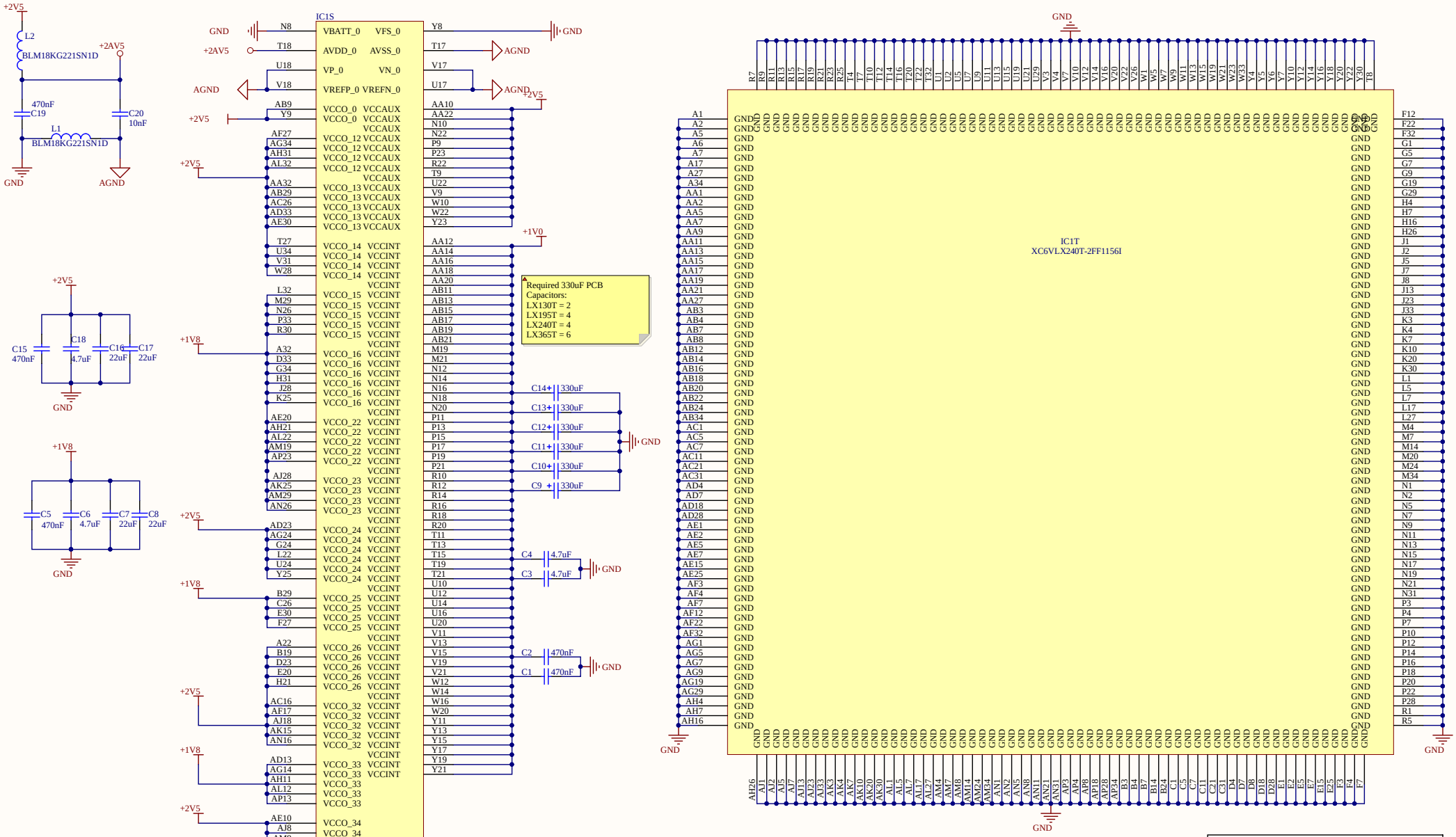
File name
FPGA_Peripherals_Control.SchDoc
Revison
1.5
Organization
Tsinghua University
Project
WRS-FL-SCB
Date
2023/12/9


+2V5
L2
BLM18KG221SN1D
+2AV5
470nF
C19
C20
10nF
L1
BLM18KG221SN1D
GND
AGND
IC1S
VBATT_0
VFS_0
AVDD_0
AVSS_0
VP_0
VN_0
VREFP_0
VREFN_0
VCCO_0 VCCAUX
VCCO_12 VCCAUX
VCCO_13 VCCAUX
VCCO_14 VCCINT
VCCO_15 VCCINT
VCCO_16 VCCINT
VCCO_22 VCCINT
VCCO_23 VCCINT
VCCO_24 VCCINT
VCCO_25 VCCINT
VCCO_26 VCCINT
VCCO_32 VCCINT
VCCO_33 VCCINT
VCCO_34
VCCO_35 VCCO_36
XC6VLX240T-2FF1156I
+1V8
+1V0
C15
470nF
C18
4.7uF
C16
22uF
C17
22uF
C5
470nF
C6
4.7uF
C7
22uF
C8
22uF
C14
330uF
C13
330uF
C12
330uF
C11
330uF
C10
330uF
C9
330uF
C4
4.7uF
C3
4.7uF
C2
470nF
C1
470nF
Required 330uF PCB
Capacitors:
LX130T = 2
LX195T = 4
LX240T = 4
LX365T = 6
IC1T
XC6VLX240T-2FF1156I
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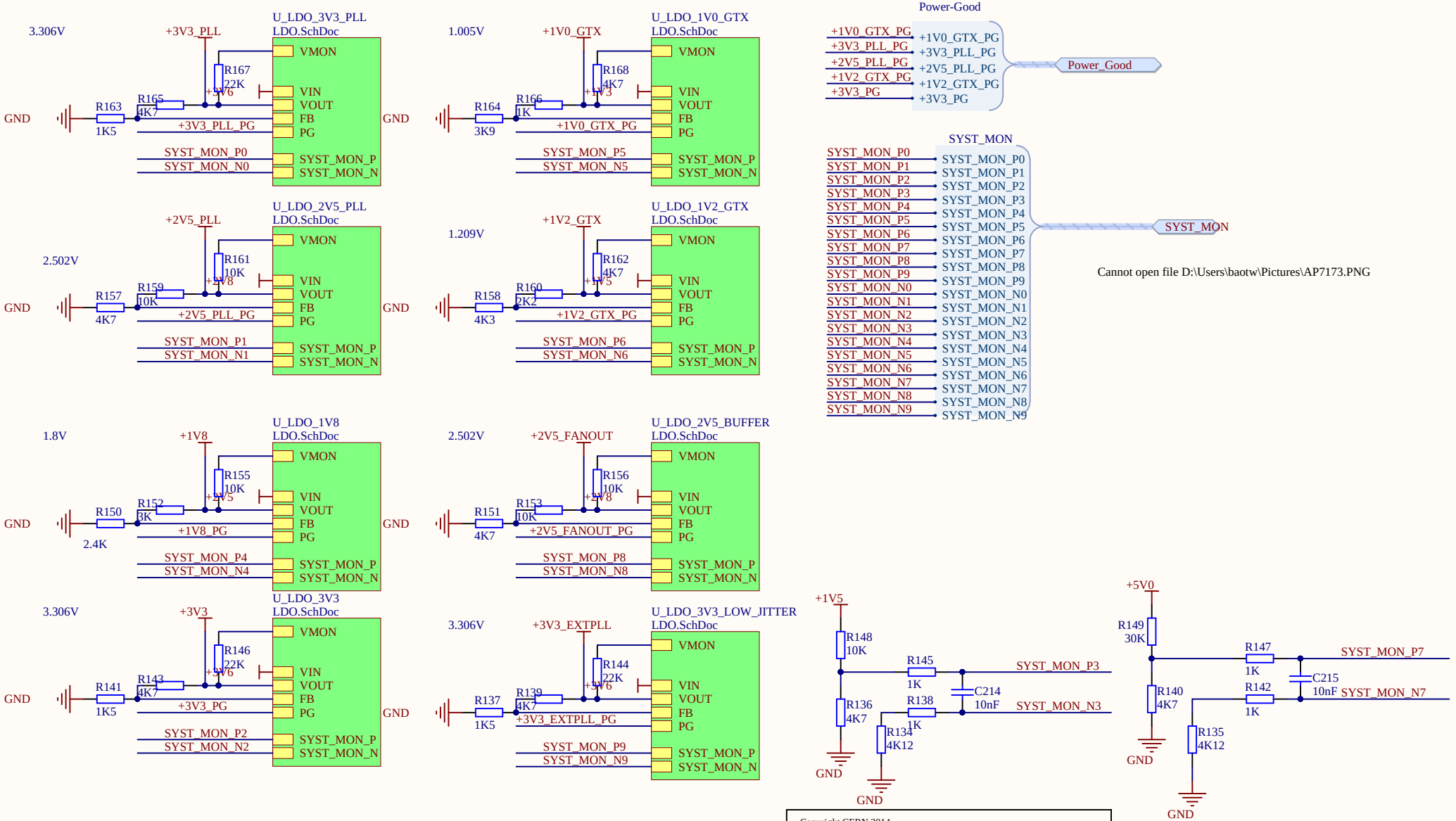
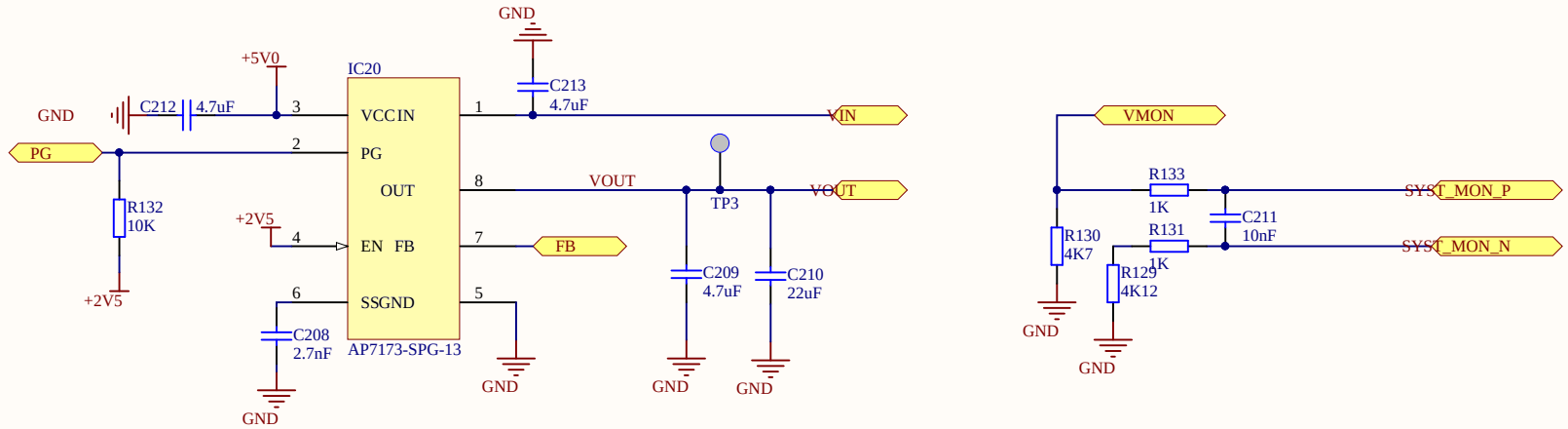
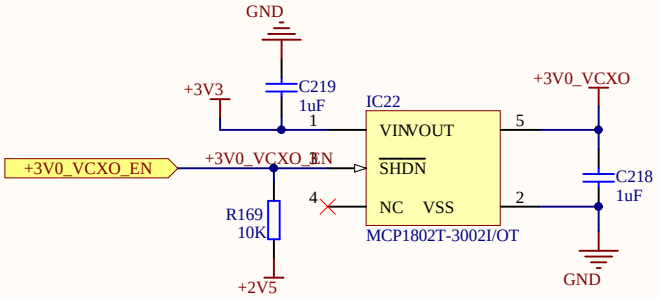
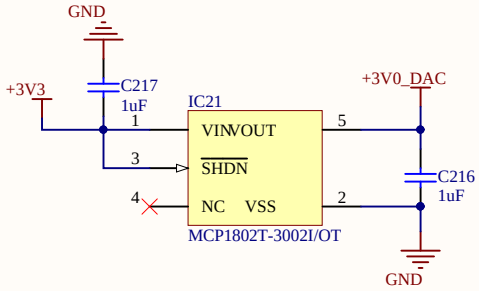
File name
FPGA_POWER_DGND.SchDoc
Revison
1.5
Organization
Tsinghua University
Project
WRS-FL-SCB
Date
2023/12/9

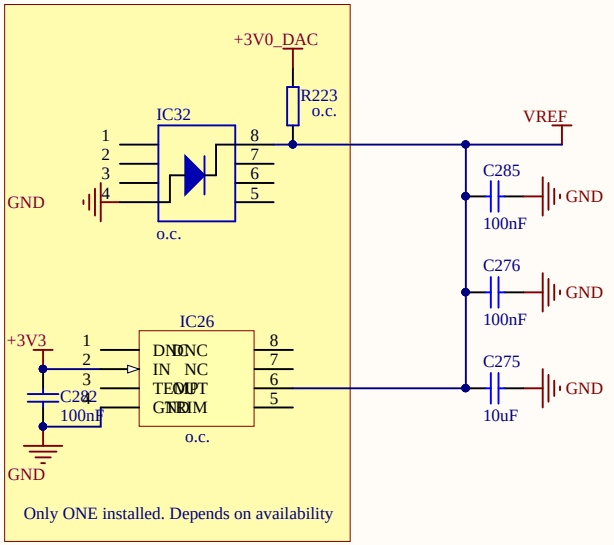


File name	LDO_ALL.SchDoc		
Revison	1.5	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2023/12/9

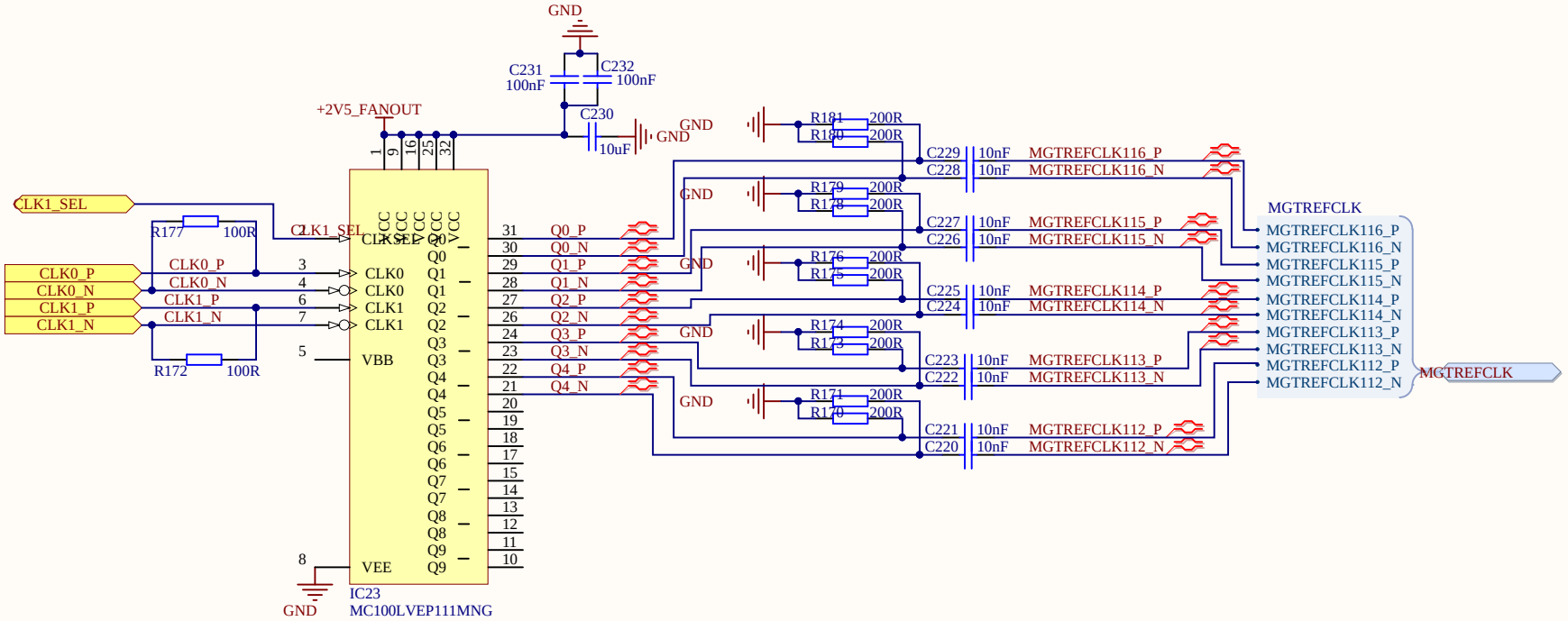

GND
+5V0
IC20
C213
4.7uF
GND
C212
4.7uF
3
VCC IN
1
VIN
PG
2
PG
OUT
8
VOUT
VOUT
TP3
R132
10K
+2V5
4
EN FB
7
FB
C209
4.7uF
C210
22uF
6
SSGND
5
C208
2.7nF
AP7173-SPG-13
GND
GND
GND
GND
VMON
R133
1K
SYST_MON_P
C211
10nF
R130
4K7
R131
1K
SYST_MON_N
R129
4K12
GND
GND



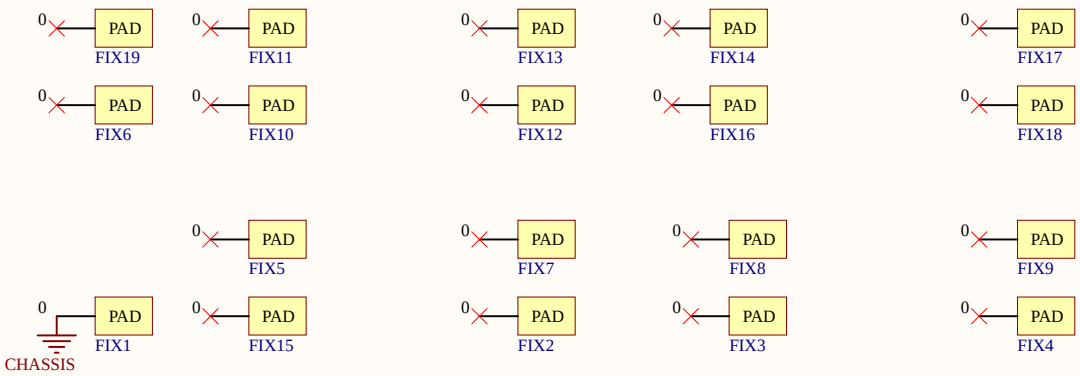




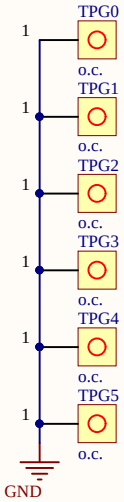
File name	LDO_XO.SchDoc		
Revison	1.5	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2023/12/9



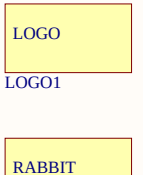
File name	LVPECL_FANOUT.SchDoc		
Revison	1.5	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2023/12/9



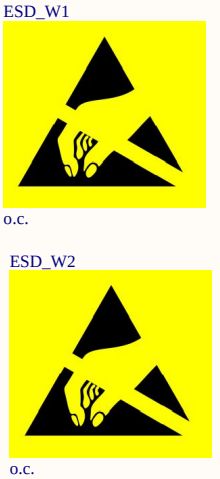
FFIX holes



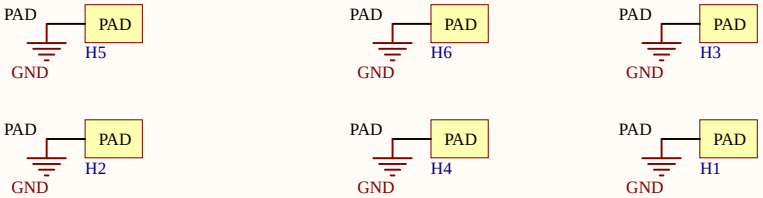
GND test point



Logo

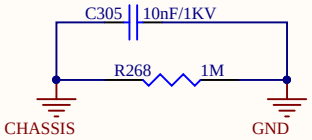


ESD warning drawing

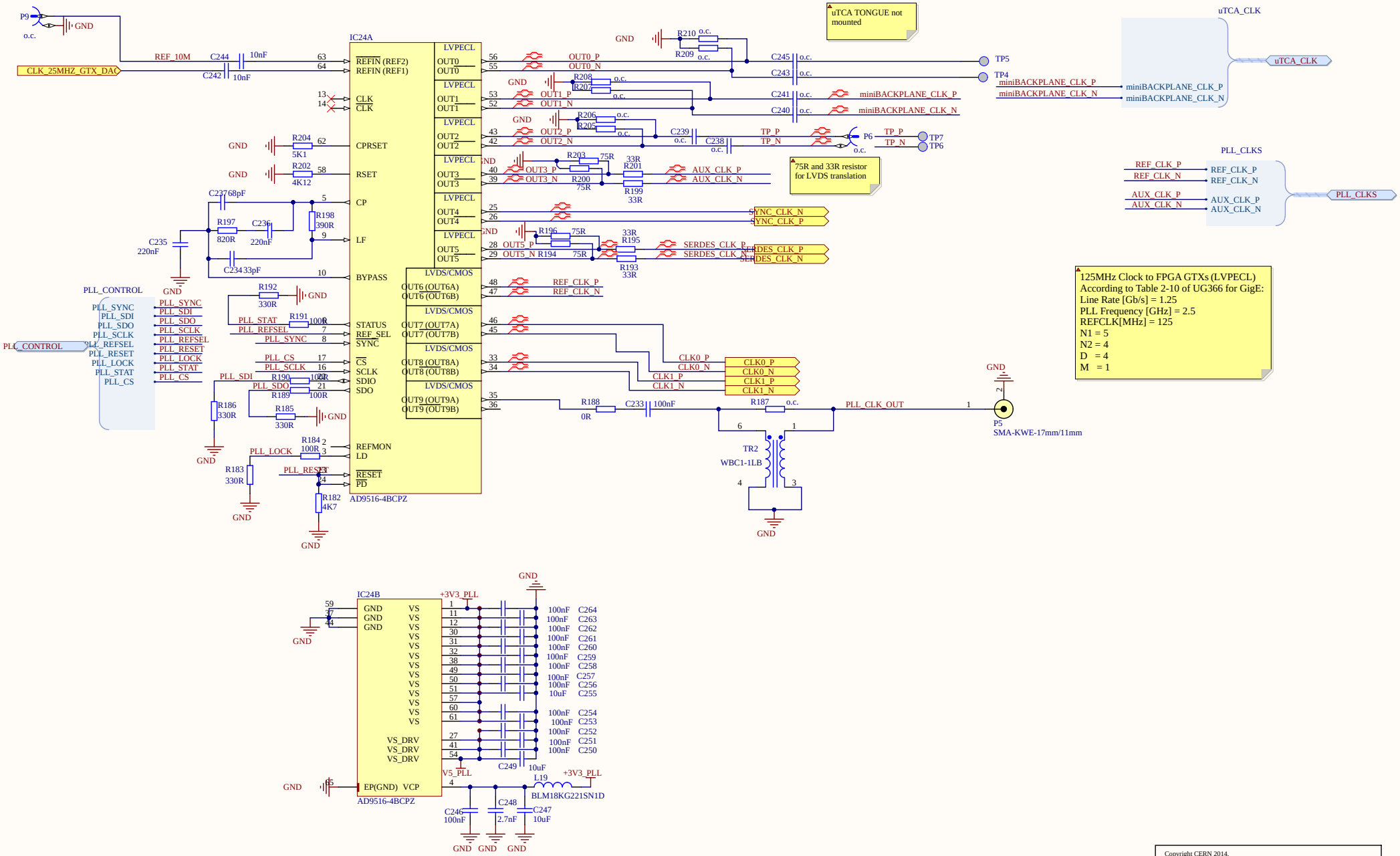


Thermal PAD for the PCB

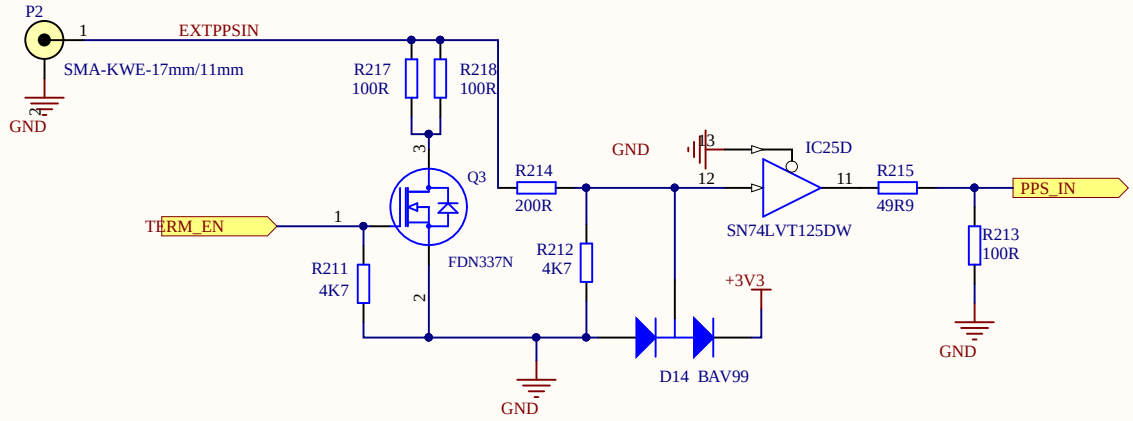
Scare Fiducial Target,

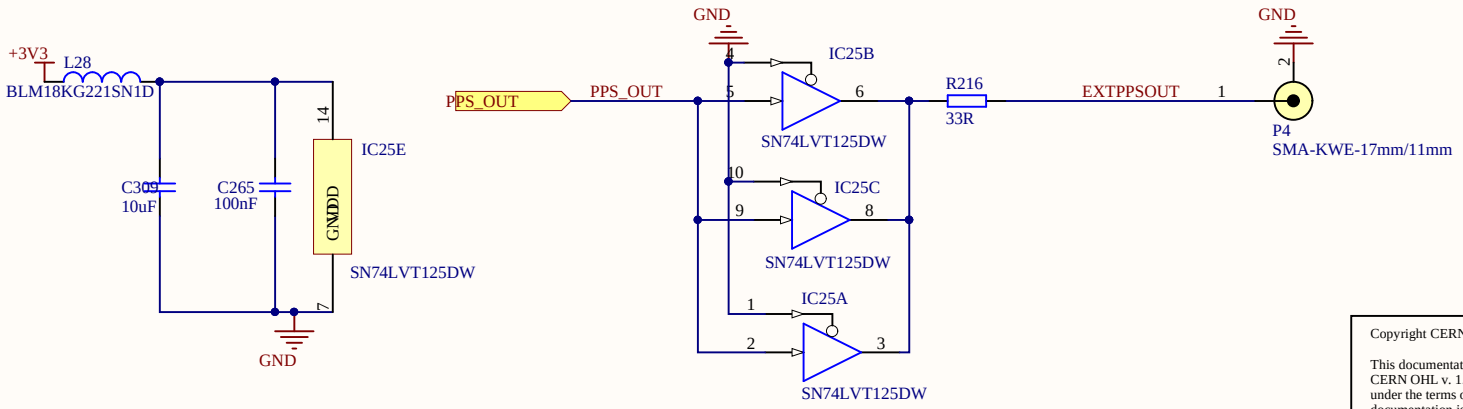


File name	NPTH_MARK_LOGO.SchDoc		
Revison	1.5	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2023/12/9

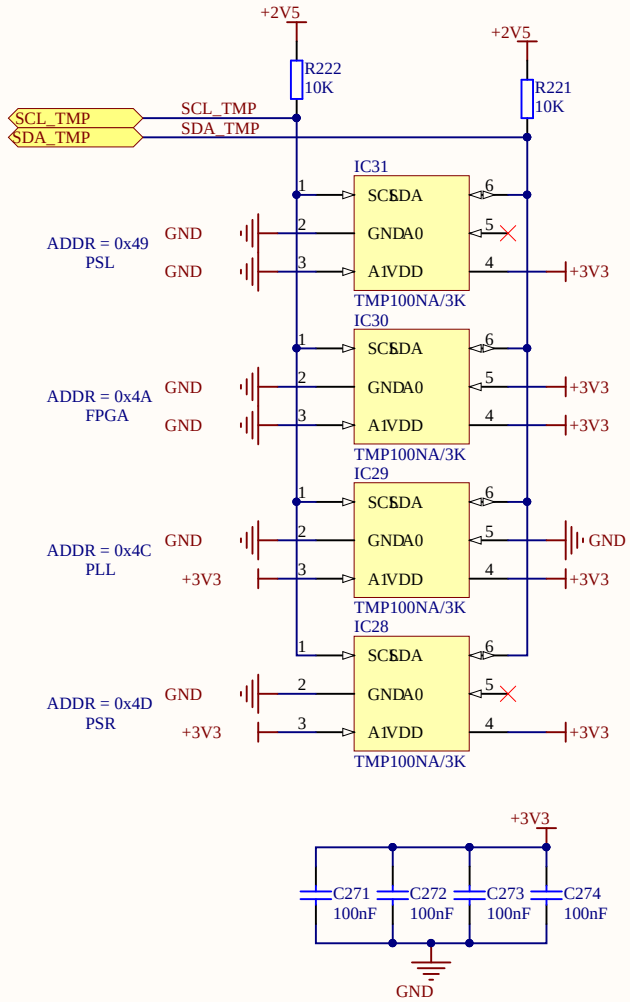


File name	PLL.SchDoc		
Revison	1.5	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2023/12/9

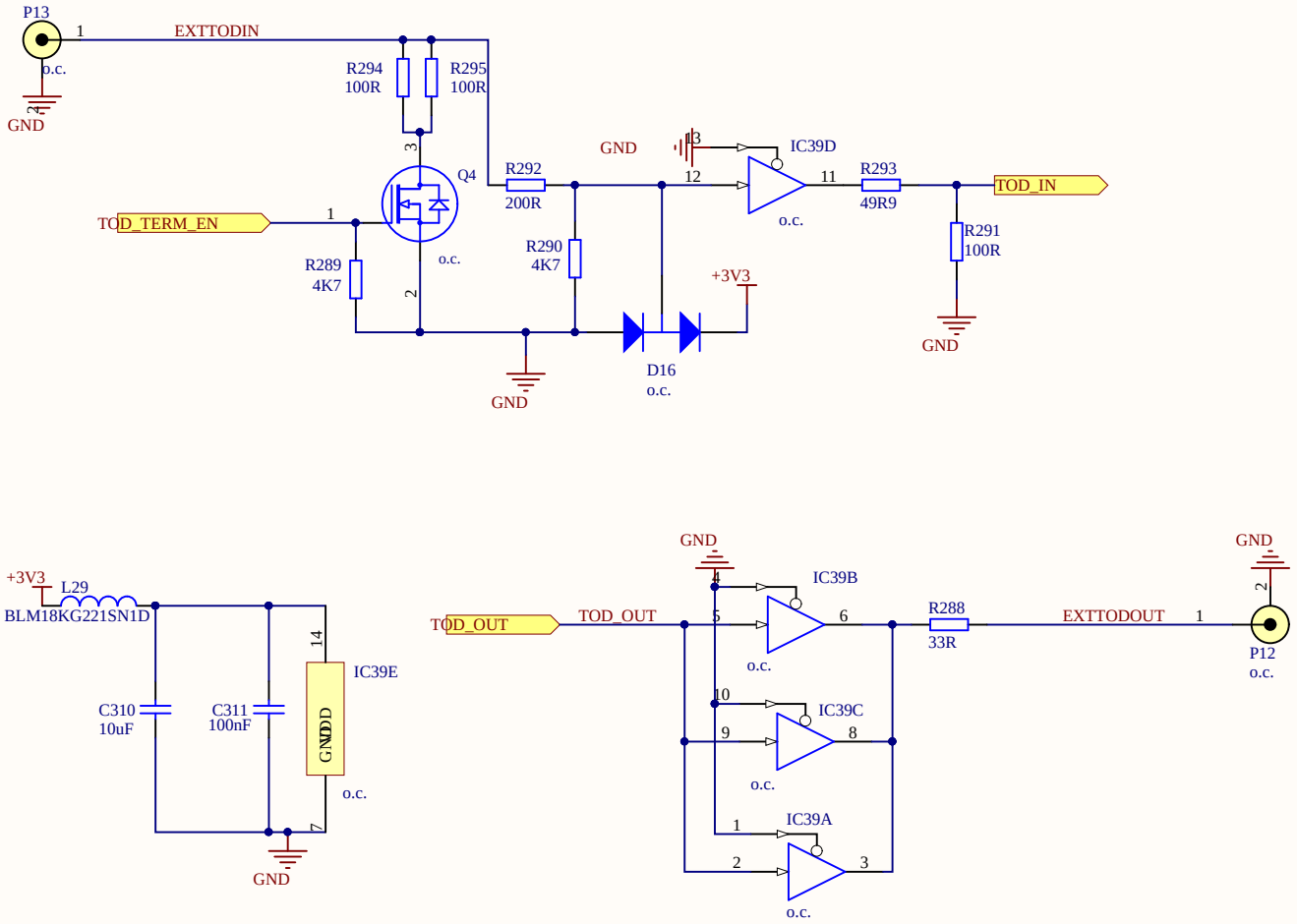




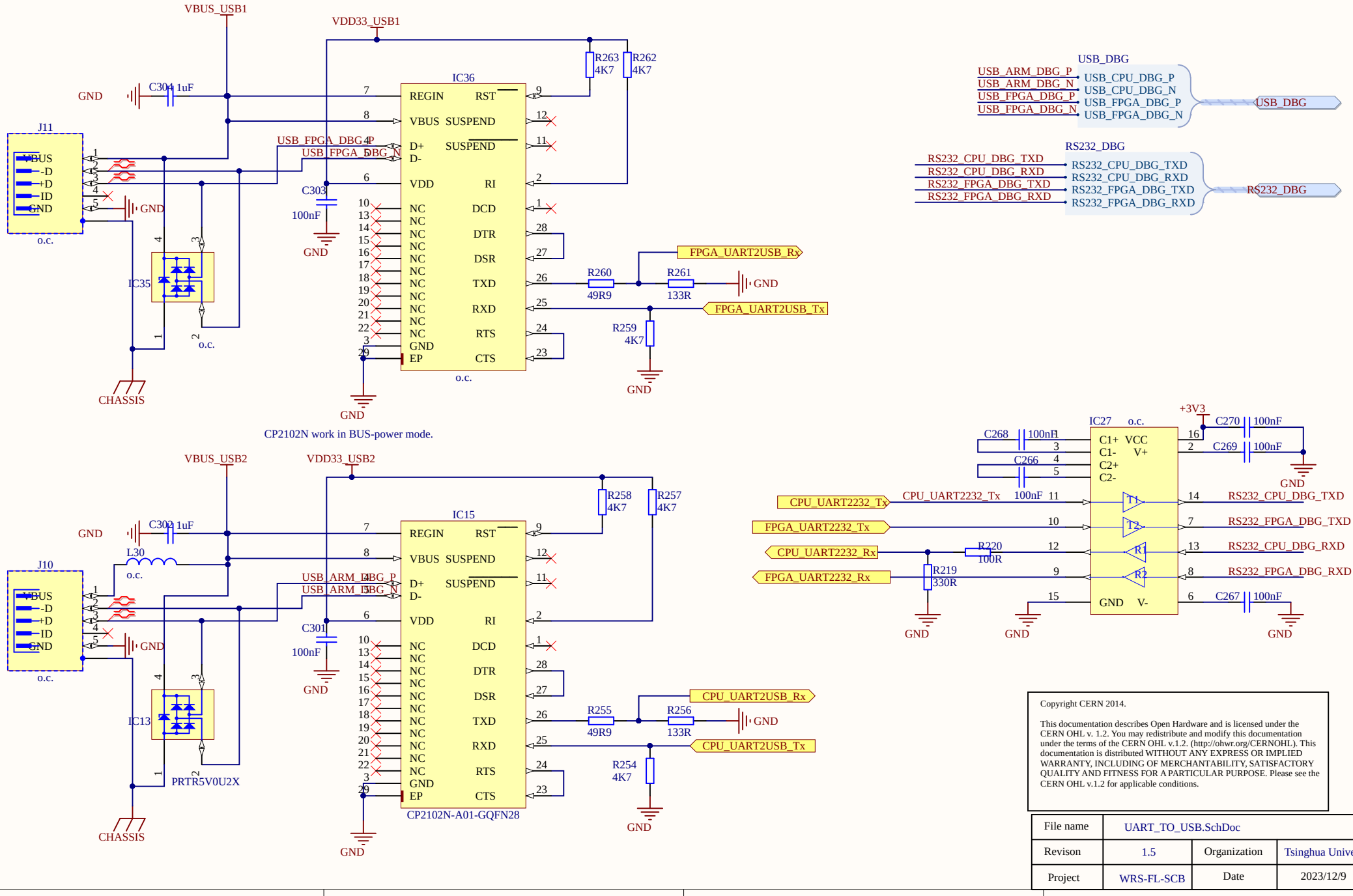
File name	PPS.SchDoc		
Revison	1.5	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2023/12/9



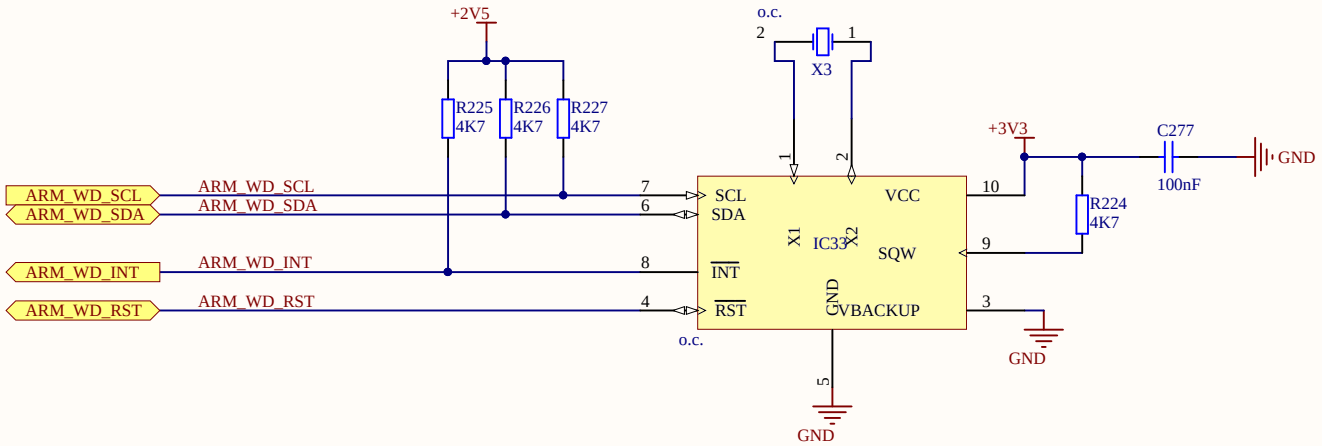
File name	SENSOR.SchDoc		
Revison	1.5	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2023/12/9



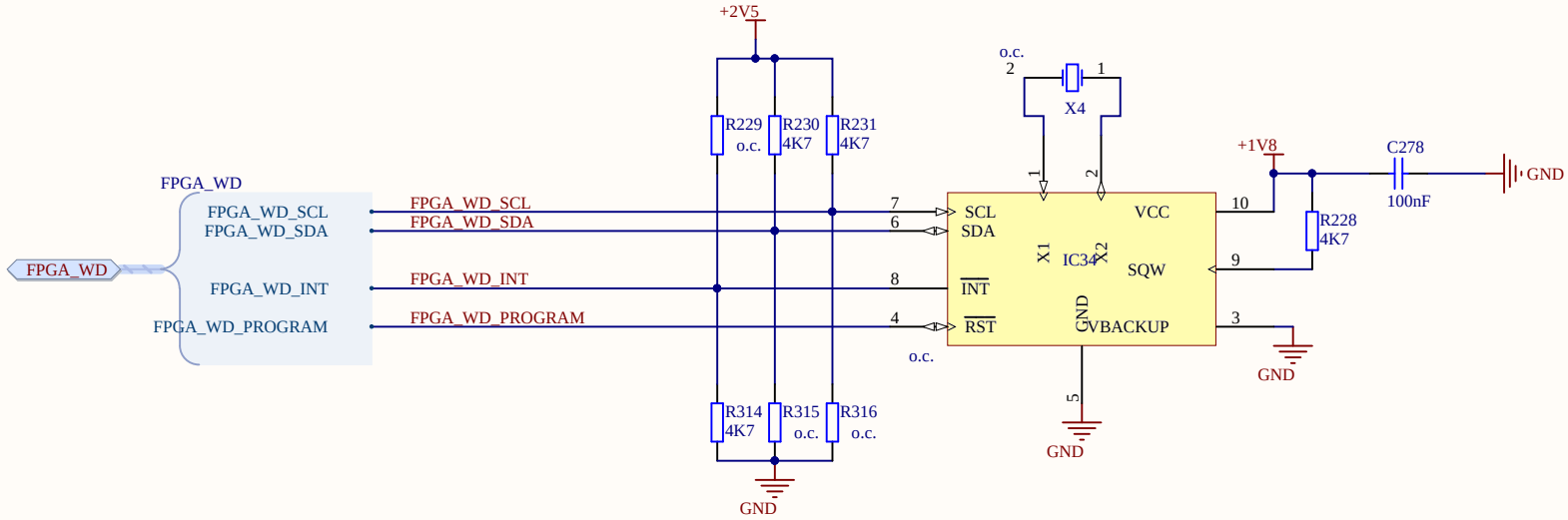
File name	TOD.SchDoc		
Revison	1.5	Organization	*
Project	White Rabbit	Date	2023/12/9



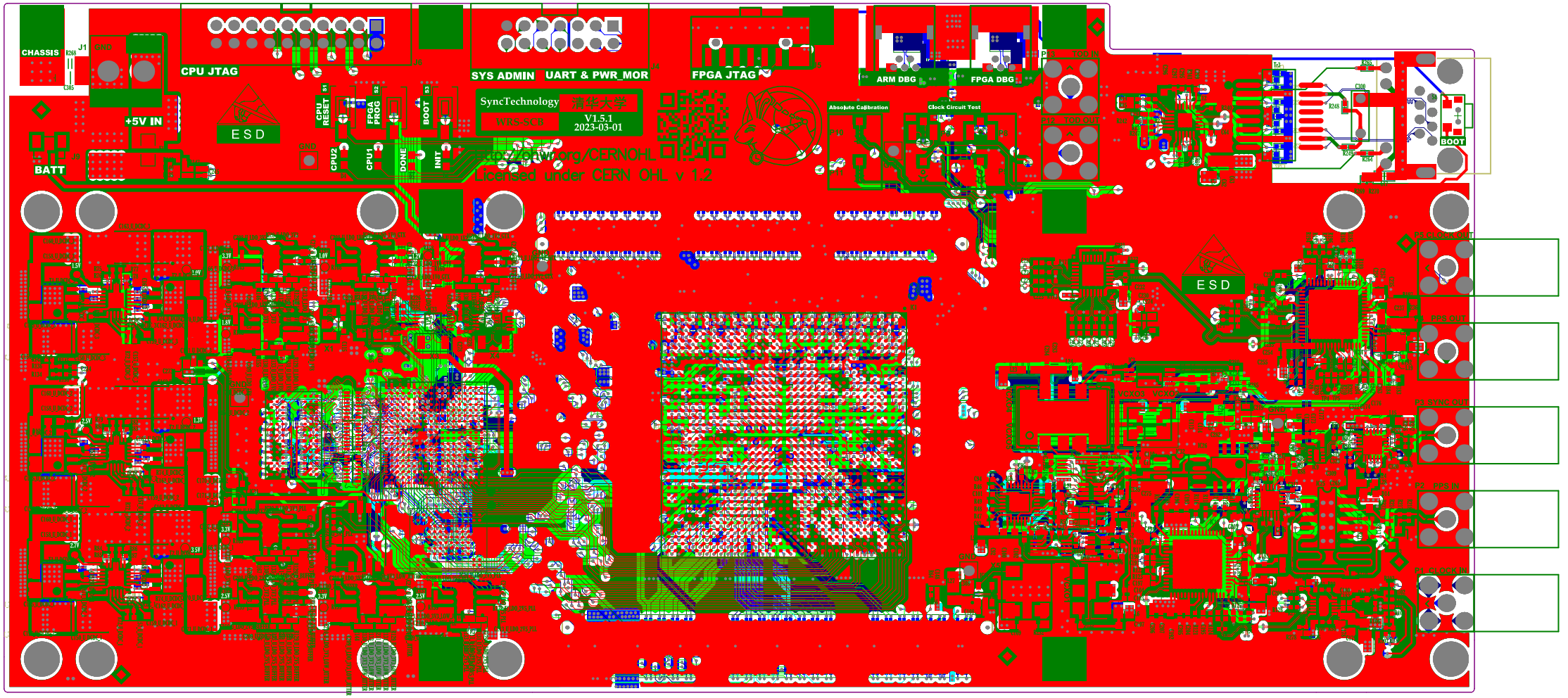
File name	UART_TO_USB.SchDoc		
Revison	1.5	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2023/12/9



File name	WDT_ARM.SchDoc		
Revison	1.5	Organization	Tsinghua University
Project	White Rabbit	Date	2023/12/9



File name	WDT_FPGA.SchDoc		
Revison	1.5	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2023/12/9


CHASSIS
J1
GND
CPU JTAG
+5V IN
ESD
BATT
SYS ADMIN
UART & PWR_MOR
FPGA JTAG
ARM DBG
FPGA DBG
SyncTechnology
清华大学
WRS-SCB
V1.5.1
2023-03-01
CPU1 RESET
FPGA PROG
BOOT
CPU2
CPU1
DONE
INIT
Absolute Calibration
Clock Circuit Test
P12_TOD OUT
P13_TOD IN
BOOT
ESD
P0_CLOCK OUT
P1_PPS OUT
P3_SYNC OUT
P2_PPS IN
P1_CLOCK IN

T 1 2 3 4 B